μCOM 84/87/78K Families
8/16-Bit Microcomputer

Data Book

Contents

Page

Section 4 – The μCOM84 Family

Section 1: General Information

Section 1 – General Information

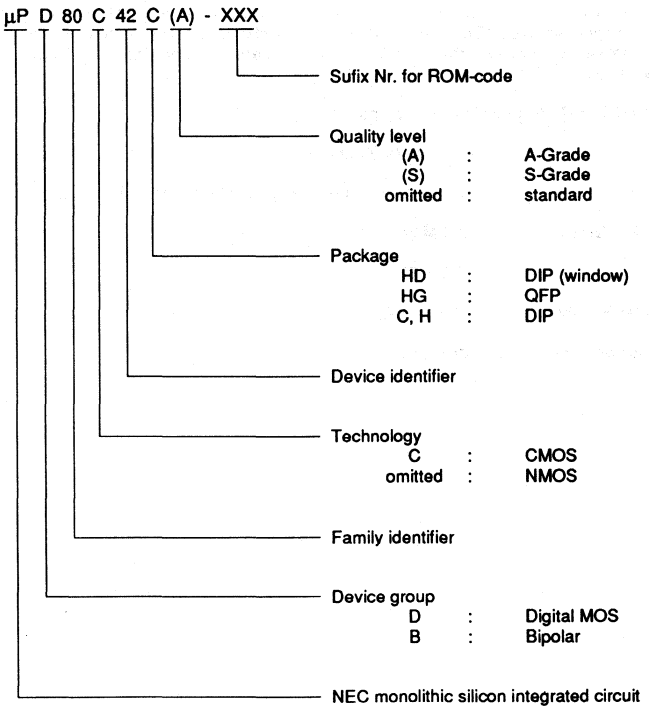
Introduction

NEC offers a wide variety of microprocessors and support products for you to choose from. This volume covers microprocessor, standard peripherals and intelligent peripheral controller products. These products are offered in a variety of processes (NMOS and CMOS) and in a variety of package types. This extraordinary selection of products provides the systems designer with a wide assortment of design alternatives with products that truly fit your data processing, communications, instrumentation, industrial, and telecommunications needs.

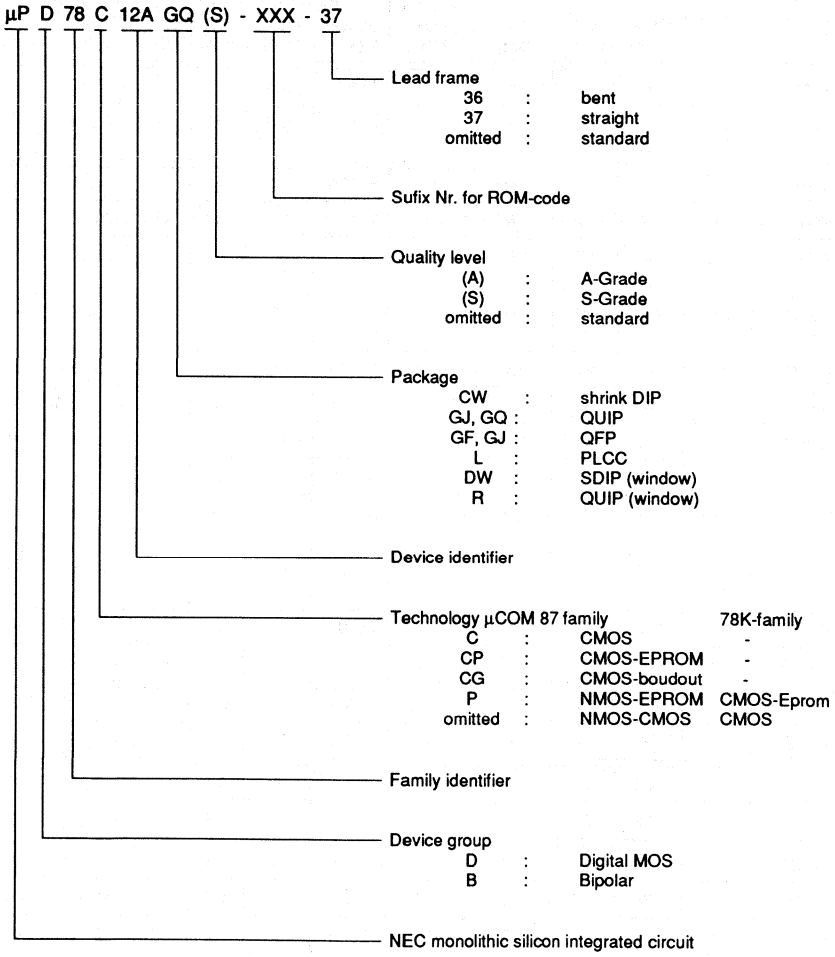
The section GENERAL INFORMATION provides following parts:

		Ordering Number System
Part 1.	**General Information**	This section includes ordering information and product selection guides.
Part 2.	**Microcomputer Family**	**μCOM 84**
Part 3.	**Microcomputer Family**	**μCOM 87**
Part 4.	**Microcomputer Family**	**μPD78XXX**
Part 5.	**Peripherals for Microcomputer**	**μPD71P30X**

Part 1
Ordering Number System for μCOM 84 Family



Ordering Number System for μCOM 87 and 78K Family



μCOM -84X 8 Bit NMOS/CMOS Microcomputers

Device	ROM (Byte)	RAM (Byte)	I/O Lines	Techno-logy	ext. clk max. (MHz)	Power supply (typ.) voltage (V)	active (mA)	hold (mA)	stop (μA)	Operating Temp. T_a/°C	Pins	Package
μPD8041AH	1k	64	18	N		5±10%	135	15	—	0 +70	40	DIP
μPD8741A	UV 1k	64	18	N		5±10%	135	15	—	0 +70	40	DIP (window)
μPD8035HL	—	64	27	N		5±10%	50	4	—	0 +70	40	DIP
μPD8048H	1k	64	27	N		5±10%	50	4	—	0 +70	40	DIP
μPD8748HC	OTP 1k	64	27	N		5±10%	85	2	—	0 +70	40	DIP
μPD8748HD	UV 1k	64	27	N		5±10%	85	2	—	0 +70	40	DIP (window)
μPD8048H(A)	1k	64	27	N		5±10%	50	4	—	-40 +85	40	DIP
μPD8048H(S)	1k	64	27	N		5±10%	50	4	—	-40 +110	40	DIP
μPD8039HLC	2k	128	27	N	11	5±10%	80	5	—	0 +70	40	DIP
μPD8049HC	2k	128	27	N	11	5±10%	80	5	—	0 +70	40	DIP
μPD8749HC	OTP 2k	128	27	N	11	5±10%	85	2	—	0 +70	40	DIP
μPD8749HD	UV 2k	128	27	N	11	5±10%	85	2	—	0 +70	40	DIP (window)
μPD8049HC(A)	2k	128	27	N	11	5±10%	85	5	—	-40 +85	40	DIP
μPD8049HC(S)	2k	128	27	N	11	5±10%	85	5	—	-40 +110	40	DIP
μPD80C48C	1k	64	27	C	6	2.5-6	4	0.4	1	-40 +85	40	DIP
μPD80C35C	—	64	27	C	6	2.5-6	4	0.4	1	-40 +85	40	DIP
μPD80C39C	—	128	27	C	8	2.5-6	6	0.4	1	-40 +85	40	DIP
μPD80C49C	2k	128	27	C	8	2.5-6	6	0.4	1	-40 +85	40	DIP
μPD80C49H	2k	128	27	C	12	2.5-6	6	1.5	1	-40 +85	40	DIP
μPD80C39H	—	128	27	C	12	2.5-6	6	1.5	1	-40 +85	40	DIP
μPD49H	2k	128	27	C	12	2.5-6	6	1.5	1	-40 +85	40	QFP
μPD80C42C	2k	128	18	C	12	2.5-6	10	1.5	1	-40 +85	40	DIP
μPD80C40HG	4k	256	16	C	12	2.5-6	6	1.5	1	-40 +85	44	QFP
μPD80C40HC	4k	256	16	C	12	2.5-6	6	1.5	1	-40 +85	40	DIP
μPD80C50HC	4k	256	16	C	12	2.5-6	6	1.5	1	-40 +85	40	DIP

μCOM -87 Family — 8 Bit NMOS/CMOS Microcomputers

Device	ROM (Byte)	RAM (Byte)	I/O Lines	Techno-logy	ext. clk max. (MHz)	Power supply (typ.) voltage (V)	active (mA)	hold (mA)	stop (μA)	Operating Temp. T_a/°C	Pins	Package
μPD7810CW	—	256	44	N	10[1)]	5±10%	150	1.5		-40 +85	64	SDIP
μPD7810G-36	—	256	44	N	10[1)]	5±10%	150	1.5		-40 +85	64	QUIP
μPD7810HCW	—	256	44	N	15	5±10%	150	1.5		-10 +70	64	SDIP
μPD7810HG36	—	256	44	N	15	5±10%	150	1.5		-10 +70	64	QUIP
μPD7811G-36	4k	256	44	N	10[1)]	5±10%	150	1.5		-40 +85	64	QUIP
μPD7811HCW	4k	256	44	N	15	5±10%	150	1.5		-10 +70	64	SDIP
μPD7811HG-36	4k	256	44	N	15	5±10%	150	1.5		-10 +70	64	QUIP
μPD7811HG-37	4k	256	44	N	15	5±10%	150	1.5		-10 +70	64	QUIP (Straight)
μPD7811G-37	4k	256	44	N	10[1)]	5±10%	150	1.5		-40 +85	64	QUIP (Straight)
μPD78PG11E	4k	256	44	N	10[1)]	5±10%	140	1.5		-40 +85	64	QUIP Piggyback
μPD7810G(A)	—	256	44	N	10[1)]	5±10%	150	1.5		-40 +85	64	QUIP
μPD7811G(A)	4k	256	44	N	10[1)]	5±10%	150	1.5		-40 +85	64	QUIP
μPD78C05AG-36	—	128	30	C	6.25	5±10%	4	1.2	1	-40 +85	64	QUIP
μPD78C06AG-36	4k	128	46	C	6.25	5±10% 2.5-6	4 3	1.2 1	1 1	-40 +85	64	QUIP
μPD7807G-36	—	256	32	N	10[1)]	5±10%	150	1.5		-40 +85	64	QUIP
μPD7807CW-36	—	256	32	N	10[1)]	5±10%	150	1.5		-40 +85	64	SDIP
μPD7808G-36	4k	256	48	N	10[1)]	5±10%	150	1.5		-40 +85	64	QUIP
μPD7808CW-36	4k	256	48	N	10[1)]	5±10%	150	1.5		-40 +85	64	SDIP
μPD7809G-36	8k	256	48	N	10[1)]	5±10%	150	1.5		-40 +85	64	QUIP
μPD7809CW-36	8k	256	48	N	10[1)]	5±10%	150	1.5		-40 +85	64	SDIP
μPD78P09R	UV 8k	256	48	N	12	5±10%	240	1.5		-10 +70	64	QUIP (window)
μPD78P09DW	UV 8k	256	48	N	12	5±10%	240	1.5		-10 +70	64	SDIP (window)
μPD78C10CW	—	256	44	C	15	5±10%	16	8	10	-40 +85	64	SDIP
μPD7810G-1B	—	256	44	C	15	5±10%	16	8	10	-40 +85	64	QFP
μPD78C10GF	—	256	44	C	15	5±10%	16	8	10	-40 +85	64	QFP
μPD78C10G-36	—	256	44	C	15	5±10%	16	8	10	-40 +85	64	QUIP
μPD78C10L	—	256	44	C	15	5±10%	16	8	10	-40 +85	68	PLCC
μPD78C10G-(S)	—	256	44	C	12	5±10%	12	5	10	-40 +110	64	QUIP

Note: 1) 12 MHz can be obtained when limiting supply voltage tollerance to ±5% and T_a = -10°C to +70°C

μCOM -87 Family **8 Bit NMOS/CMOS Microcomputers**

Device	ROM (Byte)	RAM (Byte)	I/O Lines	Techno-logy	ext. clk max. (MHz)	Power supply (typ.) voltage (V)	active (mA)	hold (mA)	stop (μA)	Operating Temp. T_a/°C	Pins	Package
μPD78C10L-(S)	—	256	44	C	12	5±10%	12	5	10	-40 +110	68	PLCC
μPD78C11G-(S) -36	4k	256	44	C	15	5±10%	16	8	10	-40 +110	64	QUIP
μPD78C11L-(S)	4k	256	44	C	15	5±10%	16	8	10	-40 +110	68	PLCC
μPD78C11G-1B	4k	256	44	C	15	5±10%	16	8	10	-40 +85	64	QFP
μPD78C11GF	4k	256	44	C	15	5±10%	16	8	10	-40 +85	64	QFP
μPD78C11G-37	4k	256	44	C	15	5±10%	16	8	10	-40 +85	64	QUIP (Straight)
μPD78C11G-36	4k	256	44	C	15	5±10%	16	8	10	-40 +85	64	QUIP
μPD78C11L	4k	256	44	C	15	5±10%	16	8	10	-40 +85	68	PLCC
μPD78C14CW	16k	256	44	C	15	5±10%	16	8	10	-40 +85	64	SDIP
μPD78C14G-1B	16k	256	44	C	15	5±10%	16	8	10	-40 +85	64	QFP
μPD78C14GF	16k	256	44	C	15	5±10%	16	8	10	-40 +85	64	QFP
μPD78C14G-37	16k	256	44	C	15	5±10%	16	8	10	-40 +85	64	QUIP (Straight)
μPD78C14G-36	16k	256	44	C	15	5±10%	16	8	10	-40 +85	64	QUIP
μPD78C14L	16k	256	44	C	15	5±10%	16	8	10	-40 +85	68	PLCC
μPD78C14G-(A) -36	16k	256	44	C	12	5±10%	16	8	10	-40 +85	64	QUIP
μPD78C14L-(A)	16k	256	44	C	12	5±10%	16	8	10	-40 +85	68	PLCC
μPD78C10ACW	—	256	44	C	15	5±10%	13	7	10	-40 +85	64	SDIP
μPD78C10AGQ -36	—	256	44	C	15	5±10%	13	7	10	-40 +85	64	QUIP
μPD78C10AGF	—	256	44	C	15	5±10%	13	7	10	-40 +85	64	QFP
μPD78C10AL	—	256	44	C	15	5±10%	13	7	10	-40 +85	68	PLCC
μPD78C11ACW	4k	256	44	C	15	5±10%	13	7	10	-40 +85	64	SDIP
μPD78C11AGQ -37	4k	256	44	C	15	5±10%	13	7	10	-40 +85	64	QUIP (Straight)
μPD78C11AGQ -36	4k	256	44	C	15	5±10%	13	7	10	-40 +85	64	QUIP
μPD78C11AGF	4k	256	44	C	15	5±10%	13	7	10	-40 +85	64	QFP
μPD78C11AL	4k	256	44	C	15	5±10%	13	7	10	-40 +85	68	PLCC
μPD78C12ACW	8k	256	44	C	15	5±10%	13	7	10	-40 +85	64	SDIP
μPD78C12AGQ -37	8k	256	44	C	15	5±10%	13	7	10	-40 +85	64	QUIP (Straight)

μCOM -87 Family **8 Bit NMOS/CMOS Microcomputers**

Device	ROM (Byte)	RAM (Byte)	I/O Lines	Technology	ext. clk max. (MHz)	Power supply (typ.) voltage (V)	active (mA)	hold (mA)	stop (μA)	Operating Temp. T_a/°C	Pins	Package	
μPD78C12AGQ -36	8k	256	44	C	15	5±10%	13	7	10	-40 +85	64	QUIP	
μPD78C12AGF	8k	256	44	C	15	5±10%	13	7	10	-40 +85	64	QFP	
μPD78C12AL	8k	256	44	C	15	5±10%	13	7	10	-40 +85	68	PLCC	
μPD78C14AGC	16k	256	44	C	15	5±10%	13	7	10	-40 +85	64	QFP	
μPD78CG14E	Piggyback 16k	256	44	C	15	5±10%	16	8	10	-40 +85	64	QUIP Piggyback	
μPD78CP14CW	OTP 16k	256	44	C	15	5±10%	16	8	10	-40 +85	64	SDIP	
μPD78CP14G-36	OTP 16k	256	44	C	15	5±10%	16	8	10	-40 +85	64	QUIP	
μPD78CP14GF	OTP 16k	256	44	C	15	5±10%	16	8	10	-40 +85	64	QFP	
μPD78CP14L	OTP 16k	256	44	C	15	5±10%	16	8	10	-40 +85	68	PLCC	
μPD78CP14DW	UV 16k	256	44	C	15	5±10%	16	8	10	-40 +85	64	SDIP (window)	
μPD78CP14R	UV 16k	256	44	C	15	5±10%	16	8	10	-40 +85	64	QUIP (window)	
μPD78C18CW	32k	1k	44	C	15	5±10%	tbm	tbm	tbm	-40 +85	64	SDIP	1)
μPD78C18GQ36	32k	1k	44	C	15	5±10%	tbm	tbm	tbm	-40 +85	64	QUIP	1)
μPD78C18GF	32k	1k	44	C	15	5±10%	tbm	tbm	tbm	-40 +85	64	QFP	1)
μPD78C17CW	—	1k	44	C	15	5±10%	tbm	tbm	tbm	-40 +85	64	SDIP	
μPD78C17GQ36	—	1k	44	C	15	5±10%	tbm	tbm	tbm	-40 +85	64	QUIP	
μPD78C17GF	—	1k	44	C	15	5±10%	tbm	tbm	tbm	-40 +85	64	QFP	
μPD78CP18CW	OTP 32k	1k	44	C	15	5±10%	tbm	tbm	tbm	-40 +85	64	SDIP	1)
μPD78CP18G-36	OTP 32k	1k	44	C	15	5±10%	tbm	tbm	tbm	-40 +85	64	QUIP	1)
μPD78CP18GF	OTP 32k	1k	44	C	15	5±10%	tbm	tbm	tbm	-40 +85	64	QFP	1)
μPD78CP18UV	OTP 32k	1k	44	C	15	5±10%	tbm	tbm	tbm	-40 +85	68	LCC (window)	

Note: 1) device in development
tbm: to be measured

μCOM -78K I Family — 8 Bit CMOS Microcomputers

Device	ROM (Byte)	RAM (Byte)	I/O Lines	Technology	ext. clk max. (MHz)	Power supply (typ.) voltage (V)	active (mA)	hold (mA)	stop (μA)	Operating Temp. T_a/°C	Pins	Package
μPD78112CW	8k	192	54	C	12	5±10%	20		(max.) 10	-10 +70	64	SDIP
μPD78112GF -3BE	8k	192	54	C	12	5±10%	20		(max.) 10	-10 +70	64	QFP
μPD78P112GF -3BE	OTP 8k	192	54	C	12	5±10%	20		(max.) 20	-10 +70	64	QFP
μPD78P112CW	OTP 8k	192	54	C	12	5±10%	20	(max.) 20		-10 +70	64	SDIP
μPD78134GF -3BE	16k	384	66	C	12	5±10%	20	10	2	-10 +70	80	QFP
μPD78P134GF	OTP 16k	384	66	C	12	5±10%	20	10		-10 +70	80	QFP

μCOM -78K II Family — 8 Bit CMOS Microcomputers

Device	ROM (Byte)	RAM (Byte)	I/O Lines	Technology	ext. clk max. (MHz)	Power supply (typ.) voltage (V)	active (mA)	hold (mA)	stop (μA)	Operating Temp. T_a/°C	Pins	Package
μPD78212CW	8k	384	54	C	12	5±10%	20	7	5	-40 +85	64	SDIP
μPD78212GQ-36	8k	384	54	C	12	5±10%	20	7	5	-40 +85	64	QUIP
μPD78212GC	8k	384	54	C	12	5±10%	20	7	5	-40 +85	64	QFP
μPD78212GJ	8k	384	54	C	12	5±10%	20	7	5	-40 +85	74	QFP
μPD78212L	8k	384	54	C	12	5±10%	20	7	5	-40 +85	68	PLCC
μPD78213CW	—	512	54	C	12	5±10%	20	7	5	-40 +85	64	SDIP
μPD78213GQ-36	—	512	54	C	12	5±10%	20	7	5	-40 +85	64	QUIP
μPD78213GC	—	512	54	C	12	5±10%	20	7	5	-40 +85	64	QFP
μPD78213GJ	—	512	54	C	12	5±10%	20	7	5	-40 +85	74	QFP
μPD78213L	—	512	54	C	12	5±10%	20	7	5	-40 +85	68	PLCC
μPD78214CW	16k	512	54	C	12	5±10%	20	7	5	-40 +85	64	SDIP
μPD78214GQ-36	16k	512	54	C	12	5±10%	20	7	5	-40 +85	64	QUIP
μPD78214GC	16k	512	54	C	12	5±10%	20	7	5	-40 +85	64	QFP
μPD78214GJ	16k	512	54	C	12	5±10%	20	7	5	-40 +85	74	QFP
μPD78214L	16k	512	54	C	12	5±10%	20	7	5	-40 +85	68	PLCC
μPD78P214DW	UV 16k	512	54	C	12	5±10%	20	7	5	-40 +85	64	SDIP (window)
μPD78P214CW	OTP 16k	512	54	C	12	5±10%	20	7	5	-40 +85	64	SDIP

μCOM -78K II Family **8 Bit CMOS Microcomputers**

Device	ROM (Byte)	RAM (Byte)	I/O Lines	Techno-logy	ext. clk max. (MHz)	Power supply (typ.) voltage (V)	active (mA)	hold (mA)	stop (μA)	Operating Temp. T_a/°C	Pins	Package
μPD78P214GQ -36	OTP 16k	512	54	C	12	5±10%	20	7	5	-40 +85	64	QUIP
μPD78P214GC	OTP 16k	512	54	C	12	5±10%	20	7	5	-40 +85	64	QFP
μPD78P214GJ	OTP 16k	512	54	C	12	5±10%	20	7	5	-40 +85	74	QFP
μPD78P214L	OTP 16k	512	54	C	12	5±10%	20	7	5	-40 +85	68	PLCC
μPD78220L	—	640	55	C	12	5±10%	16	7	5	-40 +85	84	PLCC
μPD78220GJ	—	640	55	C	12	5±10%	16	7	5	-40 +85	94	QFP
μPD78224L	16k	640	71	C	12	5±10%	16	7	5	-40 +85	84	PLCC
μPD78224GJ	16k	640	71	C	12	5±10%	16	7	5	-40 +85	94	QFP
μPD78P224L	OTP 16k	640	71	C	12	5±10%	16	7	5	-40 +85	84	PLCC
μPD78P224GJ	OTP 16k	640	71	C	12	5±10%	16	7	5	-40 +85	94	QFP

μCOM -78K III Family **16 Bit CMOS Microcomputers**

Device	ROM (Byte)	RAM (Byte)	I/O Lines	Techno-logy	ext. clk max. (MHz)	Power supply (typ.) voltage (V)	active (mA)	hold (mA)	stop (μA)	Operating Temp. T_a/°C	Pins	Package
μPD78310CW	—	256	32	C	12	5±10%	30	5	10	-10 +70	64	SDIP
μPD78310G-1B	—	256	32	C	12	5±10%	30	5	10	-10 +70	64	QFP
μPD78310G-36	—	256	32	C	12	5±10%	30	5	10	-10 +70	64	QUIP
μPD78310L	—	256	32	C	12	5±10%	30	5	10	-10 +70	68	PLCC
μPD78312CW	8k	256	48	C	12	5±10%	30	5	10	-10 +70	64	SDIP
μPD78312G-1B	8k	256	48	C	12	5±10%	30	5	10	-10 +70	64	QFP
μPD78312G-36	8k	256	48	C	12	5±10%	30	5	10	-10 +70	64	QUIP
μPD78312L	8k	256	48	C	12	5±10%	30	5	10	-10 +70	68	PLCC
μPD78310ACW	—	256	32	C	12	5±10%	30	5	10	-10 +70	64	SDIP
μPD78310AGF	—	256	32	C	12	5±10%	30	5	10	-10 +70	64	QFP
μPD78310AGQ -36	—	256	32	C	12	5±10%	30	5	10	-10 +70	64	QUIP
μPD78310AL	—	256	32	C	12	5±10%	30	5	10	-10 +70	68	PLCC
μPD78312ACW	8k	256	48	C	12	5±10%	30	5	10	-10 +70	64	SDIP

μCOM -78K III Family **16 Bit CMOS Microcomputers**

Device	ROM (Byte)	RAM (Byte)	I/O Lines	Techno-logy	ext. clk max. (MHz)	Power supply (typ.) voltage (V)	active (mA)	hold (mA)	stop (μA)	Operating Temp. T_a/°C	Pins	Package
μPD78312AGF	8k	256	48	C	12	5±10%	30	5	10	-10 +70	64	QFP
μPD78312AGQ -36	8k	256	48	C	12	5±10%	30	5	10	-10 +70	64	QUIP
μPD78312AL	8k	256	48	C	12	5±10%	30	5	10	-10 +70	68	PLCC
μPD78P312ADW	UV 8k	256	48	C	12	5±10%	30	5	10	-10 +70	64	SDIP (window)
μPD78P312AR	UV 8k	256	48	C	12	5±10%	30	5	10	-10 +70	64	QUIP (window)
μPD78P312ACW	OTP 8k	256	48	C	12	5±10%	30	5	10	-10 +70	64	SDIP
μPD78P312AGF	OTP 8k	256	48	C	12	5±10%	30	5	10	-10 +70	64	QFP
μPD78P312AGQ -36	OTP 8k	256	48	C	12	5±10%	30	5	10	-10 +70	64	QUIP
μPD78P312AL	OTP 8k	256	48	C	12	5±10%	30	5	10	-10 +70	68	PLCC
μPD78320L	—	640	37	C	16	5±10%	40	20	10	-10 +70	68	PLCC
μPD78320L(A)	—	640	37	C	16	5±10%	40	25	20	-40 +85	68	PLCC
μPD78320L(S)	—	640	37	C	16	5±10%	40	25	20	-40 +110	68	PLCC
μPD78320GJ	—	640	37	C	16	5±10%	40	20	10	-10 +70	74	QFP
μPD78320GJ(A)	—	640	37	C	16	5±10%	40	25	20	-40 +85	74	QFP
μPD78320GJ(S)	—	640	37	C	16	5±10%	40	25	20	-40 +110	74	QFP
μPD78322L	16k	640	55	C	16	5±10%	40	20	10	-10 +70	68	PLCC
μPD78322L(A)	16k	640	55	C	16	5±10%	40	25	20	-40 +85	68	PLCC
μPD78322L(S)	16k	640	55	C	16	5±10%	40	25	20	-40 +110	68	PLCC
μPD78322GJ	16k	640	55	C	16	5±10%	40	20	10	-10 +70	74	QFP
μPD78322GJ(A)	16k	640	55	C	16	5±10%	40	25	20	-40 +85	74	QFP
μPD78322GJ(S)	16k	640	55	C	16	5±10%	40	25	20	-40 +110	74	QFP
μPD78P322L	OTP 16k	640	55	C	16						68	PLCC
μPD78P322GJ	OTP 16k	640	55	C	16						74	QFP
μPD78P322KC	UV 16k	640	55	C	16						68	LCC (window)
μPD78P322KD	UV 16k	640	55	C	16						74	ceramic LCC (window)

μCOM -78K III Family **16 Bit CMOS Microcomputers**

Device	ROM (Byte)	RAM (Byte)	I/O Lines	Technology	ext. clk max. (MHz)	Power supply (typ.) voltage (V)	active (mA)	hold (mA)	stop (μA)	Operating Temp. T_a/°C	Pins	Package
μPD78327CW	—	512	52	C	16	5±10%	40	20	10	-10 +70	64	SDIP
μPD78327GF	—	512	52	C	16	5±10%	40	20	10	-10 +70	64	QFP
μPD78328CW	16k	512	52	C	16	5±10%	40	20	10	-10 +70	64	SDIP
μPD78328GF	16k	512	52	C	16	5±10%	40	20	10	-10 +70	64	QFP
μPD78P328DW	UV 16k	512	52	C	16	5±10%					64	SDIP (window)
μPD78P328KB	UV 16k	512	52	C	16	5±10%					64	ceramic LCC (window)
μPD78330L	—	1k	62	C	16	5±10%	40	20	10	-10 +70	84	PLCC
μPD78330L(A)	—	1k	62	C	16	5±10%	45	25	10	-40 +85	84	PLCC
μPD78330L(S)	—	1k	62	C	12	5±10%	45	25	10	-40 +110	84	PLCC
μPD78330L-10	—	1k	62	C	20	5±5%	45	25	10	-10 +70	84	PLCC
μPD78330GJ	—	1k	62	C	16	5±10%	40	20	10	-10 +70	94	QFP
μPD78330GJ(A)	—	1k	62	C	16	5±10%	45	25	10	-40 +85	94	QFP
μPD78330GJ(S)	—	1k	62	C	12	5±10%	45	25	10	-40 +110	94	QFP
μPD78330GJ-10	—	1k	62	C	20	5±5%	45	25	10	-10 +70	94	QFP
μPD78334L	32k	1k	62	C	16	5±10%	40	20	10	-10 +70	84	PLCC
μPD78334L(A)	32k	1k	62	C	16	5±10%	45	25	10	-40 +85	84	PLCC
μPD78334L(S)	32k	1k	62	C	12	5±10%	45	25	10	-40 +110	84	PLCC
μPD78334L-10	32k	1k	62	C	20	5±5%	40	20	10	-10 +70	84	PLCC
μPD78334GJ	32k	1k	62	C	16	5±10%	40	20	10	-10 +70	94	QFP
μPD78334GJ(A)	32k	1k	62	C	16	5±10%	45	25	10	-40 +85	94	QFP
μPD78334GJ(S)	32k	1k	62	C	12	5±10%	45	25	10	-40 +110	94	QFP
μPD78334GJ-10	32k	1k	62	C	20	5±5%	40	20	10	-10 +70	94	QFP
μPD78P334L	OTP 32k	1k	62	C							84	PLCC
μPD78P334GJ	OTP 32k	1k	62	C							94	QFP

Part 5

μCOM -78K VI Family — 16 Bit CMOS Microcomputers

Device	ROM (Byte)	RAM (Byte)	I/O Lines	Techno-logy	ext. clk max. (MHz)	Power supply (typ.) voltage (V)	active (mA)	hold (mA)	stop (μA)	Operating Temp. T_a/°C	Pins	Package
μPD78600	—	1k	52	C	25	5±10%	80	TBD	TBD	-40 +110	84/94	PLCC/Flat
μPD78602	16k	1k	68	C	25	5± 10%	80	TBD	TBD	-40 +110	84/94	PLCC/Flat

μCOM -71 — peripherals for Microcomputers

Device	ROM (Byte)	RAM (Byte)	I/O Lines	Techno-logy	ext. clk max. (MHz)	Power supply (typ.) voltage (V)	active (mA)	hold (mA)	stop (μA)	Operating Temp. T_a/°C	Pins	Package
μPD71P301KA	UV 16k	1k	16	C	16	5±10%	40		1	-10 +70	44	LCC (window)
μPD71P301KB	UV 16k	1k	16	C	16	5±10%	40		1	-10 +70	64	LCC (window)
μPD71P301L	16k	1k	16	C	16	5±10%	40		1	-10 +70	44	PLCC
μPD71P301GF -3BE	16k	1k	16	C	16	5±10%	40		1	-10 +70	64	QFP
μPD71P302KB	UV 16k	1k	32	C	16	5±10%	40		1	-10 +70	64	LCC (window)
μPD71P302GF	16k	1k	32	C	16	5±10%	40		1	-10 +70	64	QFP
μPD71302RQ	UV 16k	1k	32	C	16	5±10%	40		1	-10 +70	64	QUIP (window)
μPD71P302GQ	16k	1k	32	C	16	5±10%	40		1	-10 +70	64	QUIP
μPD71P302KC	16k	1k	32	C	16	5±10%	40		1	-10 +70	68	LCC (window)
μPD71P302L	16k	1k	32	C	16	5±10%	40		1	-10 +70	68	PLCC

Section 2: The μCOM78K Family

Section 2 – The μCOM78K Family

Description

The μPD78112 is a 8-bit CMOS single-chip microcomputer. In addition to 8-bit CPU, ROM (8192 x 8 bits), and RAM (192 x 8 bits), devices such as a serial interface, an A/D converter, a PWM output unit, and a servo control unit are integrated on a single CMOS chip.

This microcomputer has many servo system control functions, best suited for controlling various servo systems like VCR, DAT etc. Moreover, since the functions of conventional large and bulky servo systems have been integrated on a single chip, this computer can miniaturize a servo system drastically. For prototyping a programmable version (μPD78P112) is available.

Features

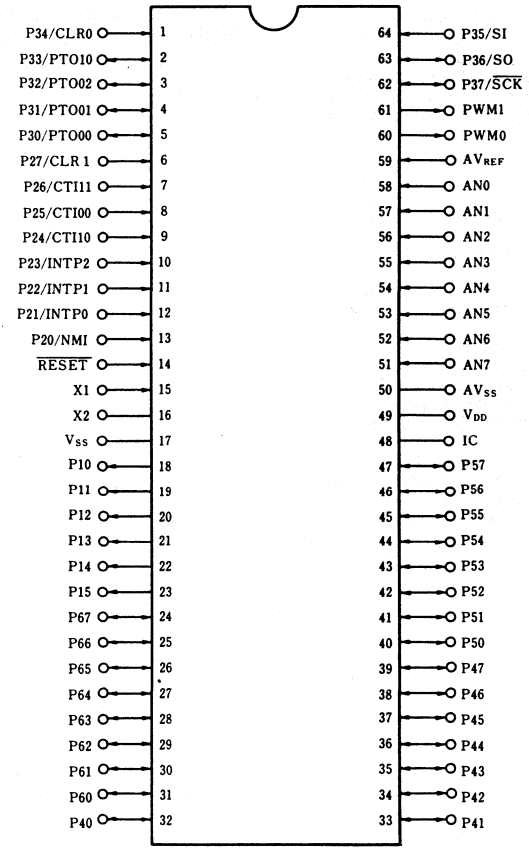
- □ μCOM-78KI single chip microcomputer
- □ High instruction execution speed (instruction cycle; 333 ns/12 MHz)
- □ Memory mapping of internal peripheral hardware (special registers)
- □ Internal interrupt controller providing two interrupt processing formats: vector interrupt and macro service functions.
- □ Highly accurate internal A/D converter
  - 8-bit precision: 8 analog inputs
  - Conversion time per analog input: 26.7 μs/12 MHz
- □ Internal hardware (servo control unit) suited for controlling servo systems such as VCRs, industrial control etc.
  - 16-bit free running counter and two capture registers
  - 16-bit phase difference counter and capture register
  - Special pulse output control function
  - Two 12-bit precision PWM outputs

Ordering Information

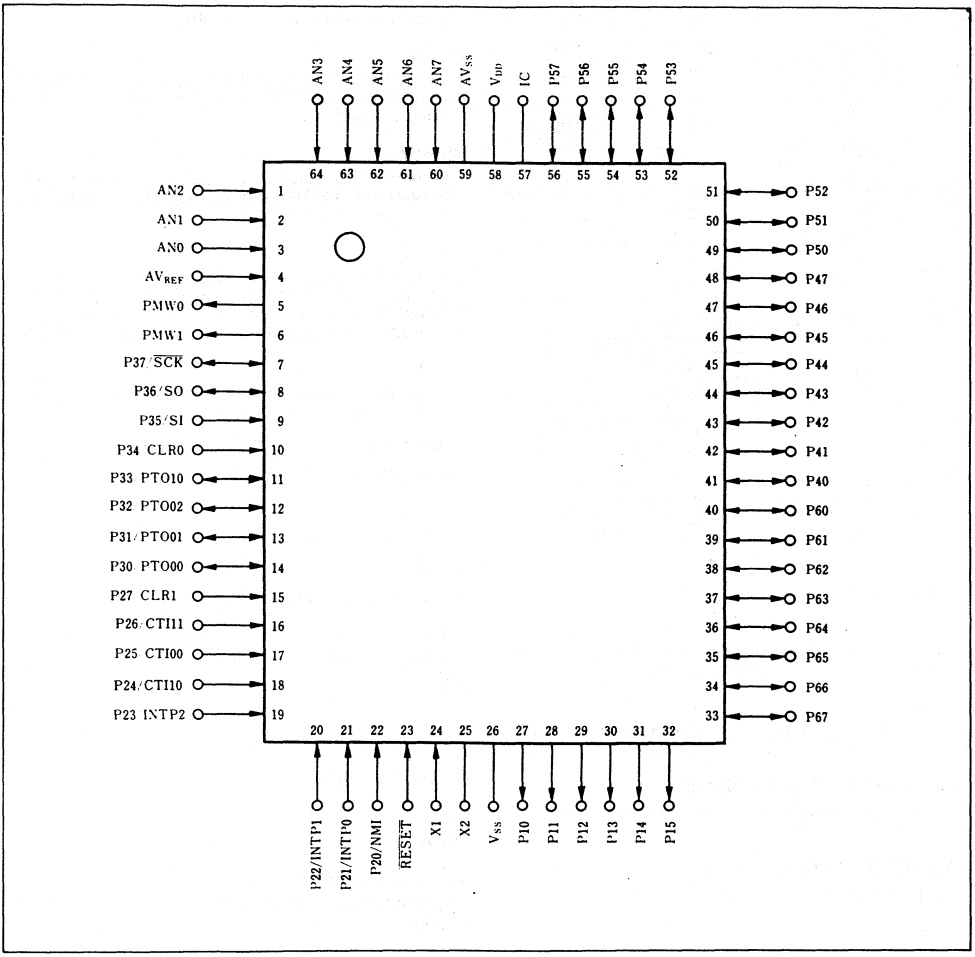
Part Number	Package	Type	ROM
μPD78112CW	64-pin	SDIP	8K Mask ROM
μPD78112GF-3BE	64-pin	FLAT	8K Mask ROM
μPD78P112GF-3BE	64-pin	FLAT	8K OTPROM Version
μPD78P112CW	64-pin	SDIP	8K OTPROM Version

2

Pin Configuration
64-Pin SDIP



Pin Configuration
64-Pin Flat



2

Pin Identification (SDIP)

No	Symbol	Function
1	CLR 0/P34	Port 34/Timer Clear Input
2-5	P33-30/PTO10-PTO00	Port 30-33/Timer Outputs
6	P27/CLR1	Port 27/Timer 1 Clear Input
7-9	P24-26/CTI11-00	Port 24-26/Capture Trigger Input
10-12	P21-23/INTP2-0	Port 21-23/Peripheral Interrupt
13	P20/NMI	Port 20/Nonmaskable Interrupt
14	RESET	Reset Input
15, 16	X1, X2	Crystal
17	V_{SS}	Ground
18-23	P10-P15	Port 1
24-31	P67-P60	Port 6
32-39	P40-P47	Port 4
40-47	P50-P57	Port 5
48	IC	Internally Connected
49	V_{DD}	Supply Voltage
50-58	AN7-AN0	Analog Inputs
59	AV_{REF}	Analog Reference Voltage
60-61	PWM 0,1	Pulse with Modulation Outputs
62	P37/SCK	Port 37/Serial Clock
63	P36 ISO	Port 36/Serial Output
64	P35/SI	Port 35/Serial Input

Pin Functions

P10-P15
PORT 1 is a 6-bit output port with direct LED drive capability. Output enable/disable can specified bit wise.

NMI/P20
Input PORT or nonmaskable interrupt input Pin. Rising or falling edge can be specified by software.

INTP01/P21, INTP1/P22, INTP2/P23
Input port or interrupt request input. Detection edge can be specified by software.

CTI00/P25, CTI10/P24, CTI11/P26
Input port or Super Timer capture trigger inputs.

CLR1/P27
Super Timer. Timer clear input.

PTO00/30, PTO01/31, PTO02/P32, PTO10/P33
I/O port or Super Timer output.

CLR0/P34
Input port or Super Timer clear input.

SI/P35
Input port or serial data input pin.

SO/P36
Input port or serial output.

$\overline{SCK}$/P37
Input port or serial clock input/output.

P40-P47
8-bit input/output port 4. Input/output can be specified in 8-bit units. For μPD78P112 in programming mode port 4 is used as a data bus.

P50-P57
8-bit input/output port 5. Input/output can be specified in 8-bit units. For μPD78P112 in programming mode ports is used as address bus A_0 to A_7.

P60-P67
8-bit input/output port 6. Input/output can be specified in 8-bit units. For μPD78P112 in programming mode P60 to P64 is used as address bus A_8 to A_{12}, P66 as the output enable signal ($\overline{OE}$) and P67 as the chip enable input ($\overline{CE}$).

X1, X2
Crystal input/output for system clock oscillator. X1 can be used as an external clock input.

PWM0, PWM1
Pulse width modulator outputs.

AN0-AN7
A/D converter inputs.

AV_{REF}
Reference voltage input for the A/D converter.

AV_{SS}
Analog ground for the A/D converter.

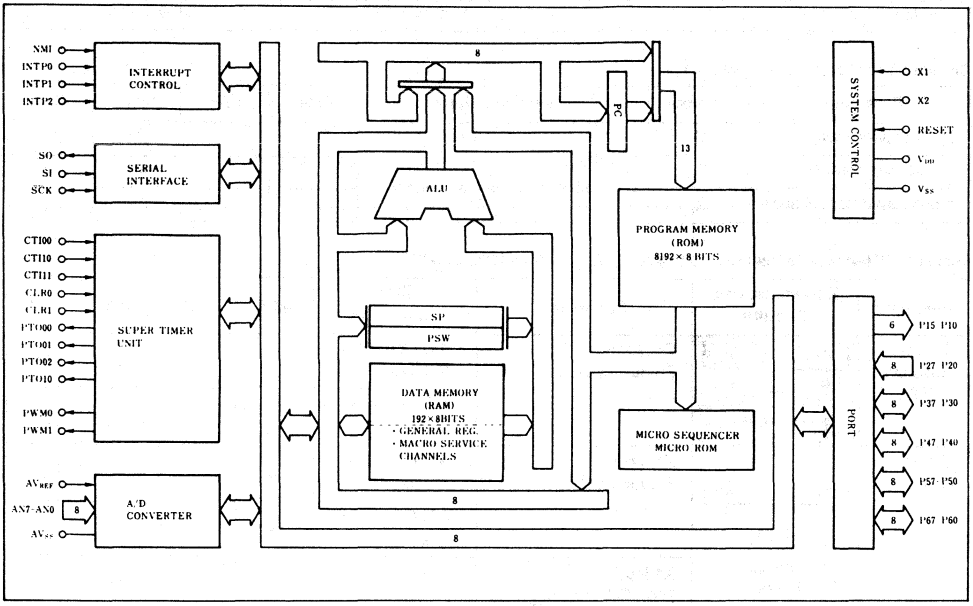
$\overline{RESET}$
System reset input.

V_{DD}
Power supply input.

V_{SS}
Ground

V_{PP} (only for 78P112)
Programming voltage. If not used V_{PP} must be connected to V_{DD}.

Block Diagram
μPD78112



Absolute Maximum Ratings ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Ratings	Unit
Power voltage	V_{DD}		−0.5 to +7.0	V
	AV_{SS}		−0.5 to +0.5	V
A/D converter reference input voltage	AV_{REF}		−0.5 to V_{DD} +0.3	V
Input voltage	V_I		−0.5 to V_{DD} +0.5	V
Output voltage	V_O		−0.5 to V_{DD} +0.5	V
Low-level output current	I_{OL}	1 pin	10	mA
		Total	60	mA
High-level output current	I_{OH}	1 pin	−1	mA
		Total	−20	mA
Operating temperature	T_{opt}	4 MHz ≦ f_{XX} ≦ 12 MHz	−10 to +70	°C
Storage temperature	T_{stg}		−65 to +150	°C

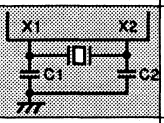
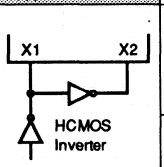
Operating Conditions

Oscillation Frequency	T_a	V_{DD}
4 MHz ≤ f_{XX} ≤ 12 MHz	-10°C to +70°C	+5.0 V ±10%

Capacitance (Ta=25°C, V_{DD}=V_{SS}=0V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1MHz 0V at all pins except the tested pins			20	pf
Output capacitance	C_O				20	pf
Input/output capacitance	C_{IO}				20	pf

Oscillator Characteristics (Ta=-10 to +70°C, V_{DD}=+5.0V ±10%, V_{SS}=0V)

Resonator	Recommended Circuits	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic Resonator or XTAL*1		Oscillation Frequency (f_{XX})	A/D Converter Not used	4		12	MHz
			A/D Converter Used	6		12	MHz
External Clock		X1 Input Frequency (f_X)	A/D Converter Not used	4		12	MHz
			A/D Converter Used	6		12	MHz
		X1 Input Rise, Fall Time (t_{XR}, t_{XF})		0		20	ns
		X1 Input High, Low Level Width (t_{WXH}, t_{WXL})		30		220	ns

*1: For XTAL, the following external capacitances are recommended:
C_1=C_2=15pf

Note:
(1) External oscillation circuit should be connected at the minimum distance from X1 and X2 pins.
(2) No other signal line should cross the area ▨

DC Characteristics (T_a = −10°C to +70°C, V_{DD} = +5.0 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL1}	Except $\overline{RESET}$, P20 to P27, and P34 to P37	0		0.8	V
	V_{IL2}	$\overline{RESET}$, P20 to P27, P34 to P37	0		0.2 V_{DD}	V
High-level input voltage	V_{IH1}	Except $\overline{RESET}$, P20 to P27, P34 to P37 X1, and X2	2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, P20 to P27, P34 to P37, X1, and X2	0.8 V_{DD}		V_{DD}	V
Low-level output voltage	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
	V_{OL2}	I_{OL} = 8.0 mA			1.5	V
High-level output voltage	V_{OH}	I_{OH} = −400 μA	2.4			V
Input leak current	I_{LI}	0 V ≦ V_I ≦ V_{DD}			±10	μA
Output leak current	I_{LO}	0 V ≦ V_I ≦ V_{DD}			±10	μA
V_{DD} power current	I_{DD1}	Operating mode, f_{XX} = 12 MHz		20	45	mA
	I_{DD2}	STOP mode			10	μA

AC Characteristics

Clock operations (T_a = −10°C to +70°C, V_{DD} = +5.0 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Internal system clock cycle time	t_{CYK}		166		ns
X1 input cycle time	t_{CYX}		83	250	ns
X1 input high and low-level widths	t_{WXH}, t_{WXL}		30	220	ns
X1 input rising and falling times	t_{XR}, t_{XF}		0	30	ns

NOTE: The internal system clock (f_{CLK}) is obtained by dividing the oscillation clock (f_{XX}) or an external input clock (f_X) by two.

$t_{CYK} = 1/f_{CLK}$

Serial Operations (T_a = −10°C to +70°C, V_{DD} = +5.0 V ±10%, V_{SS} = 0 V)

Paramter	Symbol	Test Conditions		MIN.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{CYSK}	Output	f_{CLK}/8 is selected as clock source.	1.33		μs
			f_{CLK}/32 is selected as clock source.	5.33		μs
		Input		0.95		μs
$\overline{SCK}$ high and low-level widths	t_{WSKH} t_{WSKL}	Output (NOTE 1)	f_{CLK}/8 is selected as clock source.	0.62		μs
			f_{CLK}/32 is selected as clock source.	2.62		μs
		Input (NOTE 2)		0.43		μs
SI setup time for $\overline{SCK}$↑)	t_{SSISK}			100		ns
SI hold time for $\overline{SCK}$↑)	t_{HSKSI}			300		ns
$\overline{SCK}$↓→ SO delay time	t_{DSKSO}				300	ns

NOTE 1: t_{WSKH}, t_{WSKL} = t_{CYSK}/2−50
NOTE 2: t_{WSKH}, t_{WSKL} = t_{CYSK}/2−40

A/D Converter Characteristics

(T_a = −10°C to + 70°C, V_{DD} = +5 V ±10%, V_{DD} −0.5 V < AV_{REF} < V_{DD}, AV_{SS} = V_{SS} = 0 V)

Paramter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8			bit
Full-scale error		6 MHz ≦ f_{XX} ≦ 12 MHz			0.6	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	6 MHz ≦ f_{XX} ≦ 12 MHz	160			t_{CYK}
Sampling time	t_{SAMP}	6 MHz ≦ f_{XX} ≦ 12 MHz	28			t_{CYK}
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	AV_{REF}		V_{DD} −0.5		V_{DD}	V
AV_{REF} current	AI_{REF}			0.5	1.5	mA

Other Operations ($T_a = -10°C$ to $+70°C$, $V_{DD} = 5.0\ V \pm 10\%$, $V_{SS} = 0\ V$)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
CTI00/10/11 high/low-level width	t_{WCTH}, t_{WCTL}		4		t_{CYK}
CLR1 high/low-level width	t_{WCRIH} t_{WCRIL}	When a noise suppressor is not used.	4		t_{CYK}
		When a noise suppressor is used.	48		t_{CYK}
NMI high/low-level width	t_{WNIH} t_{WNIL}		10		μs
INTP0 to INTP2 high/low-level widths	t_{WIPH}, t_{WIPL}		4		t_{CYK}
$\overline{RESET}$ high/low-level width	t_{WRSH}, t_{WRSL}		10		μs

2

Absolute Maximum Ratings ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Ratings	Unit
Power voltage	V_{DD}		−0.5 to +7.0	V
	AV_{SS}		−0.5 to +0.5	V
A/D converter reference input voltage	AV_{REF}		−0.5 to V_{DD} +0.3	V
Input voltage	V_I		−0.5 to V_{DD} +0.5	V
Output voltage	V_O		−0.5 to V_{DD} +0.5	V
Low-level output current	I_{OL}	1 pin	10	mA
		Total	60	mA
High-level output current	I_{OH}	1 pin	−1	mA
		Total	−20	mA
Operating temperature	T_{opt}	4 MHz ≦ f_{XX} ≦ 12 MHz	−10 to +70	°C
Storage temperature	T_{stg}		−65 to +150	°C

2

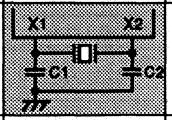
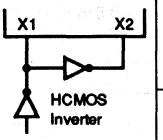
Operating Conditions

Oscillation Frequency	T_a	V_{DD}
4 MHz ≤ f_{XX} ≤ 12 MHz	-10°C to +70°C	+5.0 V ±10%

Capacitance (Ta=25°C, $V_{DD}=V_{SS}=0V$)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1MHz 0V at all pins except the tested pins			20	pf
Output capacitance	C_O				20	pf
Input/output capacitance	C_{IO}				20	pf

Oscillator Characteristics (Ta=-10 to +70°C, V_{DD}=+5.0V ±10%, V_{SS}=0V)

Resonator	Recommended Circuits	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic Resonator or XTAL*1		Oscillation Frequency (f_{XX})	A/D Converter Not used	4		12	MHz
			A/D Converter Used	6		12	MHz
External Clock		X1 Input Frequency (f_X)	A/D Converter Not used	4		12	MHz
			A/D Converter Used	6		12	MHz
		X1 Input Rise, Fall Time (t_{XR}, t_{XF})		0		20	ns
		X1 Input High, Low Level Width (t_{WXH}, t_{WXL})		30		220	ns

*1: For XTAL, the following external capacitances are recommended:
C_1=C_2=15pf

Note:
(1) External oscillation circuit should be connected at the minimum distance from X1 and X2 pins.
(2) No other signal line should cross the area ▨

DC Characteristics (T_a = −10°C to +70°C, V_{DD} = +5.0 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL1}	Except $\overline{RESET}$, P20 to P27, and P34 to P37	0		0.8	V
	V_{IL2}	$\overline{RESET}$, P20 to P27, P34 to P37	0		0.2 V_{DD}	V
High-level input voltage	V_{IH1}	Except $\overline{RESET}$, P20 to P27, P34 to P37 X1, and X2	2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, P20 to P27, P34 to P37, X1, and X2	0.8 V_{DD}		V_{DD}	V
Low-level output voltage	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
	V_{OL2}	I_{OL} = 8.0 mA			1.5	V
High-level output voltage	V_{OH}	I_{OH} = −400 μA	2.4			V
Input leak current	I_{LI}	0 V ≦ V_I ≦ V_{DD}			±10	μA
Output leak current	I_{LO}	0 V ≦ V_I ≦ V_{DD}			±10	μA
V_{DD} power current	I_{DD1}	Operating mode, f_{XX} = 12 MHz		20	45	mA
	I_{DD2}	STOP mode			20	μA

2

AC Characteristics

Clock operations (T_a = −10°C to +70°C, V_{DD} = +5.0 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Internal system clock cycle time	t_{CYK}		166		ns
X1 input cycle time	t_{CYX}		83	250	ns
X1 input high and low-level widths	t_{WXH}, t_{WXL}		30	220	ns
X1 input rising and falling times	t_{XR}, t_{XF}		0	30	ns

NOTE: The internal system clock (f_{CLK}) is obtained by dividing the oscillation clock (f_{XX}) or an external input clock (f_X) by two.

$t_{CYK} = 1/f_{CLK}$

Serial Operations (T_a = −10°C to +70°C, V_{DD} = +5.0 V ±10%, V_{SS} = 0 V)

Paramter	Symbol	Test Conditions		MIN.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{CYSK}	Output	f_{CLK}/8 is selected as clock source.	1.33		μs
			f_{CLK}/32 is selected as clock source.	5.33		μs
		Input		0.95		μs
$\overline{SCK}$ high and low-level widths	t_{WSKH} t_{WSKL}	Output (NOTE 1)	f_{CLK}/8 is selected as clock source.	0.62		μs
			f_{CLK}/32 is selected as clock source.	2.62		μs
		Input (NOTE 2)		0.43		μs
SI setup time for $\overline{SCK}$↑)	t_{SSISK}			100		ns
SI hold time for $\overline{SCK}$↑)	t_{HSKSI}			300		ns
$\overline{SCK}$↓→ SO delay time	t_{DSKSO}				300	ns

NOTE 1: t_{WSKH}, t_{WSKL} = t_{CYSK}/2−50
NOTE 2: t_{WSKH}, t_{WSKL} = t_{CYSK}/2−40

A/D Converter Characteristics

(T_a = −10°C to + 70°C, V_{DD} = +5 V ±10%, V_{DD} −0.5 V < AV_{REF} < V_{DD}, AV_{SS} = V_{SS} = 0 V)

Paramter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8			bit
Full-scale error		6 MHz ≦ f_{XX} ≦ 12 MHz			0.6	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	6 MHz ≦ f_{XX} ≦ 12 MHz	160			t_{CYK}
Sampling time	t_{SAMP}	6 MHz ≦ f_{XX} ≦ 12 MHz	28			t_{CYK}
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	AV_{REF}		V_{DD} −0.5		V_{DD}	V
AV_{REF} current	AI_{REF}			0.5	1.5	mA

Other Operations ($T_a = -10°C$ to $+70°C$, $V_{DD} = 5.0\ V \pm 10\%$, $V_{SS} = 0\ V$)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
CTI00/10/11 high/low-level width	t_{WCTH}, t_{WCTL}		4		t_{CYK}
CLR1 high/low-level width	t_{WCRIH} t_{WCRIL}	When a noise suppressor is not used.	4		t_{CYK}
		When a noise suppressor is used.	48		t_{CYK}
NMI high/low-level width	t_{WNIH} t_{WNIL}		10		μs
INTP0 to INTP2 high/low-level widths	t_{WIPH}, t_{WIPL}		4		t_{CYK}
$\overline{RESET}$ high/low-level width	t_{WRSH}, t_{WRSL}		10		μs

DC Programming Characteristics ($T_a = 25 \pm 5°C$, $V_{IP} = 12.0 \pm 0.5\ V$, $V_{SS} = 0\ V$)

Parameter	Symbol	Symbol (NOTE)	Test Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}	V_{IH}		2.4		V_{DDP} +0.3	V
Low-level input voltage	V_{IL}	V_{IL}		−0.3		0.8	V
Input leak current	V_{LIP}	V_{LI}	$0 \leqq V_I \leqq V_{DDP}$			10	μA
High-level output voltage	V_{OH}	V_{OH}	$I_{OH} = -400\ \mu A$	2.4			V
Low-level output voltage	V_{OL}	V_{OL}	$I_{OH} = 2.0\ mA$			0.45	V
Output leak current	I_{LO}		$0 \leqq V_O \leqq V_{DDP}$, $\overline{OE} = V_{IH}$			10	μA
PROG pin High-voltage input current	I_{IP}					±10	μA
V_{DDP} power voltage	V_{DDP}	V_{DD}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} power voltage	V_{PP}	V_{PP}	Program memory write mode	12.5	12.5	12.8	V
			Program memory read mode	$V_{PP} = V_{DDP}$			V
V_{DDP} power current	I_{DD}	I_{DD}	Program memory write mode		5	30	mA
			Program memory read mode $\overline{CE} = V_{IL}$, $V_I = V_{IH}$		5	30	mA
V_{PP} power current	I_{PP}	I_{PP}	Program memory write mode $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		5	30	mA
			Program memory read mode		1	100	μA

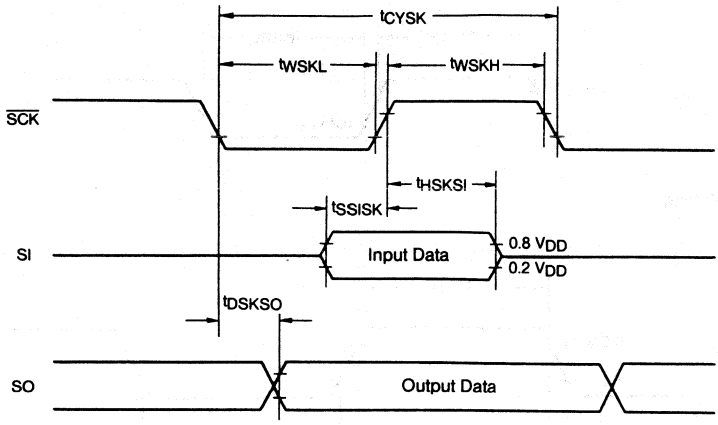
NOTE: Symbol corresponding to μPD27C256A

AC Programming Characteristics (T_a = 25 ±5°C, V_{IP} = 12.0 ±0.5 V, V_{SS} = 0 V)

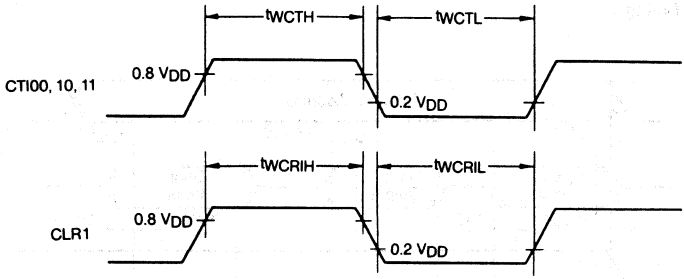
Parameter	Symbol	Symbol (NOTE)	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (for $\overline{CE}\downarrow$)	t_{SAC}	t_{AS}		2			μs
Data → $\overline{OE}\downarrow$ delay time	t_{DDOO}	t_{OES}		2			μs
Input data setup time (for $\overline{CE}\downarrow$)	t_{SIDC}	t_{DS}		2			μs
Address hold time (for $\overline{CE}\uparrow$)	t_{HCA}	t_{AH}		2			μs
Input data hold time (for $\overline{CE}\uparrow$)	t_{HCID}	t_{DH}		2			μs
Output data hold time (for $\overline{OE}\uparrow$)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} setup time (for $\overline{CE}\downarrow$)	t_{SVPC}	t_{VPS}		1			ms
V_{DDP} setup time (for $\overline{CE}\downarrow$)	t_{SVDC}	t_{VDS}		1			ms
Initial program pulse width	t_{WLI}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{WL2}	t_{OPW}		2.85		78.75	ms
PROG high-voltage input setup time (for $\overline{CE}\downarrow$)	t_{SPC}			2			μs
Address → data output time	t_{DAOD}	t_{ACC}	PROG = $\overline{OE}$ = V_{IL}			2	μs
$\overline{CE}\downarrow$ → data output time	t_{DCOD}	t_{CE}	$\overline{OE}$ = V_{IL}			2	μs
$\overline{OE}\downarrow$ → data output time	t_{DOOD}	t_{OE}				1	μs
Data hold time (for $\overline{OE}\uparrow$)	t_{HCOD}	t_{DF}	PROG = V_{IL}	0		130	ns
Data hold time (for address)	t_{HAOD}	t_{OH}	PROG = $\overline{OE}$ = V_{IL}	0			ns

NOTE: Symbol corresponding to μPD27C256A

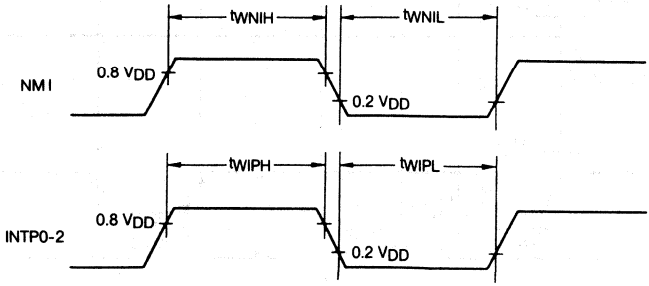
Serial Operation Timing



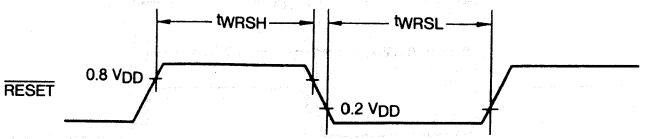
Super Timer Input Timing



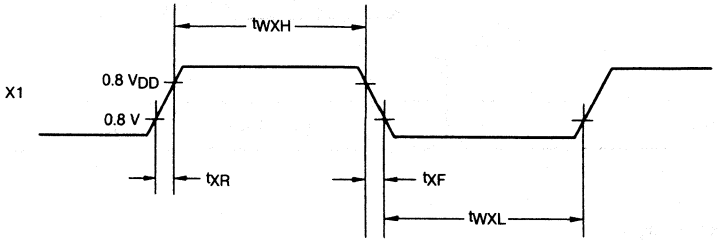
Interrupt Input Timing



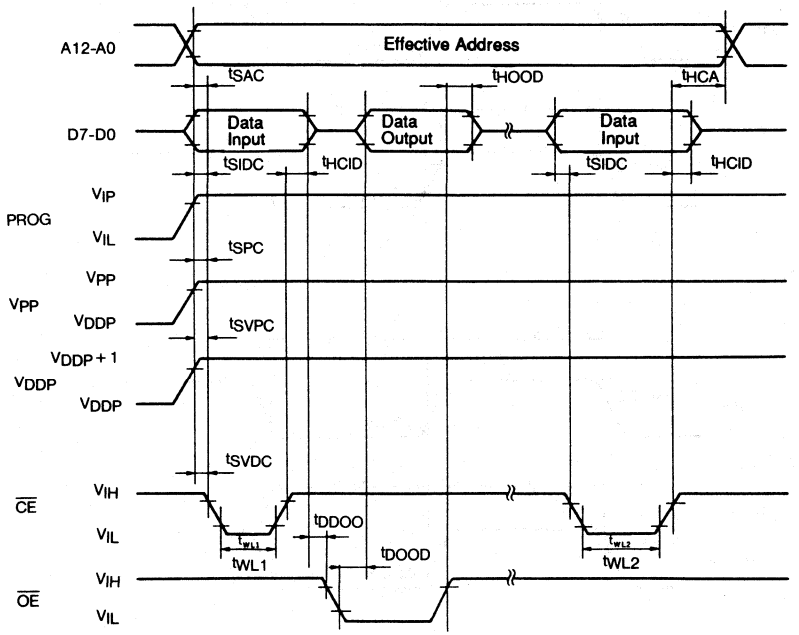
Reset/Input Timing



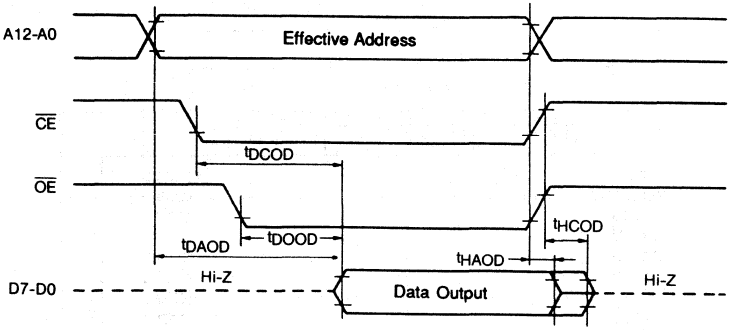
External Clock Timing



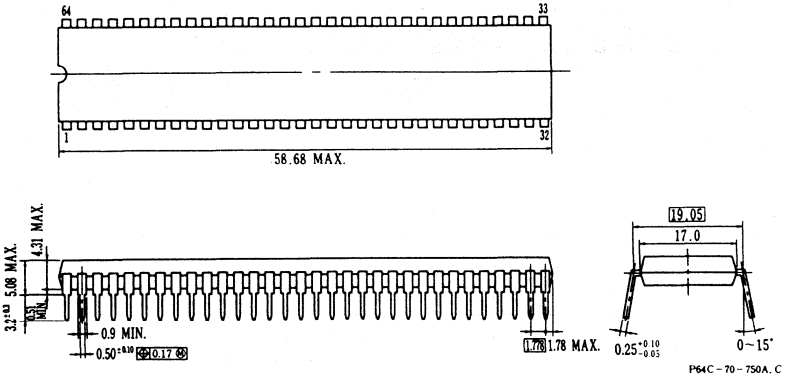
PROM Write Mode Timing



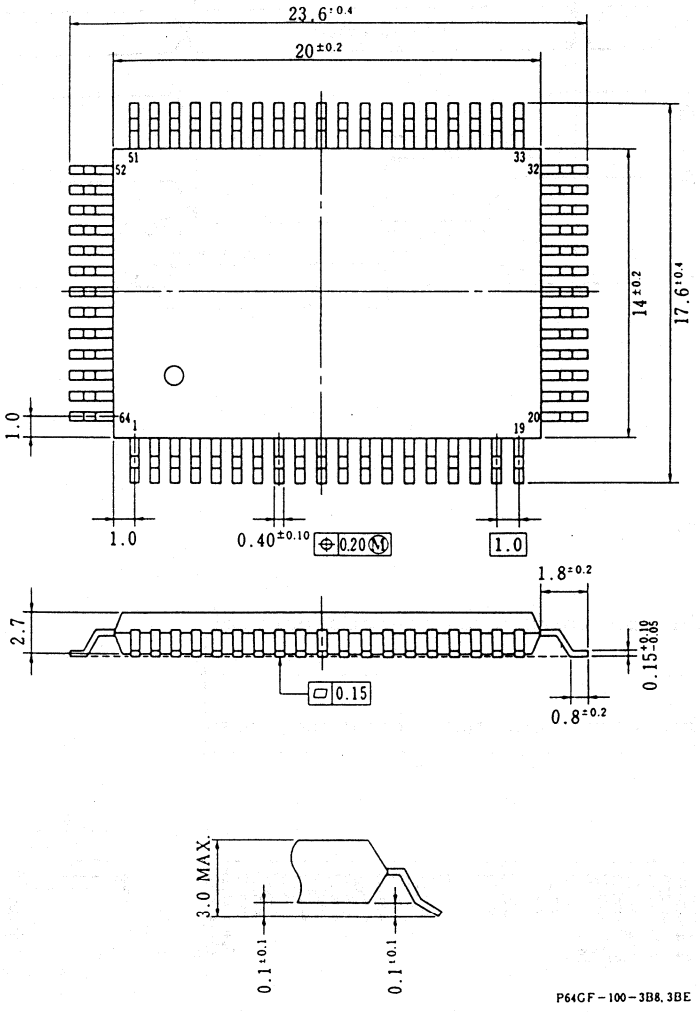
PROM Read Mode Timing



Package Dimensions
64-Pin Shrink DIP



Package Dimensions
64-Pin FLAT PACK



P64GF-100-3B8, 3BE

Description

The μPD78134 is an 8-bit single-chip microcomputer which incorporates a high-speed, high-performance 8-bit CPU and belongs to the μCOM-78K/I family. Because the μPD78134 also incorporates peripheral devices suitable for servo control by software, it is ideal for applications requiring digital servo control such as video tape recorders (VTRs). In addition to this servo control function, the microcomputer allows system control with a single chip and can thus faciliate miniaturization of the applied set. The μPD78134 is also available in a version whose on-chip mask ROM is replaced with a one-time PROM (OTPROM), which is intended for trial production of a system in system development and for production of various models in small quantities.

The μPD78134 is best suited for servo control applications as follows:
VTR : Video Tape Recorders
PPC : Plain Paper Copier
HDD: Hard Disc Drive
FDD : Floppy Disc Drive
DAT : Digital Audio Tape Recorder
CDP: Compact Disc Player

Features

- ☐ High-speed execution of Instructions realized by multiplexing internal buses: 0.33 μs (at 12 MHz CPU clock)
- ☐ Super timer unit ideal for servo control of VTR, etc. incorporated
  - – Speed and phase control for drum and capstan motor
  - – 2-channel head switch outputs for voice and image
  - – VSYNC (Vertical Synchronizing) signal detecting function
  - – Input pulse duty factor judging function
  - – 2-channel PWM output circuits which allow variable active level setting
- ☐ Built-in real-time output function (PORT0) capable of varying output patterns at any time intervals (ideal for VTR head switch output and step motor control)
- ☐ Powerful interrupt function selectable from these two types of interrupt handling:
  - – Vectored interrupt function
  - – Macro service function
- ☐ Built-in pull-up resistance function eliminating the need of any external resistor
- ☐ 80-pin plastic QFP

Ordering Information

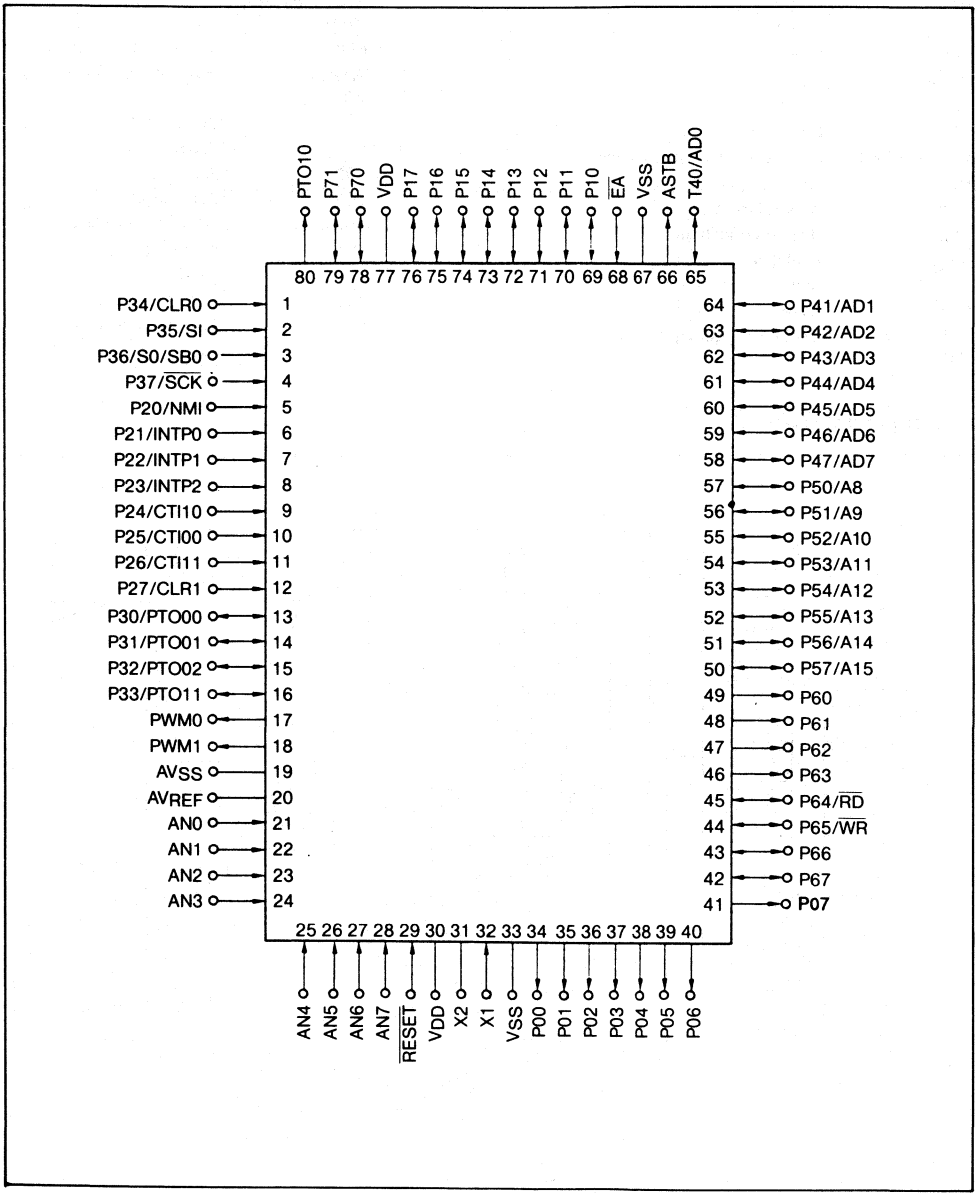
Product name	Package
μPD78134GF-XXX-3B9	80-pin plastic QFP
	16K OTPROM Version
μPD78P134GF	80-pin plastic QFP

2

Function Table

Item	Description
No. of basic instructions	63 instuctions
Minimum instruction execution time	0.33 μs (at 12 MHz CPU clock)
Memory expansion function	**Expandable up to 64K bytes**
General registers	8 bits x 8 registers x 4 banks (memory mapping)
Instruction set	● **16-bit Add, Subtract Compare** ● **Multiply and Divide (16 bits x 8 bits, 16 bits Add 8 bits)** ● Bit manipulation (Move, Boolean operation, Set, Reset, Test) ● BCD Adjust
I/O lines	66 lines in total Input ports: 12 Output ports: 12 I/O ports: 34 Analog input: 8
Super timer unit	● Timers: 16 bits x 3 units 7 bits x 1 unit ● Counters: 18 bits x 1 unit ● Capture registers: 18 bits x 1 unit 16 bits x 4 units 7 bits x 1 unit ● Compare registers: 16 bits x 6 units 7 bits x 1 unit ● PWM outputs: 12 bits x 2 units (Active level variable)
Real-time output port	● Port output function interlocked with timer ● 4 bits x 2 or 8 bits x 1
Serial interface	NEC format serial bus interface (SBI) or 3-wire system serial interface is selectable.
A/D converter	● 8-bit precision x 8 inputs ● Conversion time: 30μs per analog input (at 12 MHz)
Interrupts	● Interrupt sources: 17 sources (External: 5; Internal: 12) ● Method of handling selectable from Macro service function or Vectored interrupt function. ● Interrupt priority variable (2 levels)
Standby function	STOP Mode
Pull-up resistance	44 resistors incorporated (Enable/disable can be specified by software)

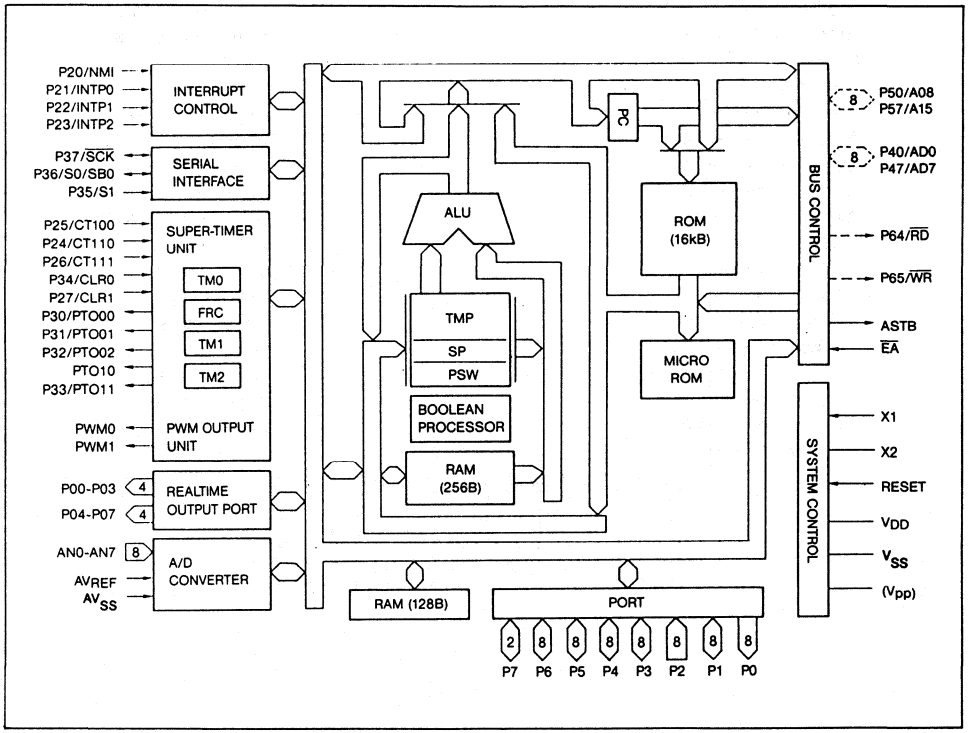
Pin Configuration
80-pin plastic QFP (Top View)



Pin Identification

P00 to P07	: Port 0
P10 to P17	: Port 1
P20 to P27	: Port 2
P30 to P37	: Port 3
P40 to P47	: Port 4
P50 to P57	: Port 5
P60 to P67	: Port 6
P70, P71	: Port 7
PWM0, PWM1	: Pulse Width Modulation Outputs
CL0	: Clock Output
AN0 to AN7	: Analog Inputs
AV_{REF}	: Reference Voltage
AV_{SS}	: Analog V_{SS}
X1, X2	: Crystal
$\overline{RESET}$	: Reset
CTI00, CTI10, CTI11	: Capture Trigger Inputs
CLR0, CLR1	: Timer Clear Inputs
PTO00 to PTO02, PTO10, PTO11	: Programmable Timer Inputs
NMI	: Nonmaskable Interrupt
INTP0 to INTP2	: Interrupts from Peripherals
SI	; Serial Input
SO	: Serial Output
$\overline{SB0}$	: Serial Bus
$\overline{SCK}$	: Serial Clock
AD0 to AD7	: Address/Data (Bus)
A8 to A15	: Address (Bus)
$\overline{RD}$	: Read
$\overline{WR}$	: Write
ASTB	: Address Strobe
$\overline{EA}$	: External Access

Block Diagram of μPD78134



Pin Functions

1. Ports

Pin name	Input/Output	Dual function pin	Function
P00-P07	Output	—	(Port 0) An 8-bit output port only, provided with an output latch. This Port can also be used as an 8-bit real-time output port or as two 4-bit real-time output ports.
P10-P17	Input/Output	—	(Port 1) An 8-bit input/output port with output latch. This port can be specified for input/output in bit units.
P20	Input	NMI	(Port 2) An 8-bit input-only port. P22 to P27 have software controlled pull-up resistors built in, P20 and P21 do not have.
P21		INTP0	
P22		INTP1	
P23		INTP2	
P24		CTI10	
P25		CTI00	
P26		CTI11	
P27		CLR1	
P30	Input/Output	PTO00	A 4-bit input/output port (3-state) with output latch.
P31		PTO01	
P32		PTO02	
P33		PTO11	
P34	—	CLR0	No port function, just signal I/O mode.
P35		SI	
P36	Input	SO/SB0	Can be specified for input/output.
P37		$\overline{SCK}$	
P40-P47	Input/Output	AD0-AD7	(Port 4) An 8-bit input/output port (3-state) with output latch. This port can be specified for input/output in 8-bit units.
P50-P57	Input/Output	A8-A15	(Port 5) An 8-bit input/output port (3-state) with output latch. This port can be specified for input or output in bit units.
P60	Output	—	A 4-bit output-only port.
P61			
P62			
P63			
P64	Input/Output	$\overline{RD}$	Can be specified for input/output port (3-state). They have Software controlled pull-up resistors built in.
P65		$\overline{WR}$	
P66		—	
P67			
P70	Input/Output	—	A 2-bit input/output port (3-state), with software-controlled pull-up resistor built in.
P71			

2. Other than Ports

Pin name	Input/Output	Dual function pin	Function
PTO00	Output	P30	Programmable timer outputs, from the Super timer unit.
PTO01	Output	P31	
PTO02	Output	P32	
PTO10	Output	—	
PTO11	Ouptut	P33	
CLR0	Input	—	Timer 0 clear input.
SI	Input	—	Serial data input.
SO/SB0	Input/Output	P36	Serial data output in 3-wire mode or serial bus input/output inSBI mode.
$\overline{SCK}$	Input/Output	P37	Serial clock input/output.
NMI	Input	P20	Non-maskable interrupt request input for which the rising or falling edge can be specified as the detection edge by the mode register.
INTP0	Input	P21	External interrupt request input pin for which the effective edge can be specified in the mode register.
INTP1-INTP2	Input	P22-P23	External interrupt request input pin for which the effective edge can be specified in the mode register. Pull-up resistors built in.
CTI00	Input	P25	Capture trigger input to capture contents of free-running counter into FRC capture register 2.
CTI10	Input	P24	Capture trigger input.
CTI11	Input	P26	Capture trigger input.
CLR1	Input	P27	Timer 1 clear input with digital noise eliminating circuit.
AD0-AD7	Input/Output	P40-P47	Time-division multiplexed address/data bus (when external memory is connected).
A08-A15	Ouptu	P50-P57	Address output port (when external memory is connected).
$\overline{RD}$	Output	P64	Strobe signal output pin for external memory read, if $\overline{EA}$ pin is set to 0 or extended Mode is specified inMM register.
$\overline{WR}$	Output	P65	Strobe signal output pin for external memory write, if $\overline{EA}$ pin is set to 0 or extended Mode is specified in MM register.
PWM0, PWM1	Output	—	Pulse width modulated output 0 and 1.
PTO10	Output	—	Timer 1 output pin.
AN0-AN7	Input	—	8-analog inputs to the A/D converter.
AV_{REF}	Input	—	Reference voltage input to the A/D converter.
AV_{SS}	Input	—	Ground input to the A/D converter.
$\overline{EA}$	Input	—	If this pin is activated the device works in a ROMless mode to access external memory instead of the on chip ROM.
ASTB/ CLO	Output	—	Address Strobe to latch address when accessing external memory or in single chip mode to output clock to other external circuits.
X1, X2	—	—	A crystal for the system clock is connected across these pins. External clock would be supplied to X1 and reverse phase to X2.
$\overline{RESET}$	Input	—	An active-Low level input to reset system.
V_{DD}		—	Positive power supply.
V_{SS}		—	GND.

I/O Circuits

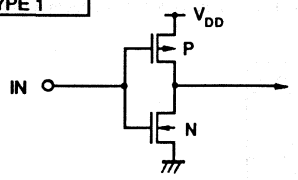
The types of I/O circuits of each pin are shown in following table and the different types of I/O circuits are shown afterwards.

Input/Output Circuit type of each pin:

Pin	I/O Circuit type	Pin	I/O circuit type
P00-P07	4	P35/SI	2-A
P10-P17	5-A	P36/SO/SB0	10-A
P20-NM1	2	P37/$\overline{SCK}$	8-A
P21/INTP0		P40-P47	5-A
P22/INTP12-A	2-A	P50-P57	5-A
P23/INTP2		P60-P63	3
P24/CTI10		P64-P67	5-A
P25/CTI00		P70-P71	5-A
P26/CTI11		PWM0, PWM1	3
P27/CLR1		PTO10	3
P30/PTO00	5-A	AN0-AN7	7
P31/PTO01		EA	1
P32/PTO02		ASTB/CLO	3
P33/PTO11		$\overline{RESET}$	2
P34/CLR0	2-A		

Pin I/O Circuits

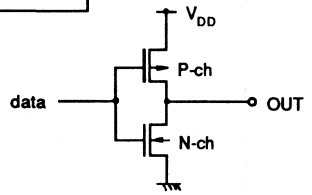
TYPE 1



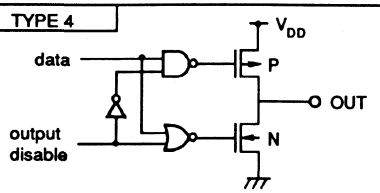
TYPE 2

Schmitt trigger input with hysteresis characteristics

TYPE 3

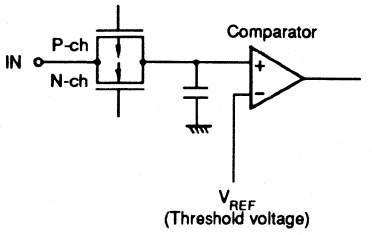


TYPE 4

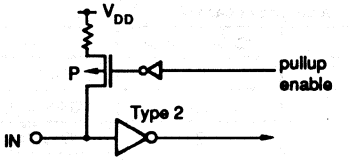


Push-pull output type which can put its output in High impedance state (which can turn off both P-ch and N-ch).

type 7

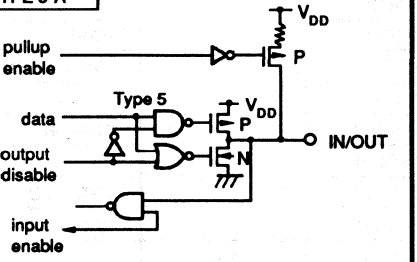


Type 2-A

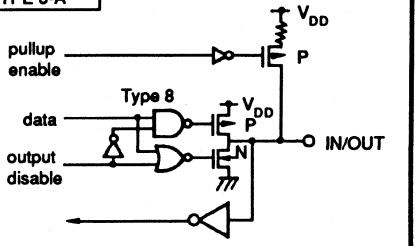


Schmitt trigger input with hysteresis characteristic

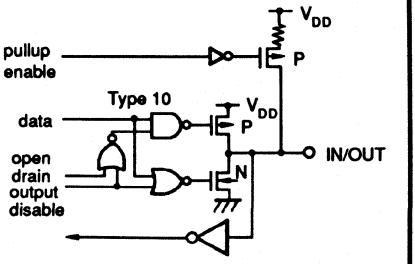
TYPE 5-A



TYPE 8-A



TYPE 10-A



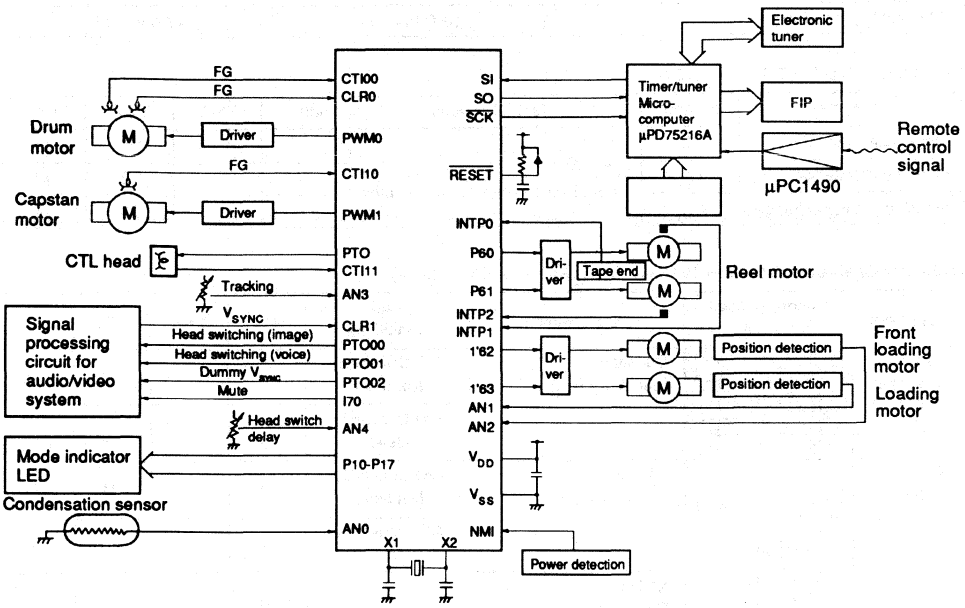
How connect Unused Pins

Pin	Recommended action
P00-P07	Leave the unused pinopen.
P10-P17	Input condition: Connect the unused pin to V_{DD} through pull-up resistor. Output condition: Leave the unused pinopen.
P20-P27	Connect the unused pin to V_{SS}.
P30-P33	Input condition: Connect the unused pin to V_{DD} through pull-up resistor. Output condition: Leave the unused pin open.
P34-P37	Connect the unused pin to V_{DD} or V_{SS}.
P40-P47	Input condition: Connect the unused pin to VDD through pull-up resistor. Output condition: Leave the unused pin open.
P50-P57	
P60-P67	
P70-P71	
PWM0, PWM1	Leave the unused pin open.
PTO10	Leave the unused pin open.
AN0-AN7	Connect the unused pin to V_{SS}.
AV_{REF}	Connect the unused pin to V_{SS}.
AV_{SS}	
ASTB/CLO	Leave the unused pin open.

Differences between μPD78134 and μPD78112

Item \ Product		μPD78134	μPD78112
Internal memories	ROM	16384 bytes	8192 bytes
	RAM	384 bytes	192 bytes
Memory expansion function		**Expandable externally up to 64K bytes.**	None
Interrupt	Source	External: 5 Internal: 12	External: 2 Internal: 8 Test input: 2
	Priority level	2 levels can be set independent of Default priority (by software control)	None (Default priority only)
	Macro service	● Counter mode ● Data transfer mode ● Real-time output port control mode ● Data pattern recognition mode	● Counter mode ● Data transfer mode ● Multiple Counter channel mode
Super timer unit	Timers & counter	● Timers: 16 bits x 3 7 bits x 1 ● Counter: 18 bits x 1	● Timers: 16 bits x 3 ● Counter: 16 bits x 1
	Registers	● Capture: 18 bits x 1 16 bits x 4 7 bits x 1 ● Comprare: 16 bits x 6 7 bits x 1	● Capture: 16 bits x 5 ● Compare: 16 bits x 6
	PWM	● 12 bits x 2 channels (Active level variable)	● 12 bits x 2 channels (Fixed to High Active)
Real-time output		4 bits x 2 or 8 bits x 1	None
Serial interface		3-wire system or SBI selectable	3-wire system only
I/O lines	I/O	● Inputs: 12 ● Outputs: 8 ● I/O: 38 ● Analog inputs: 8 66 lines in total	● Inputs: 12 ● Outputs: 6 ● I/O: 28 ● Analog inputs: 8 54 lines in total
	Pull-up resistance	44 resistors (by software control)	None
Package		80-pin plastic QFP	64-pin plastic shrink DIP or 64-pin plastic QFP

Example of System Configuration
(Stationary type VTR)



Absolute Maximum Ratings (ta=25°C)

Parameter	Symbol	Test Conditions	Ratings	Unit
Power voltage	V_{DD}		-0.5 to +7.0	V
	AV_{SS}		-0.5 to +0.5	V
A/D converter reference input voltage	AV_{REF}		-0.5 to V_{DD}	V
Input voltage	V_I		-0.5 to V_{DD} +0.5	V
Output voltage	V_O		-0.5 to V_{DD} +0.5	V
Low-level output current	I_{OL}	at 1 Pin	15	mA
		Total	100	mA
High-level output current	I_{OH}	at 1 Pin	-10	mA
		Total	-50	mA
Operating temperature	T_{opt}		-10 to +70	°C
Storage temperature	T_{stg}		-65 to +150	°C

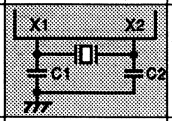
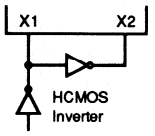
Operating Conditions

Oscillation Frequency	Ta	V_{DD}
4 MHz ≤ f_{XX} ≤ 12 MHz	-10°C to +70°C	+5.0 V ±10%

Capacitance (Ta=25°C, V_{DD}=V_{SS}=0V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1MHz 0V at all pins except the tested pins			20	pf
Output capacitance	C_O				20	pf
Input/output capacitance	C_{IO}				20	pf

Oscillator Characteristics (Ta=-10 to +70°C, V_{DD}=+5.0V ±10%, V_{SS}=0V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic Resonator or XTAL*1		Oscillation Frequency (f_{XX})	A/D Converter Not used	4		12	MHz
			A/D Converter Used	6		12	MHz
External Clock		X1 Input Frequency (f_X)	A/D Converter Not used	4		12	MHz
			A/D Converter Used	6		12	MHz
		X1 Input Rise, Fall Time (t_{XR}, t_{XF})		0		20	ns
		X1 Input High, Low Level Width (t_{WXH}, t_{WXL})		30		220	ns

*1: For XTAL, the following external capacitances are recommended:
C_1=C_2=15pf

Note:
(1) External oscillation circuit should be connected at the minimum distance from X1 and X2 pins.
(2) No other signal line should cross the area ▨

DC Characteristics

Ta=-10°C to +70°C, V_{DD}= +5.0V ±10%; V_{SS}=0V

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	Except Note1	2.2		V_{DD}	V
	V_{IH2}	Except Note1	$0.8V_{DD}$		V_{DD}	V
Output Low Voltage	V_{OL1}	I_{OL}=2.0mA Except Note2			0.45	V
	V_{OL2}	I_{OL}=8.0mA Except Note2			1.0	V
Output High Voltage	V_{OH1}	I_{OH}=-1.0mA Except Note3	V_{DD}-1.0			V
	V_{OH2}	I_{OH}=-100μA Except Note3	V_{DD}-0.5V			V
	V_{OH3}	I_{OH}=-5.0mA Except Note3	2.0			V
Input Leakage current	I_{LI}	$0V \le V_I \le V_{DD}$			±10	μA
Output Leakage current	I_{LO}	$0V \le V_O \le V_{DD}$			±10	μA
AV_{REF} current	AI_{REF}	Operation mode, f_{XX}=12MHz		1.5	5.0	mA
V_{DD} supply current	I_{DD1}	Operation mode, f_{XX}=12MHz		20	40	mA
	I_{DD2}	HALT mode, f_{XX}=12MHz		10	20	mA
Data retention voltage	V_{DDDR}	STOP mode	2.0		5.5	V
Data retention current	I_{DDDR}	STOP mode, V_{DDDR}=2.0V		1	8	μA
		STOP mode, V_{DDDR}=5V±10%		2	20	μA
Pull-up Resistance	R_L	V_I=0V	15	40	80	kΩ

Note1: X1,X2, $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2, P24/CTI10, P25/CTI00, P26/CTI11, P27/CLR1, P34/CLR0, P35/SI, P36/S0/SB0, P37/SCK, EA pins.

Note2: P10-P17

Note3: P00-P07

AC Characteristics (Ta = –10°C ~ +70°C, V_{DD} = +5.0V ± 10%, V_{SS} = 0V)
Memory Read/Write Operation:

Parameter	Symbol	Test Condition	Min	Max	Unit
X1 Input Cycle Time	tCYC		82	250	ns
Address Setup Time to ASTB ↓	tSAST		52		ns
Address Hold Time After ASTB ↓	tHSTA	R_L = 5kΩ, C_L = 50 pF	25		ns
Address to $\overline{RD}$ ↓ delay Time	tDAR		129		ns
Address Float To $\overline{RD}$ ↓ Time	tFAR		11		ns
Address to Data Input Time	tDAID			228	ns
ASTB ↓ to Data Input Time	tDSTID			181	ns
$\overline{RD}$ ↓ to Data Input Time	tDRID			99	ns
ASTB ↓ to $\overline{RD}$ ↓ delay Time	tDSTR		52		ns
Data Hold After $\overline{RD}$ ↑	tHRID		0		ns
$\overline{RD}$ ↑ to Address Active Time	tDRA		124		ns
$\overline{RD}$ ↑ to ASTB ↑ delay Time	tDRST		124		ns
$\overline{RD}$ Low Level Width	tWRL		124		ns
ASTB High Level Width	tWSTH		52		ns
Address to $\overline{WR}$ ↓ delay Time	tDAW		129		ns
ASTB ↓ to Data Output Time	tDSTOD			142	ns
$\overline{WR}$ ↓ to Data Output Time	tDWOD			60	ns
ASTB ↓ to $\overline{WR}$ ↓ delay Time	tDSTW		52		ns
Data Setup Time to $\overline{WR}$ ↑	tSODWR		146		ns
Data Hold Time After $\overline{WR}$ ↑	tHWOD	(2)	20		ns
$\overline{WR}$ ↑ to ASTB ↑ delay Time	tDWST		42		ns
$\overline{WR}$ Low Level Width	tWWL		196		ns

Note: (1) This Table show the value at f_{XX} = 12MHz and C_L = 100pF.

(2) C_L = 100 pF R_L = 2KΩ

Serial Operation:

Parameter	Symbol	Test Condition	Min	Max	Unit
$\overline{SCK}$ Cycle Time	tCYSK	External Clock Input	1.0		μs
		Internal 16 Devide Out.	1.3		μs
		Internal 64 Devide Out.	5.3		μs
$\overline{SCK}$ Low Level Width	tWSKL	External Clock Input	420		ns
		Internal 16 Devide Out.	556		ns
		Internal 64 Devide Out.	2.5		μs
$\overline{SCK}$ High Level Width	tWSKH	External Clock Input	420		ns
		Internal 16 Devide Out.	556		ns
		Internal 64 Devide Out.	2.5		μs
SI, SB0 Setup Time to $\overline{SCK}$ ↑	tSSSK		150		ns
SI, B0, Hold Time After $\overline{SCK}$ ↑	tHSSK		400		ns
SB0 Output Delay Time to $\overline{SCK}$ ↓	tDSBSK1	CMOS Push-pull Output	0	300	ns
	tDSBSK2	Open-drain Out.R_L = 1 KΩ	0	800	ns
$\overline{SCK}$ High Setup Time to SB0 ↓	tHSBSK		4		tCYX
$\overline{SCK}$ High Hold Time After SB0 ↓	tSSBSK		4		tCYX
SB0 Low Level Width	tWSBL		4		tCYX
SB0 High Level Width	tWSBH		4		tCYX

Note: This Table show the value at f_{XX} = 12Mhz and C_L = 100pF.

Clock Output Operation

Parameter	Symbol	Test Condition	Min	Max	Unit
CL0 Cycle Time	tCYCL		333	2667	ns
CL0 Low Level Width	tCLL	tCYCL/2±50	116	138	ns
CL0 High Level Width	tCLH	tCYCL/2±50	116	138	ns
CL0 Rise Time	tCLR			50	ns
CL0 Fall Time	tCLF			50	ns

Note: The above values are based on f_{XX} = 12MHz, CL = 100 pF.

Other Operations

Parameter		Symbol	Test Conditions	Min	Max	Unit
CTI00, CTI10, CTI11 Low Level Width		tWCTL		4		tCYX
CTI00, CTI10, CTI11 High Level Width		tWCTH		4		tCYX
CLR1 Low Level Width		tWCR1L	Without Noise Removal Circuit	4		tCYX
			With Noise Removal Circuit	48		tCYX
CLR1 High Level Width		tWCR1H	Without Noise Removal Circuit	4		tCYX
			With Noise Removal Circuit	48		tCYX
Vsync Separation circuit	Removal Pulse width	tWSEP			40	tCYX
	Pass-through pulse width			48		
NMI Low Level width		tWNIL		10		μs
NMI High Level width		tWNIH		10		μs
INTP0-INTP2 Low Level width		tWIPL		4		tCYX
INTP0-INTP2 High Level width		tWIPH		4		tCYX
$\overline{\text{RESET}}$ Low Level width		tWRSL		10		μs
$\overline{\text{RESET}}$ High Level width		tWRSH		10		μs

External Clock Timing

Parameter	Symbol	Test Conditions	Min	Max	Units
X1 Input Low Level Width	tWXL		30	130	ns
X1 Input High Level width	tWXH		30	130	ns
X1 Input Rise Time	tXR		0	30	ns
X1 Input Fall Time	tXF		0	30	ns
X1 Input Cycle Time	tCYX		82	250	ns

Definition of bus timing depending on cycle time tCYX: (Ta: −10°C to +70°C, V_{DD} = +5.0V ± 10%; V_{SS} = 0V)

Parameter	Symbol	Specification	Limit	10MHz	12MHz	Unit
X1 Input Cycle Time	tCYX		Min	100	82	ns
Address setup time to ASTB	tSAST	tCYX-30	Min	70	52	ns
Address to $\overline{RD}$ ↓ delay Time	tDAR	2tCYX-35	Min	165	129	ns
Address Float to $\overline{RD}$ ↓ Time	tFAR	tCYX/2-30	Min	20	11	ns
Address to Data Input Time	tDAID	(4+2n) tCYX-100	Max	300	228	ns
ASTB ↓ to Data Input Time	tDSTID	(3+2n) tCYX-65	Max	235	181	ns
$\overline{RD}$ ↓ to Data Input Time	tDRID	(2+2n) tCYX-65	Max	135	99	ns
ASTB ↓ delay Time	tDSTR	tCYX-30	Min	70	52	ns
$\overline{RD}$ ↑ to Address active Time	tDRA	2tCYX-40	Min	160	124	ns
$\overline{RD}$ ↑ to ALE ↑ delay Time	tDRST	2tCYX-40	Min	160	124	ns
$\overline{RD}$ low Level width	tWRL	(2+2n) tCYX-40	Min	160	124	ns
ASTB high level width	tWSTH	tCYX-30	Min	70	52	ns
Address to $\overline{WR}$ ↓ delay Time	tDAW	2tCYX-35	Min	165	129	ns
ASTB ↓ to Data Output Time	tDSTOD	tCYX+60	Max	160	142	ns
ASTB ↓ to $\overline{WR}$ ↓ delay Time	tDSTW	tCYX-30	Min	70	52	ns
Data setupt Time to $\overline{WR}$ ↑	tSODWR	(3+2n) tCYX-100	Min	200	146	ns
Data setup Time to $\overline{WR}$ ↓	tSODWF	tCYX-60	Min	40	22	ns
$\overline{WR}$ ↑ to ALE ↑ delay Time	tDWST	tCYX-40	Min	60	42	ns
$\overline{WR}$ Low Level width	tWWL	(3+2n) tCYX-50	Min	250	196	ns

Note 1: n means the number of wait cycles inserted by register designation

Note 2: values at 10/12MHz are at 0-wait

Note 3: The other spec parameters not listed above are independent of clock frequency.

AD Convertor Characteritics (Ta = −10°C ~ +70°C, V_{DD} = +5.0V ± 10%, 4V ≦ AV_{REF} ≦ V_{DD}, AV_{SS} = V_{SS} = 0V)

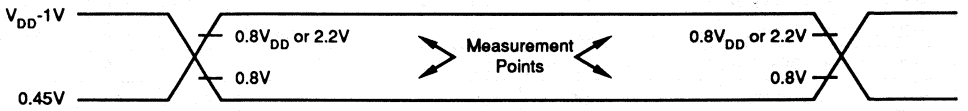
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution			8			bit
Absolute Accuracy		4.0V ≦ AV_{REF} ≦ V_{DD}			0.4	%
		3.4V ≦ AV_{REF} ≦ V_{DD}			0.8	%
Quantisation Tolerance					±½	LSB
Conversion Time	tCONV	83ns ≦ tCYX ≦ 125ns	360			tCYX
		125ns ≦ tCYX ≦ 250ns	240			tCYX
Sampling Time	tSAMP	83ns ≦ tCYX ≦ 125ns	72			tCYX
		125ns ≦ tCYX ≦ 250ns	48			tCYX
Analog Input Voltage	VIAN		0		AV_{REF}	V
Analog Input	RAN				1000	MΩ
Reference Voltage	AV_{REF}		3.4		V_{DD}	V
AV_{REF} Current	AI_{REF}	Operation Mode, f_{XX} = 12MHz		1.5	5.0	mA
		STOP MODE		0.7	1.5	mA

Memory Data Retention Characteristic
T_a=-10°C to +70°C

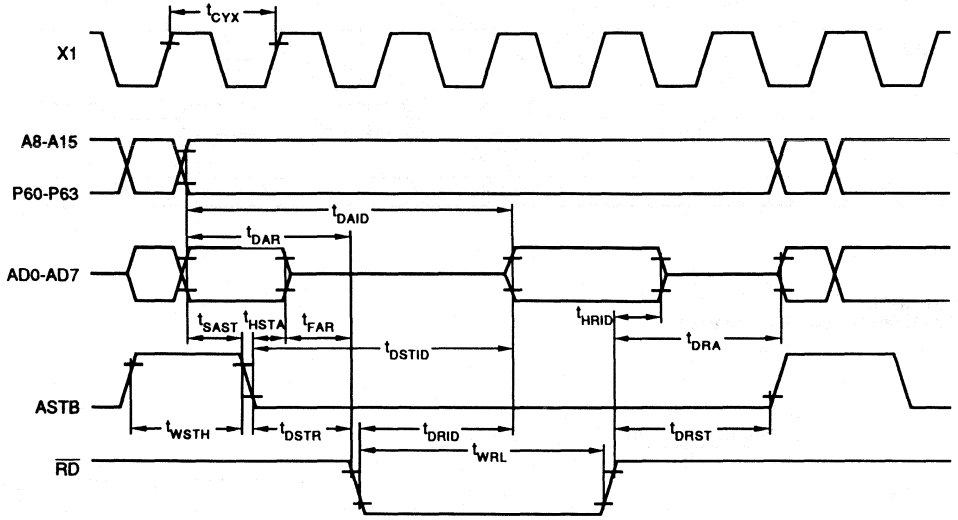
Parameter	Symbol	Test Condition	MIN.	TVP.	MAX.	Unit
Data retention Voltage	V_{DDDR}	STOP Mode	2.0		5.5	V
Data retention Current	I_{DDDR}	V_{DDDR}=2.0V		1	8	μA
		V_{DDDR}=5V±10%		2	20	μA
V_{DD} Rise Time	t_{RVD}		200			μs
V_{DD} Fall Time	t_{FVD}		200			μs
Set Release Signal Time	t_{DREL}		0			ms
Input Low Voltage	V_{IL}	Note Pins	0		$0.1V_{DD}$	V
Input High Voltage	V_{IH}	Note Pins	$0.9V_{DD}$		V_{DD}	V

Note: $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2, P24/CTI10, P25/CTI00, P26/CTI11, P27/CLR1, P34/CLR0, P35/SI, P36/SO/SB0, P37/SCK, $\overline{\text{EA}}$ pins

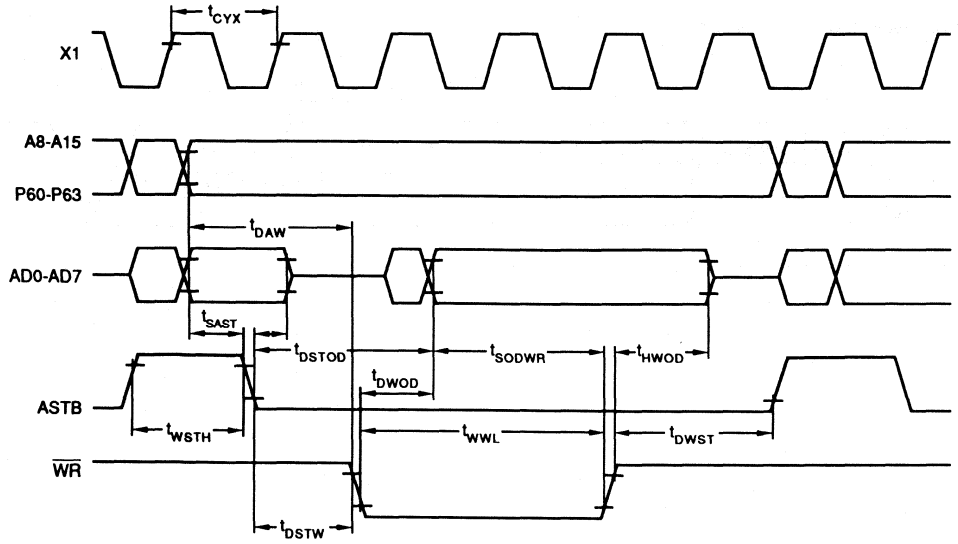
AC Timing Measurement Points



Timing Waveforms
Read Operation

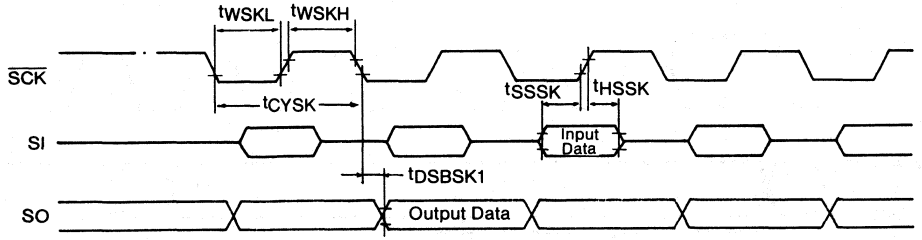


Write Operation



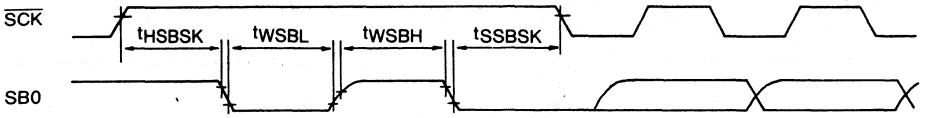
SERIAL OPERATION

3 Line Serial I/O Mode

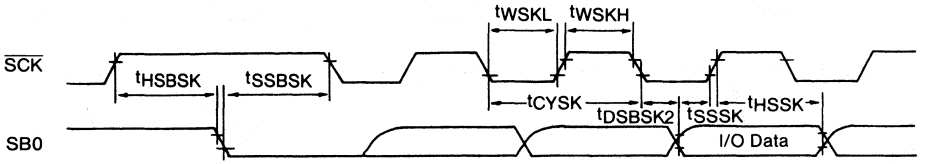


SBI MODE

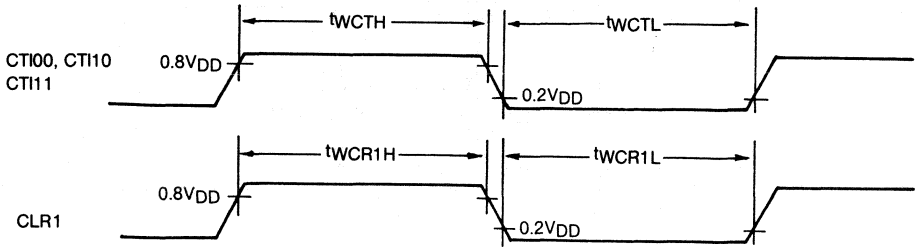
Bus Release Operation Transmit



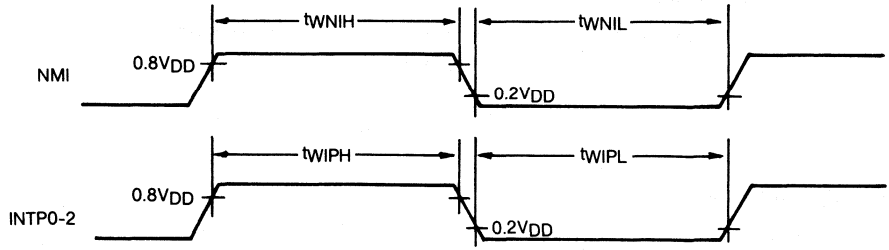
Command Operation Transmit



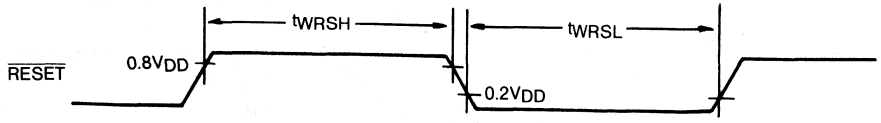
Super Timer Unit
Input Timing



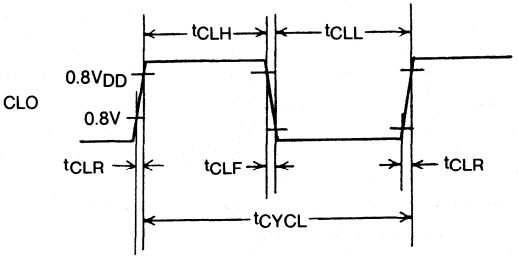
Interrupt Input Timing



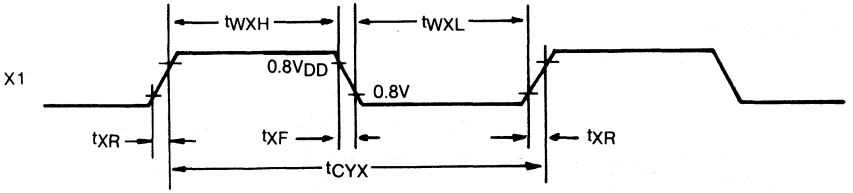
Reset Input Timing



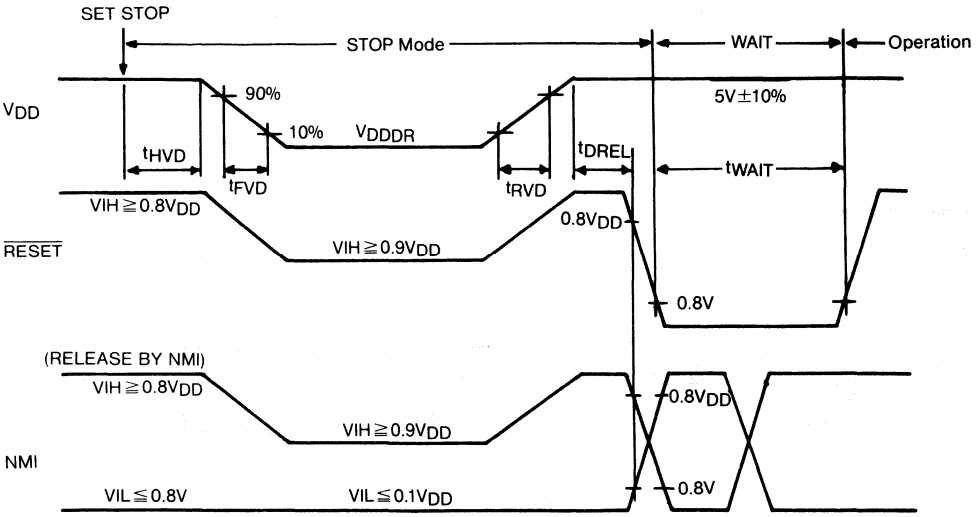
Clock Output Operation



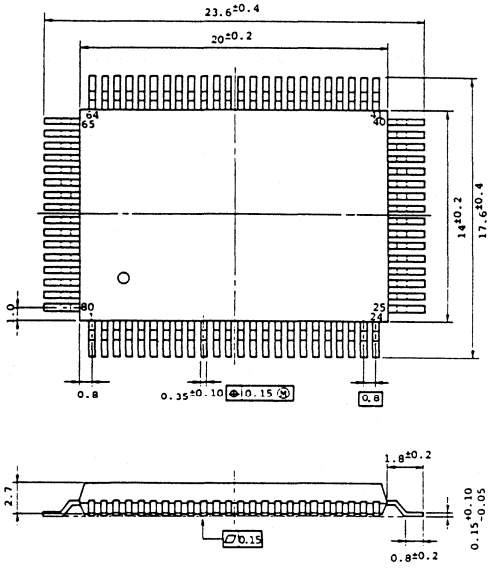
External Clock Timing



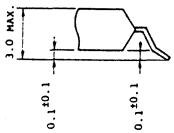
Data Retention Timing



Package Dimensions
80-pin plastic QFP (Units: mm)



Detailed drawing of pin end shape



P80GF-80-3B9

2

Description

The μPD78212, μPD78213 and μPD78214 are new members of the μCOM-78KII family, based on a high performance 8-bit CPU with up to 1MByte addressing space. The μPD78212/μPD78214 have 8-/16K bytes of on-chip mask ROM and 384-512 bytes of RAM, high-performance timers/counters, and A/D converter and two independent serial interfaces. The μPD78213 is the ROM less version with same features, just ROM on chip. For following applications these microcomputers are most suitable: Printers, typewriters, ECRs, electronic musical instruments, communication systems and cameras.

For system evaluation and small-scale production there are UVPROM Types available.

Features

- ☐ μCOM-78K/II family single-chip microcomputer
- ☐ High-speed instruction execution time realized by employing multiple internal buses
  - Instruction cycle: 330ns at 12MHz
- ☐ Instruction set suitable for control applications
  - Multiplication/division instructions (8-bit x 8-bit,) 16-bit ÷ 8-bit
  - 16-bit arithmetic instructions
  - Bit manipulation instructions
- ☐ A large amount of data can be handled using the 1M-byte data-memory expansion function
- ☐ Internal high-performance interrupt controller
  - Two levels of priority order (programmable)
  - Two different interrupt handling modes (vector interrupt function/macro service function)
- ☐ Multifunction timer/counter
  - 16-bit timer/counter: 1 channel
  - 8-bit timer/counter: 3 channel
- ☐ Powerful serial interface
  - UART: 1 channel with built in baud rate generator
  - Clock synchronized serial I/O (NEC standard serial bus): 1 channel
- ☐ Internal high precision A/D converter: 8 analog inputs
  - 8-bit precision, conversion time: 30μs (at 12 MHz)
- ☐ Real-time output port capable of controlling two stepping motors independently
- ☐ Standby functions (STOP/HALT)
- ☐ CMOS

Ordering Information

Part Number	Package Type	ROM
μPD78212CW-XXX	64-pin SDIP	8K Mask ROM
μPD78212GQ-XXX-36	64-pin QUIP	
μPD78212GC-XXX	64-pin QFP	
μPD78212GJ-XXX	74-pin QFP	
μPD78212L-XXX	68-pin PLCC	
μPD78213CW	64-pin SDIP	ROM-Less
μPD78213GQ-36	64-pin QUIP	
μPD78213GC	64-pin QFP	
μPD78213GJ	74-pin QFP	
μPD78213L	68-pin PLCC	
μPD78214CW	64-pin SDIP	16K Mask ROM
μPD78214GQ-XXX-36	64-pin QUIP	
μPD78214GC-XXX	64-pin QFP	
μPD78214GJ-XXX	74-pin QFP	
μPD78214L-XXX	68-pin PLCC	
μPD78P214DW	64-pin SDIP	16K UVPROM
μPD78P214CW	64-pin SDIP	16K OTPROM
μPD78P214GQ-36	64-pin QUIP	
μPD78P214GC	64-pin QFP	
μPD78P214GJ	74-pin QFP	
μPD78P214L	68-pin PLCC	

PLCC = plastic traded chip carrier
QUIP= Quad in line/Bent leads
SDIP = Shrink dual-in-line package
FLAT = Flat Pack (SMD)

2

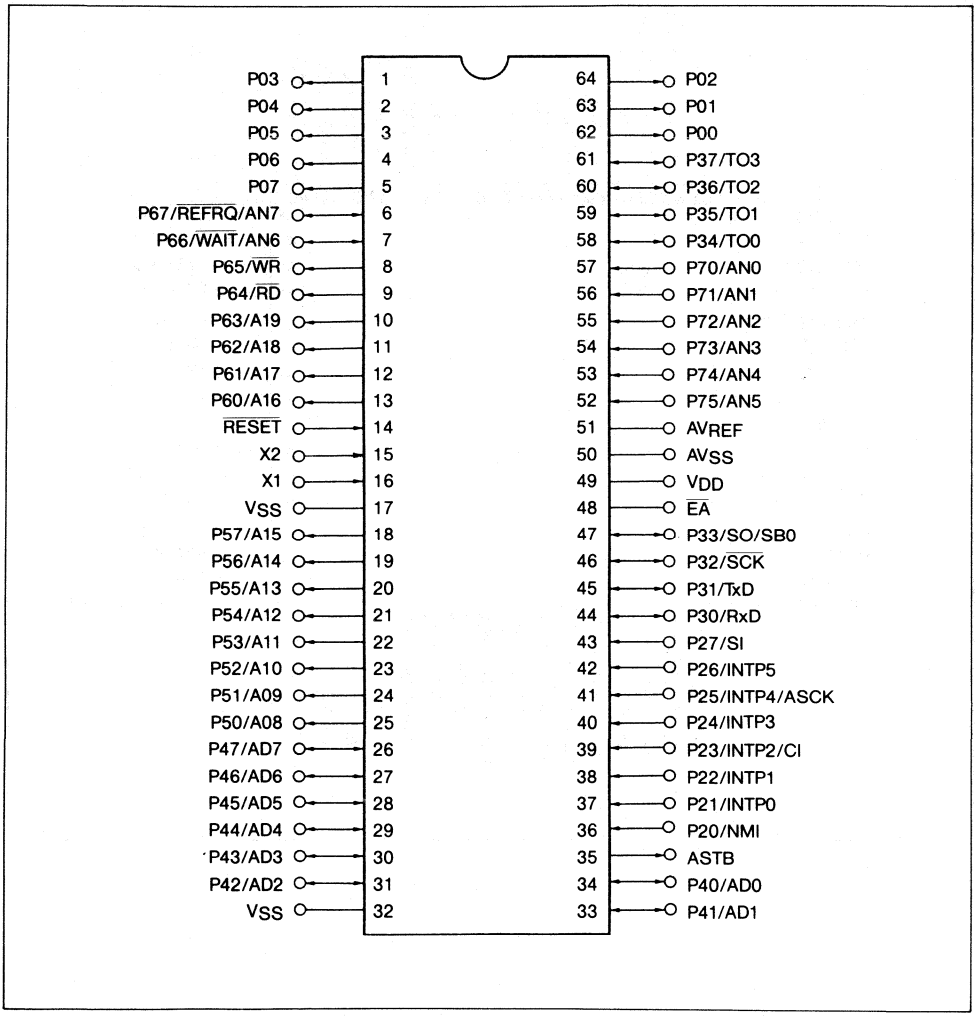
Functions Table

Function	Description	
Basic instructions (mnemonics)	65	
Minimum instruction execution time	333 ns (12 MHz operation)	
On-chip memory capacity	ROM: 8 kByte (78212), 16 kByte (78214) RAM: 384 (78212), 512 Byte (78213/214)	
Address space	1 Mbyte	
I/O pins	● Input port x 14 ● Output port x 12 ● I/O port x 28	On-chip pullup resistor (pullup specified by software): 34 inputs
General-purpose registers	8 bits x 8 x 4 bank (memory mapping)	
Timer/counter	● 16-bit timer/counter: Timer register x 1 Capture register x 1 Compare register x 2 ● 8-bit timer/counter 1: Timer register x 1 Capture/compare register x 1 Compare register x 1 ● 8-bit timer/counter 2: Timer register x 1 Capture register x 1 Compare register x 2 ● 8-bit timer/counter 3: Timer register x 1 Compare register x 1	
Serial interface	● UART: 1 channel (on-chip baud rate generator) ● Clock synchronous serial I/O: 1 channel	
Interrupts	● 19 sources (external 7, internal 12) + BRK instruction ● 2 levels of priority (programmable) ● 2 processing modes (vector interrupt, macro service)	
Instruction set	● 16-bit operation ● Multiplication and division (8 bits x 8 bits, 16 bits : 8 bits) ● Bit operation ● BCD correction, etc.	
A/D converter	8-bit precision x 8 channels	
Package	● 64-pin plastic shrink DIP (750 mil) ● 64-pin plastic QUIP ● 68-pin PLCC ● 64-pin plastic QFP (body 14 mm x 14 mm) (NOTE) ● 74-pin plastic QFP (body 20 mm x 20 mm)	

NOTE: Small 0.8 mm pin pitch package. Perfect for cameras, etc.

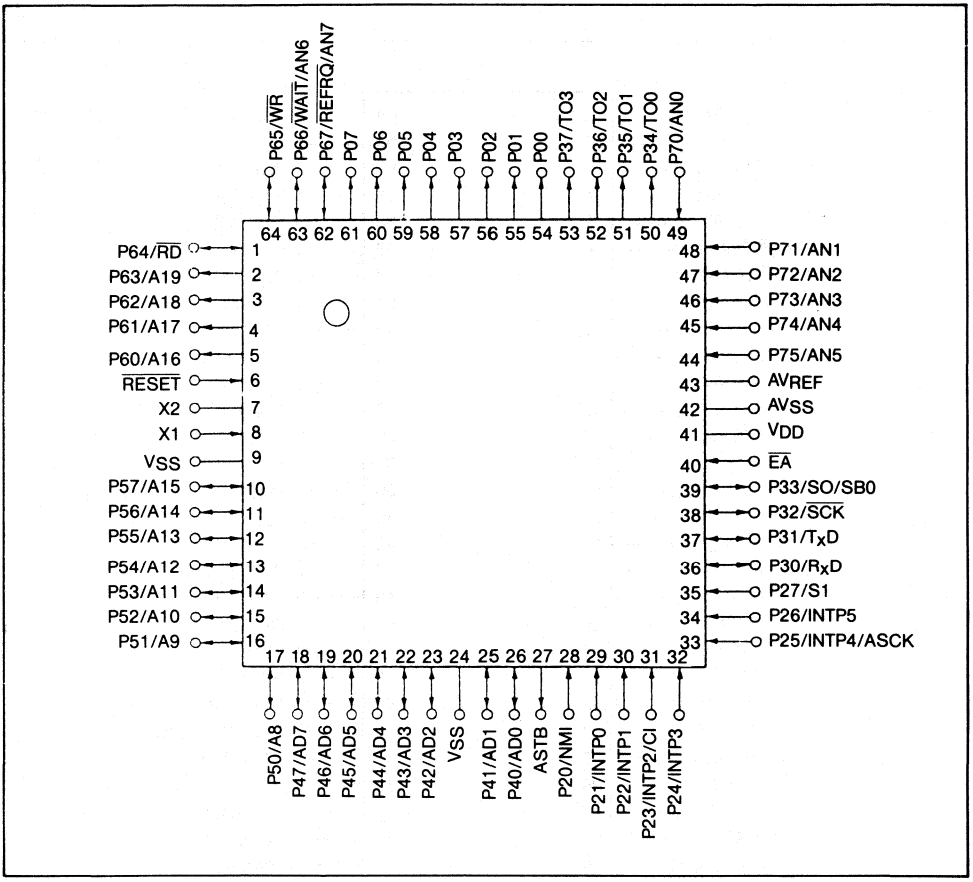
Pin Configuration

64-Pin SDIP/QUIP



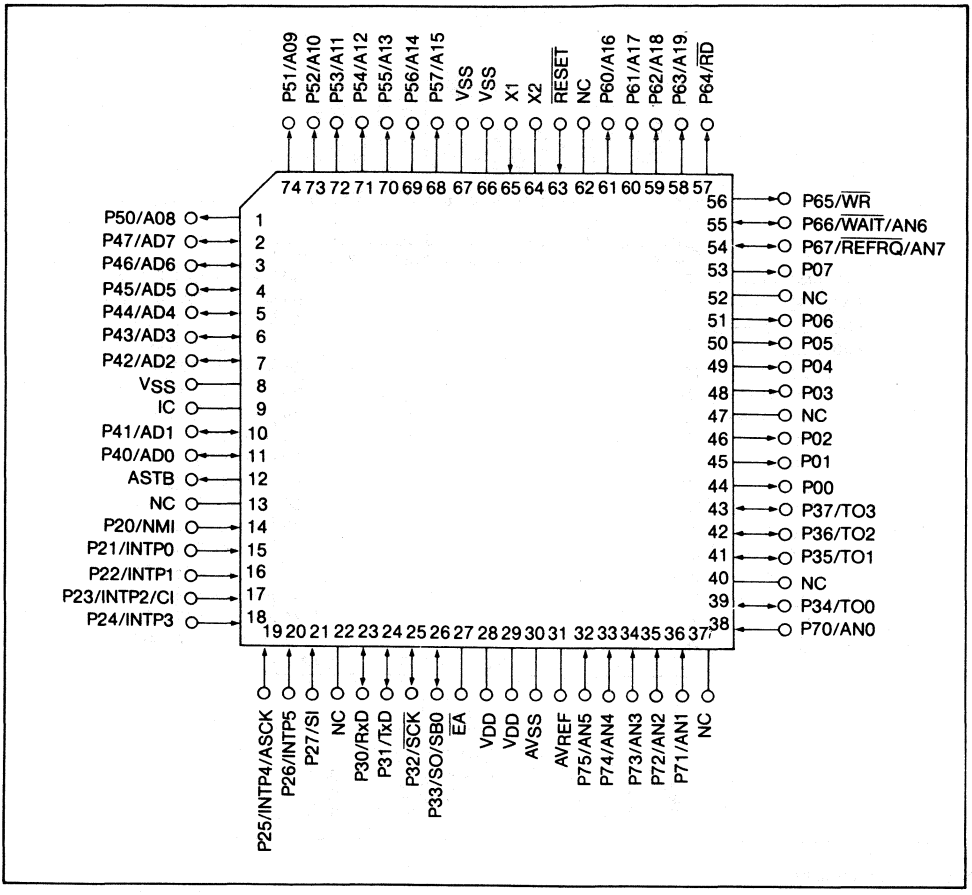
2

64-pin plastic QFP



Pin Configuration

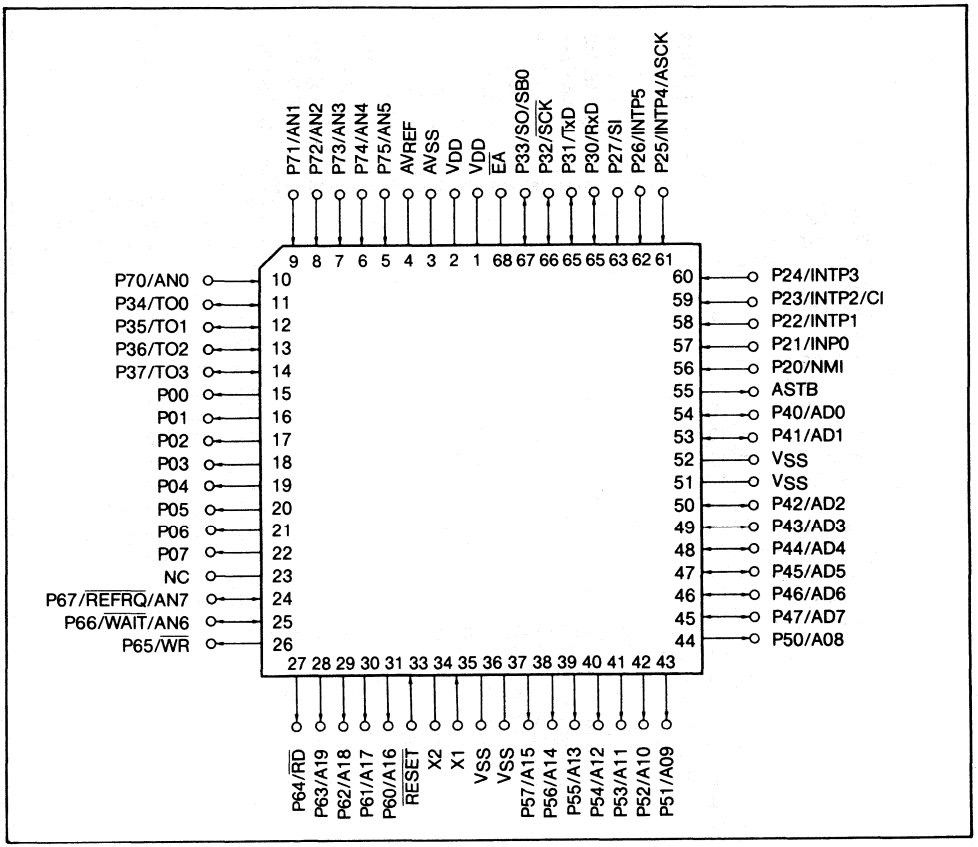
74-pin plastic QFP



*Note: IC Has to be connected to V_{SS}, NC is internally not connected

Pin Configuration

68-pin PLCC



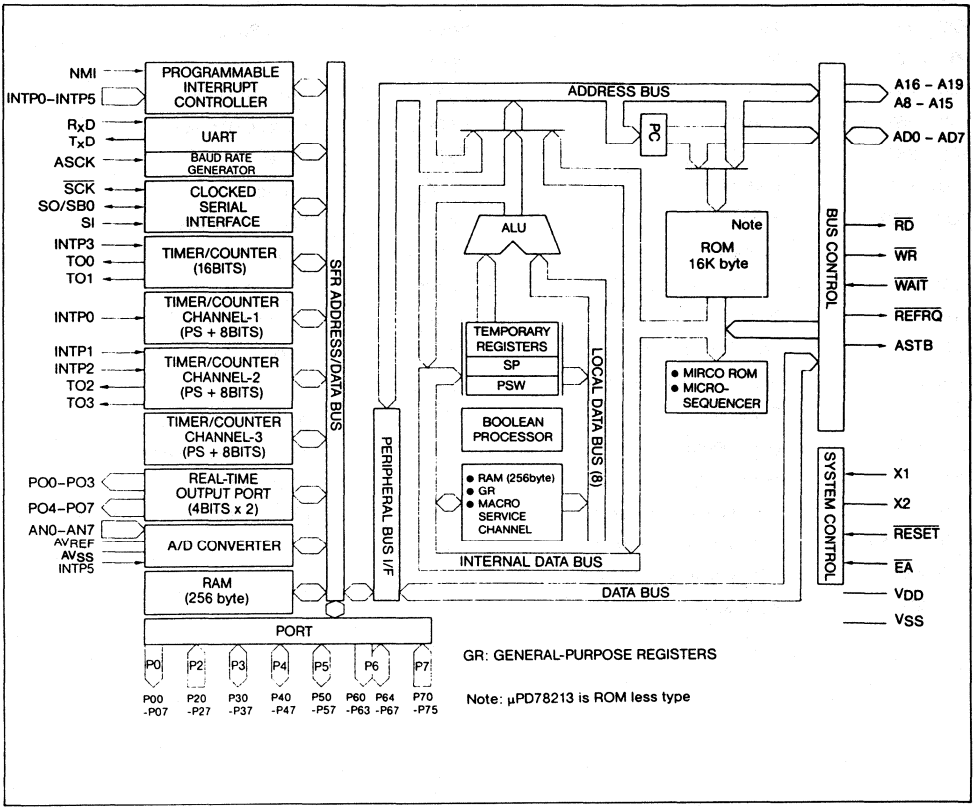
Note: NC is internally not connected

Pin Identification:

P00 – P07	:	Port 0	$\overline{RD}$	:	Read Strobe
P20 – P27	:	Port 2	$\overline{WR}$	:	Write Strobe
P30 – P37	:	Port 3	$\overline{WAIT}$	:	Wait
P40 – P47	:	Port 4	ASTB	:	Address Strobe
P50 – P57	:	Port 5	$\overline{REFRQ}$	:	Refresh Request
P60 – P67	:	Port 6	$\overline{RESET}$	:	Reset
P70 – P75	:	Port 7	X1, X2	:	Crystal
TO0 – TO3	:	Timer Output	$\overline{EA}$	:	External Access
CI	:	Clock Input	AN0 – AN7	:	Analog Input
R_XD	:	Receive Data	AV_{REF}	:	Reference Voltage
T_XD	:	Transmit Data	AV_{SS}	:	Analog Ground
$\overline{SCK}$	:	Serial Clock	V_{DD}	:	Power Supply
ASCK	:	Asynchronous Serial Clock	V_{SS}	:	Ground
SBO	:	Serial Bus	NC	:	Non-connection
SI	:	Serial Input	IC	:	Internally Connected
SO	:	Serial Output	$\overline{CE}$	:	Chip Enable
NMI	:	Non-maskable Interrupt	$\overline{OE}$	:	Output Enable
INTP0-INTP5	:	Interrupt From Peripherals	V_{PP}	:	Programming Power Supply
AD0 – AD7	:	Address/Data Bus			
A8 – A19	:	Address Bus			

2

Block Diagram



Pin Functions

1. Ports

Pin Name	Input/ Output	Dual Function Pin	Function
PO0 to PO7	Output tri-state	–	Port 0 (P0): Can be used as realtime output port (4 bits x 2).
P20	Input	NMI	Port 2 (P2): P20 cannot be used as a generalpurpose port. (Non maskable interrupt)
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK	
P26		INTP5	
P27		SI	
P30	Input/ output	RxD	Port 3 (P3): Input/output can be specified for each bit.
P31		TxD	
P32		$\overline{SCK}$	
P33		SO/SB0	
P34 to P37		TO0 to TO3	
P40 to P47	Input/ output	AD0 to AD7	Port 4(P4): Input/output can be specified for batch of 8 bits.
P50 to P57	Input/ output	A8 to A15	Port 5 (P5): Input/output can be specified for each bit.
P60 to P63	Output	A16 to A19	Port 6 (P6): Input/output can be specified for each bit of P64 to P67.
P64	Input/ output	$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$/AN6	
P67		$\overline{REFRQ}$/AN7	
P70 to P75	Input	AN0 to AN5	Port 7 (P7)

2

2. Other than Ports

Pin Name	Input/ Output	Dual Function Pin	Function
TO0 to TO3	Output	P34 to P37	Timer output
CI	Input	P23/INTP2	Count clock input to 8-bit timer/counter 2
RxD	Input	P30	Serial data input (UART)
TxD	Output	P31	Serial data output (UART)
ASCK	Input	P25/INTP4	Baud rate clock input (UART)
SB0	Input/Output	P33/SO	Serial data input/output (SBI)
SI	Input	P27	Serial data input (3-wire serial I/O)
SO	Output	P33/SB0	Serial data output (3-wire serial I/O)
$\overline{SCK}$	Input/Output	P32	Serial clock input/output (SBI, 3-wire serial I/O)
NMI	Input	P20	External interrupt request
INTP0		P21	
INTP1		P22	
INTP2		P23/CI	
INTP3		P24	
INTP4		P25/ASCK	
INTP5		P26	
AD0 to AD7	Input/Output	P40 to P47	Time division address/data bus (external memory connection)
A8 to A15	Output	P50 to P57	High-order address bus (external memory connection)
A16 to A19	Output	P60 to P63	High-order address at address expansion (external memory connection)
$\overline{RD}$	Output	P64	Read strobe to external memory
$\overline{WR}$	Output	P65	Write strobe to external memory
$\overline{WAIT}$	Input	P66	Wait insertion
ASTB	Output	–	Time division address (A0 to A7) latch timing output (at external memory access)
$\overline{REFRQ}$	Output	P67	Refresh pulse output to external pseudo-static memory
RESET	Input		Chip reset
X1	Input		System clock oscillation crystal connection (clock input also possible at X1)
X2	–		
$\overline{EA}$	Input		ROMLESS operation order (external access of same space as on-chip ROM)
AN0 to AN5	Input	P70 to P75	A/D converter analog voltage input
AN6, AN7		P66, P67	
AV_{REF}	–	–	A/D converter reference voltage impression
AV_{SS}			A/D converter GND
V_{DD}			Normal power supply
V_{SS}			GND
NC			Not internally connected (do not connect anything to this pin.)
IC			Internally connected (connect to V_{SS})

I/O Circuits

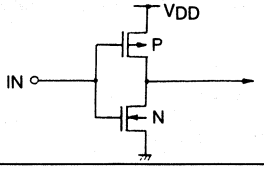
The type of I/O circuit of each pin and recommended connections for unused pins are shown in following table. The different types of I/O circuits are shown afterwards.

Input/Output type of each pin and what to do when not used:

Pin	I/O Type	Input/ Output	Recommended connection when not used
PO0 to PO7	4	Output	No connection required
P20/NMI	2	Input	Connect to V_{DD} with pull-up resistor
P21/INTP0			
P22/INTP1	2-A		
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK			
P26/INTP5			
P27/SI			
P30/RxD	5-A	Input/ output	Connect to V_{DD} or V_{SS}
P31/TxD			
P32/$\overline{SCK}$	8-A		Connect to V_{DD} through a resistor
P33/SO/SB0	10-A		
P34/TO0 to P37/TO3	5-A		Connect to V_{DD} or V_{SS}
P40/AD0 to P47/AD7			
P50/A8 to P57/A15			
P60/A16 to P63/A19	4	Output	No connection required
P64/$\overline{RD}$	5-A	Input/ output	Connect to V_{DD} or V_{SS}
P65/$\overline{WR}$			
P66/$\overline{WAIT}$/AN6	11	Input/ output	Connect to V_{DD} or V_{SS}
P67/$\overline{REFRQ}$/AN7			
P70/AN0 to P75/AN5	9	Input	
ASTB	4	Output	No connection required
$\overline{RESET}$	2	Input	-
$\overline{EA}$	1		
AV_{REF}	-		Connect to V_{SS}
AV_{SS}			
X1			-
X2			No connection required
NC			
IC			Connected to V_{SS}

Pin I/O Circuits

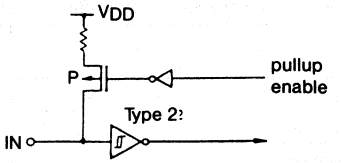
Type 1



Type 2

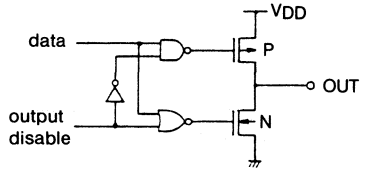
Schmitt trigger input with hysteresis characteristic

Type 2-A



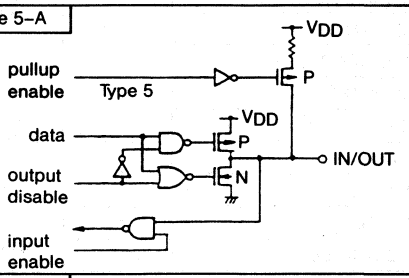
Schmitt trigger input with hysteresis characteristic

Type 4

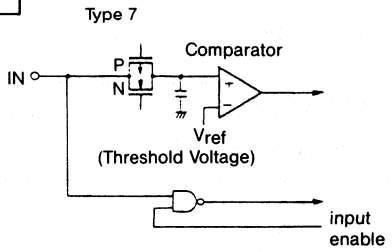


Pushpull output which can make the output high impedance (Both P-ch and N-ch off)

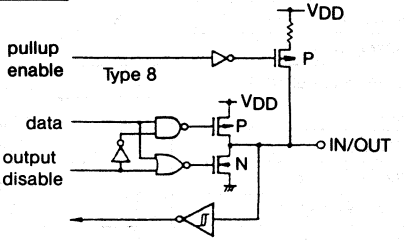
Type 5-A



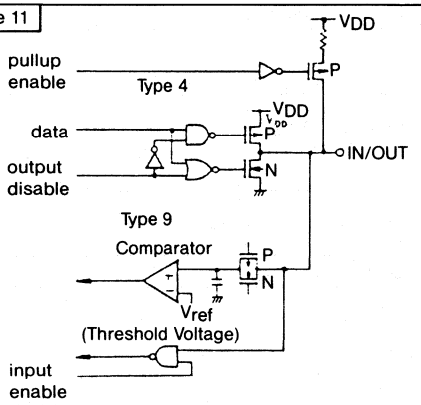
Type 9



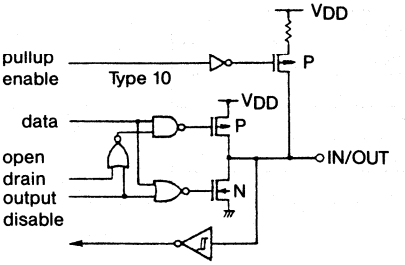
Type 8-A



Type 11



Type 10-A



Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Condition	Ratings	Unit
Power Supply Voltage	V_{DD}		− 0.5 ~ +7.0	V
	AV_{REF}		− 0.5 ~ V_{DD}	V
	AV_{SS}		− 0.5 ~ +0.5	V
Input Voltage	V_{I1}	note1 Pins	− 0.5 ~ V_{DD}+0.5	V
	V_{I2}	except note1 Pins	− 0.5 ~ AV_{REF}+0.5	V
Output Voltage	V_O		− 0.5 ~ V_{DD}+0.5	V
Low Level Output Current	I_{OL}	One Output Pin	15	mA
		All Output Pins	100	mA
High Level Output Current	I_{OH}	One Output Pin	− 10	mA
		All Output Pin	− 50	mA
Operating Temperature	T_{OPT}		− 40 ~ +85	°C
Storage Temperature	T_{STG}		− 65 ~ +150	°C

Note1: P70/AN0 − P75/AN5, P66/$\overline{WAIT}$/AN6, P67/$\overline{REFRQ}$/AN7

Recommended Operating Conditions

Clock Frequency	Operating Temperature (Ta)	Operating Voltage (V_{DD})
4MHz ≦ fxx ≦ 12 MHz	− 40 °C ~ +85 °C	+ 5.0 V ± 10%

Capacitance (Ta = 25°C, V_{DD} = V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min.	Typ	Max	Unit
Input Capacitance	C_I	fc = 1MHz Unmeasured Pins Returned to 0V			20	pF
Output Capacitance	C_O				20	pF
In/Output Capacitance	C_{IO}				20	pF

DC Characteristics (Ta = - 40°C ~ +85°C, V_{DD} = + 5.0V ± 10%, V_{SS} = OV)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	except note1 and note2	2.2		V_{DD}	V
	V_{IH2}	note1 Pins	2.2		AV_{REF}	V
	V_{IH3}	note2 Pins	$0.8V_{DD}$		V_{DD}	V
Output Low Voltage	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
	V_{OL2}	I_{OL} = 8.0 mA note3 Pins			1.0	V
Output High Voltage	V_{OH1}	I_{OH} = - 1.0 mA	V_{DD} -1.0			V
	V_{OH2}	I_{OH} = - 100μA	V_{DD} -0.5			V
	V_{OH3}	I_{OH} = - 5.0 mA note 4 Pins	2.0			V
Input Leak. Current	I_{LI}	$OV \leqq V_I \leqq V_{DD}$			±10	μA
Output Leak. Current	I_{LO}	$OV \leqq V_O \leqq V_{DD}$			±10	μA
AV_{REF} Current	AI_{REF}	Operation Mode f_{XX} = 12 MHz		1.5	5	μA
V_{DD} Supply Current	I_{DD1}	Operation Mode f_{XX} = 12 MHz		20	40	mA
	I_{DD2}	HALT Mode f_{XX} = 12 MHz		7	20	mA
Data Retention Voltage	V_{DDDR}	STOP Mode	2.5		5.5	V
Data Retention Current	I_{DDR}	STOP MODE V_{DDDR} = 2.5 V		2	20	μA
		STOP MODE V_{DDDR} = 5V ± 10%		5	50	μA
Pull-up Resistance	R_L	V_I=OV	15	40	80	kΩ

Note1: X1, X2 $\overline{\text{RESET}}$, P20/NMI, P21/INTPO, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{\text{SCK}}$, P33/SB0, and $\overline{\text{EA}}$ Pins

Note2: P70/AN0-P75/AN5, P66/WAIT/AN6, P67/REFRQ/AN7

Note3: P40/AD0 - P47/AD7, P50/A08 - P57/A15

Note4: P00 - P07

AC Characteristics ($T_a = -40°C \sim +85°C$, $V_{DD} = +5.0V \pm 10\%$, $V_{SS} = 0V$)
Memory Read/Write Operation:

Parameter	Symbol	Test Condition	Min	Max	Unit
X1 Input Cycle Time	t_{CYX}		82	250	ns
Address Setup Time to ASTB ↓	t_{SAST}		52		ns
Address Hold Time After ASTB ↓	t_{HSTA}	R_L=5kΩ, C_L=50pF	25		ns
Address to $\overline{RD}$ ↓ delay Time	t_{DAR}		129		ns
Address Float To $\overline{RD}$ ↓ Time	t_{FAR}		11		ns
Address to Data Input Time	t_{DAID}			228	ns
ASTB ↓ to Data Input Time	t_{DSTID}			181	ns
$\overline{RD}$ ↓ to Data Input Time	t_{DRID}			99	ns
ASTB ↓ to $\overline{RD}$ ↓ delay Time	t_{DSTR}		52		ns
Data Hold After $\overline{RD}$ ↑	t_{HRID}		0		ns
$\overline{RD}$ ↑ to Address Active Time	t_{DRA}		124		ns
$\overline{RD}$ ↑ to ASTB ↑ delay Time	t_{DRST}		124		ns
$\overline{RD}$ Low Level Width	t_{WRL}		124		ns
ASTB High Level Width	t_{WSTH}		52		ns
Address to $\overline{WR}$ ↓ delay Time	t_{DAW}		129		ns
ASTB ↓ to Data Output Time	t_{DSTOD}			142	ns
$\overline{WR}$ ↓ to Data Output Time	t_{DWOD}			60	ns
ASTB ↓ to $\overline{WR}$ ↓ delay Time	t_{DSTW1}		52		ns
	t_{DSTW2}	Refresh Mode	129		ns
Data Setup Time to $\overline{WR}$ ↑	t_{SODWR}		146		ns
Data Setup Time to $\overline{WR}$ ↓	t_{SODWF}	Refresh Mode	22		ns
Data Hold Time After $\overline{WR}$ ↑	t_{HWOD}	(2)	20		ns
$\overline{WR}$ ↑ to ASTB ↑ delay Time	t_{DWST}		42		ns
$\overline{WR}$ Low Level Width	t_{WWL1}		196		ns
	t_{WWL2}	Refresh Mode	114		ns
Address to $\overline{WAIT}$ ↓ Input Time	t_{DAWT}			146	ns
ASTB ↓ to $\overline{WAIT}$ ↓ Input Time	t_{DSTWT}			84	ns
X1 Low Setup Time to $\overline{WAIT}$ ↑	t_{SWTX}		0		ns
X1 Low Hold Time to $\overline{WAIT}$ ↑	t_{HWTX}		0		ns

Note: (1) This Table show the value at f_{XX} = 12MHz and C_L = 100pF.

(2) C_L = 100 pF R_L = 2KΩ

Serial Operation:

Parameter	Symbol	Test Condition	Min	Max	Unit
$\overline{SCK}$ Cycle Time	tCYSK	External Clock Input	1.0		μs
		Internal 16 Devide Out.	1.3		μs
		Internal 64 Devide Out.	5.3		μs
$\overline{SCK}$ Low Level Width	tWSKL	External Clock Input	420		ns
		Internal 16 Devide Out.	556		ns
		Internal 64 Devide Out.	2.5		μs
$\overline{SCK}$ High Level Width	tWSKH	External Clock Input	420		ns
		Internal 16 Devide Out.	556		ns
		Internal 64 Devide Out.	2.5		μs
SI, SB0 Setup Time to $\overline{SCK}$ ↑	tSSSK		150		ns
SI, B0, Hold Time After $\overline{SCK}$ ↑	tHSSK		400		ns
SB0 Output Delay Time to $\overline{SCK}$ ↓	tDSBSK1	CMOS Push-pull Output	0	300	ns
	tDSBSK2	Open-drain Out.R_L = 1 KΩ	0	800	ns
$\overline{SCK}$ High Setup Time to SB0 ↓	tHSBSK	SBI mode	4		tCYX
$\overline{SCK}$ High Hold Time After SB0 ↓	tSSBSK		4		tCYX
SB0 Low Level Width	tWSBL		4		tCYX
SB0 High Level Width	tWSBH		4		tCYX

Note: This Table show the value at f_{XX} = 12MHz and C_L = 100pF.

Other Operation:

Parameter	Symbol	Test Condition	Min	Max	Unit
NMI Low Level Width	tWNIL		10		μs
NMI High Level Width	tWNIH		10		μs
INTP0-INTP5 Low Level Width	tWITL		24		tCYX
INTP0-INTP5 High Level Width	tWITH		24		tCYX
$\overline{RESET}$ Low Level Width	tWRSL		10		μs
$\overline{RESET}$ High Level Width	tWRSH		10		μs

External Clock Timing:

Parameter	Symbol	Test Condition	Min	Max	Unit
X1 Input Low Level Width	t_{WXL}		30	130	ns
X1 Input High Level Width	t_{WXH}		30	130	ns
X1 Input Rise Time	t_{XR}		0	30	ns
X1 Input Fall Time	t_{XF}		0	30	ns
X1 Input Cycle Time	t_{CYX}		82	250	ns

AD Convertor Characteritics ($Ta = -40°C \sim +85°C$, $V_{DD} = +5.0V \pm 10\%$, $4V \leqq AV_{REF} \leqq V_{DD}$, $AV_{SS} = V_{SS} = 0V$)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution			8			bit
Absolute Accuracy					0.8%±½	LSB
		Ta=-10°C~+70°C 3.4V ≤AV_{REF}≤V_{DD}			0.8%±½	LSB
		Ta = -10°C ~ +70°C			0.4%±½	LSB
Conversion Time	t_{CONV}	83ns ≦ t_{CYX} ≦ 125ns	360			t_{CYX}
		125ns ≦ t_{CYX} ≦ 250ns	240			t_{CYX}
Sampring Time	t_{SAMP}	83ns ≦ t_{CYX} ≦ 125ns	72			t_{CYX}
		125ns ≦ t_{CYX} ≦250ns	48			t_{CYX}
Analog Input Voltage	V_{IAN}		0		AV_{REF}	V
Analog Input	R_{AN}			1000		MΩ
Reference Voltage	AV_{REF}		3.4		V_{DD}	V
AV_{REF} Current	AI_{REF}	Operation Mode, $f_{XX} = 12MHz$		1.5	5.0	mA
		STOP MODE		0.2	1.5	mA

Other operation

Parameter	Symbol	Conditions	Min	Max	Units
NMI low level width	t_{WNIL}		10		μs
NMI high level width	t_{WNIH}		10		μs
INTP0-INTP5 low level width	t_{WITL}		24		t_{CYX}
INTP0-INTP5 high level width	t_{WITH}		24		t_{CYX}
$\overline{RESET}$ low level width	t_{WRSL}		10		μs
$\overline{RESET}$ high level width	t_{WRSH}		10		μs

Definition of bus timing depending on cycle time t_{CYX} TA = -40°C ~ +85°C, V_{DD} = +5.0V ±10%, V_{SS} = 0V

Parameter	Symbol	Specification	Limit	12MHz	Unit
X1 Input Cycle Time	t_{CYX}		Min	82	ns
Address Setup Time to ASTB ↓	t_{SAST}	t_{CYX}-30	Min	52	ns
Address to $\overline{RD}$ ↓ delay Time	t_{DAR}	2t_{CYX}-35	Min	129	ns
Address Float to $\overline{RD}$ ↓ Time	t_{FAR}	t_{CYX}/2-30	Min	11	ns
Adress to Data Input Time	t_{DAID}	(4+2n) t_{CYX}-100	Max	228	ns
ASTB ↓ to Data Input Time	t_{DSTID}	(3+2n) t_{CYX}-65	Max	181	ns
$\overline{RD}$↓ to Data Input Time	t_{DRID}	(2+2n) t_{CYX}-65	Max	99	ns
ASTB ↓ to $\overline{RD}$ ↓ delay Time	t_{DSTR}	t_{CYX}-30	Min	52	ns
$\overline{RD}$ ↑ to Address Active Time	t_{DRA}	2t_{CYX}-40	Min	124	ns
$\overline{RD}$ ↑ to ASTB ↑ delay Time	t_{DRST}	2t_{CYX}-40	Min	124	ns
$\overline{RD}$ Low Level Width	t_{WRL}	(2+2n) t_{CYX}-40	Min	124	ns
ASTB High Level Width	t_{WSTH}	t_{CYX}-30	Min	52	ns
Address to $\overline{WR}$ ↓ delay Time	t_{DAW}	2t_{CYX}-35	Min	129	ns
ASTB ↓ to Data Output Time	t_{DSTOD}	t_{CYX}+60	Max	142	ns
ASTB ↓ to $\overline{WR}$ ↓ delay Time	t_{DSTW1}	t_{CYX}-30	Min	52	ns
	t_{DSTW2}	2t_{CYX}-35 Refresh Mode	Min	129	ns
Data Setup Time to$\overline{WR}$ ↑	t_{SODWR}	(3+2n)t_{CYX}-100	Min	146	ns
Data Setup Time to $\overline{WR}$ ↓	t_{SODWF}	t_{CYX}-60 Refresh Mode	Min	22	ns
$\overline{WR}$↑ to ASTB ↑ delay Time	t_{DWST}	t_{CYX}-40	Min	42	ns
$\overline{WR}$ Low Level Width	t_{WWL1}	(3+2n) t_{CYX}-50	Min	196	ns
Refresh Mode	t_{WWL2}	(2+2n) t_{CYX}-50 (Refresh Mode)	Min	114	ns
Address to $\overline{WAIT}$ ↓ Input Time	t_{DAWT}	3t_{CYX}-100	Max	146	ns
ASTB ↓ Input time	t_{DSTWT}	2t_{CYX}-80	Max	84	ns

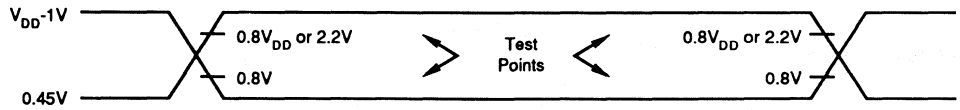
Note: n means number of wait Cycles

Memory Data Retention Characteristic (Ta = –40°C to +85°C)

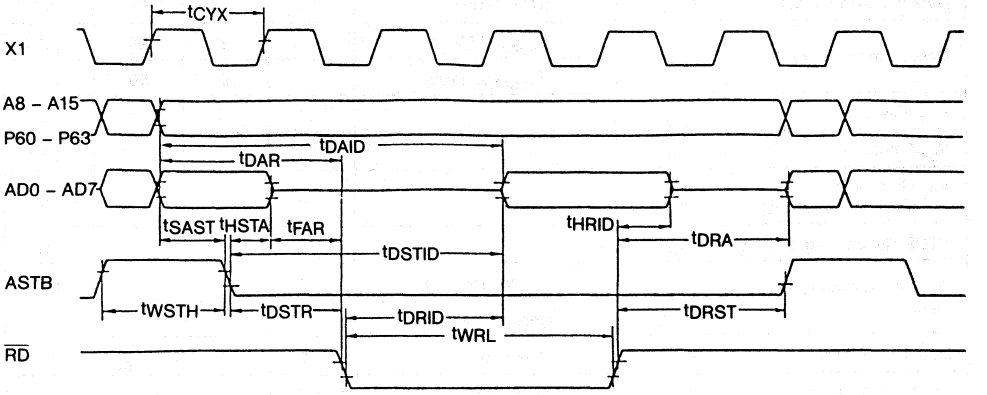
Parameter	Symbol	Test Condition	MIN.	TVP.	MAX.	Unit
Data retention Voltage	V_{DDDR}	STOP Mode	2.5		5.5	V
Data retention Current	I_{DDDR}	V_{DDDR}=2.5V		2	20	μA
		V_{DDDR}=5V±10%		5	50	μA
V_{DD} Rise Time	t_{RVD}		200			μs
V_{DD} Fall Time	t_{FVD}		200			μs
V_{DD} Hold Time (for STOP mode setting)	t_{HVD}		0			ms
STOP Release Signal Time	t_{DREL}		0			ms
Oscillation Stabilize Wait Time	t_{wait}	Crystal Oscillator	30			ms
		Ceramic Oscillator	5			ms
Input Low Voltage	V_{IL}	Note Pins	0		$0.1V_{DDDR}$	V
Input High Voltage	V_{IH}	Note Pins	$0.9V_{DDDR}$		V_{DDDR}	V

Note: $\overline{RESET}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{SCK}$, P33/SO/SB0, and $\overline{EA}$ Pins

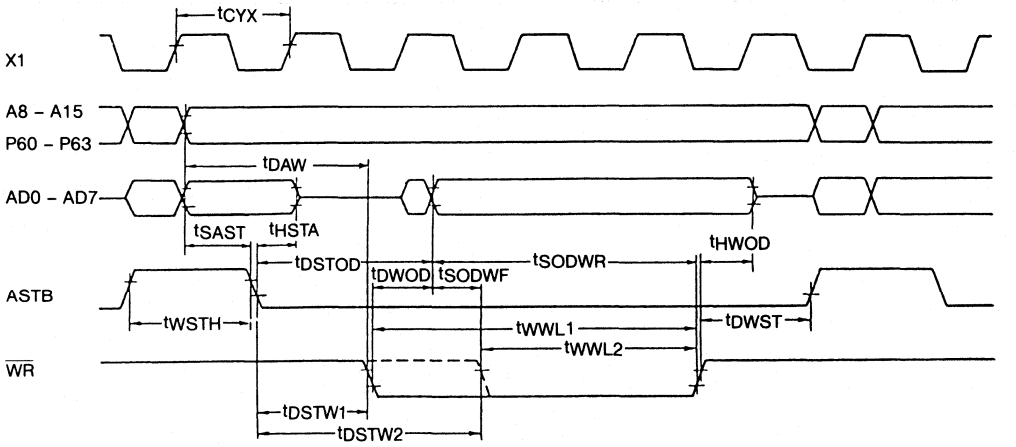
AC Timing Test Points



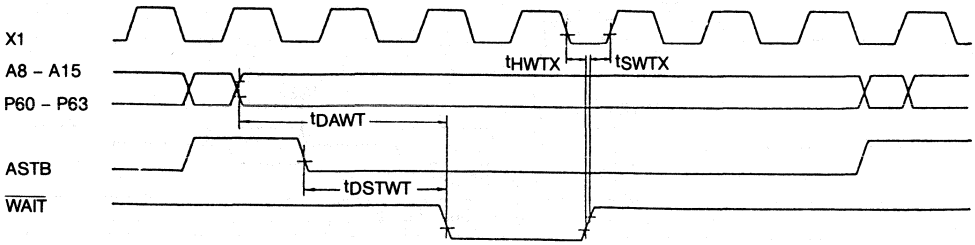
Timing Waveforms
Read Operation



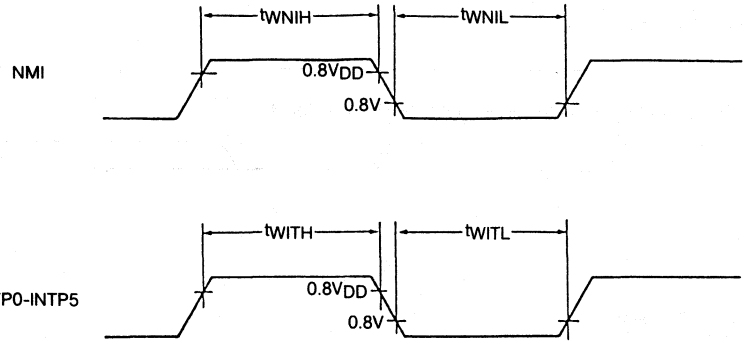
Write Operation



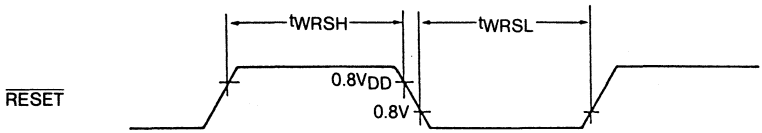
$\overline{\text{WAIT}}$ Input Timing



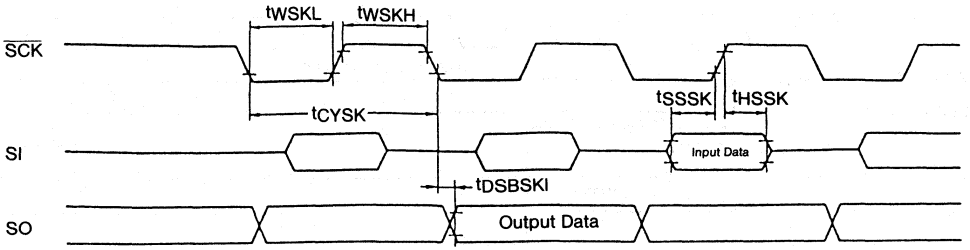
Interrupt Input Timing



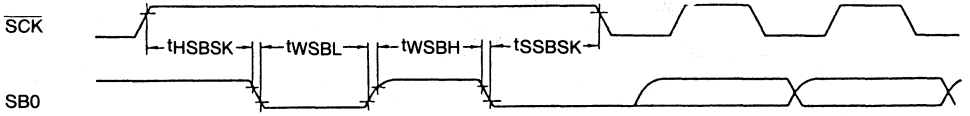
Reset Input Timing



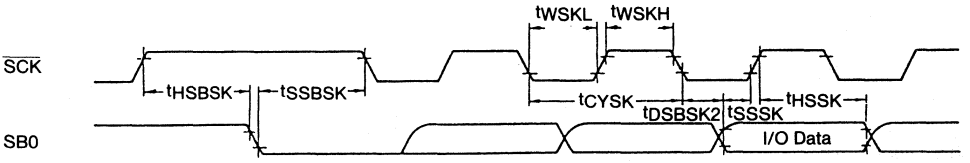
Serial Operation
Serial I/O Mode



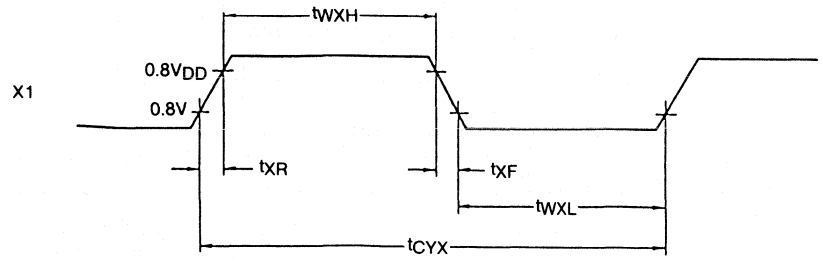
SBI Mode
Bus Release Operation Transmit



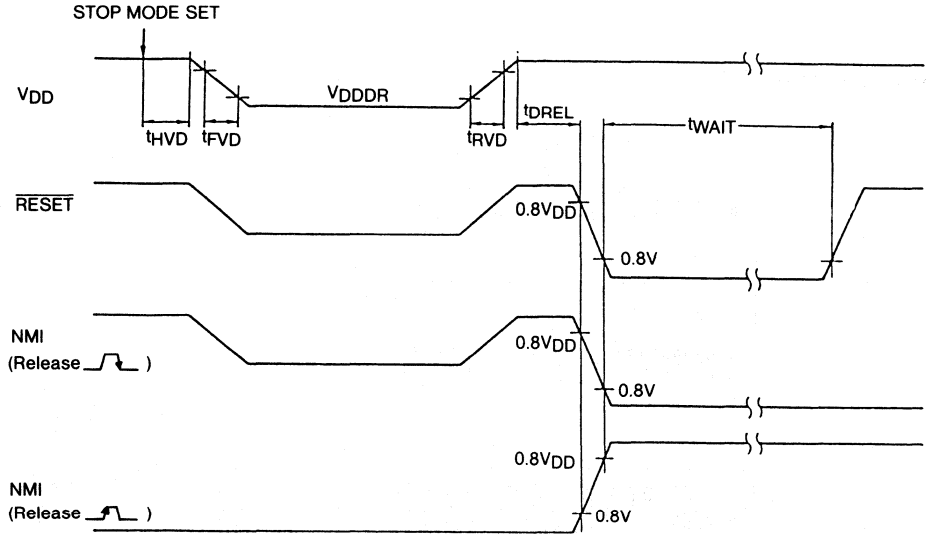
Command Operation Transmit



Clock Timing

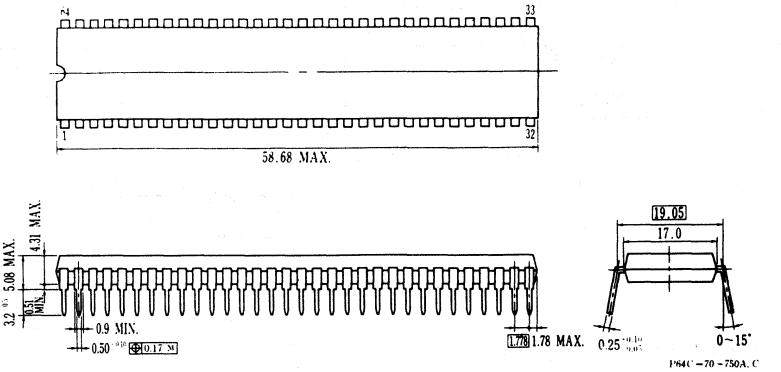


Data Hold Characteristics

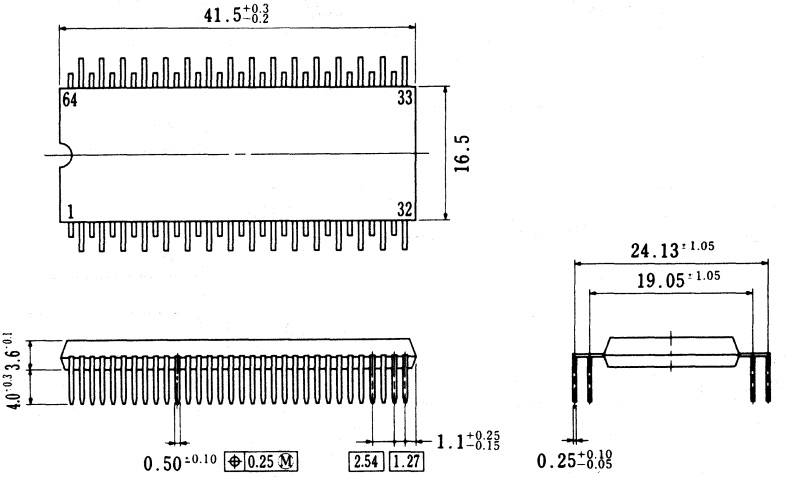


Package Dimensions

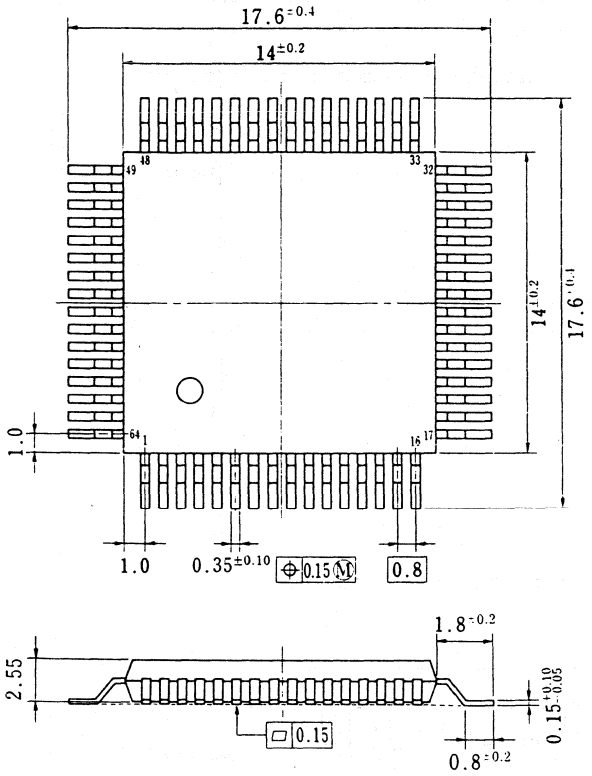
64 pin plastic shrink DIP (750mil) (Units: mm)



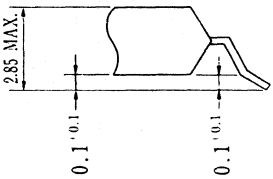
64 pin plastic QUIP (Units: mm)



64-pin plastic QFP (Units: mm)



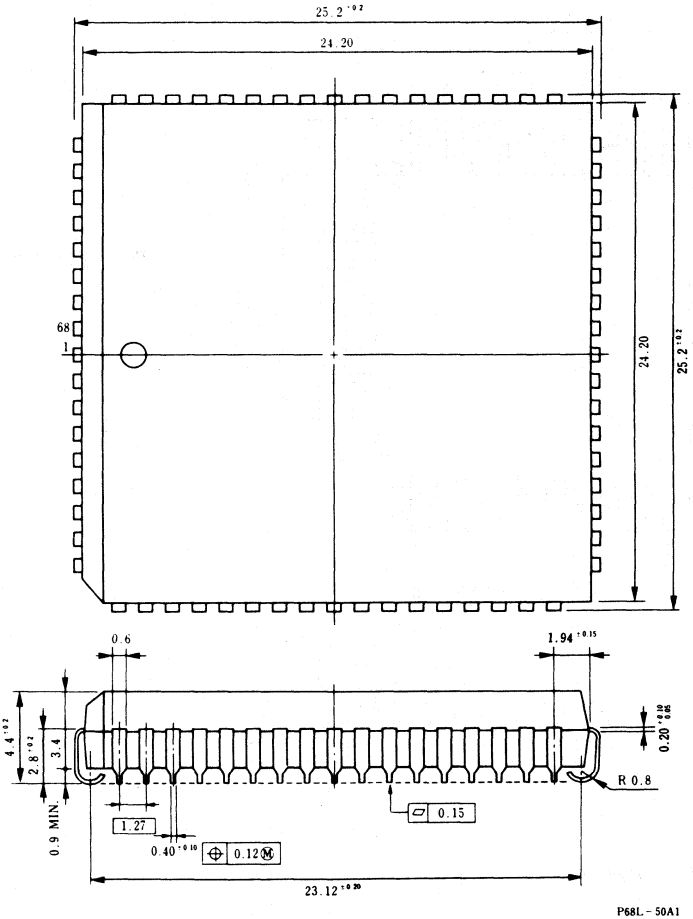
Detail of pin shape



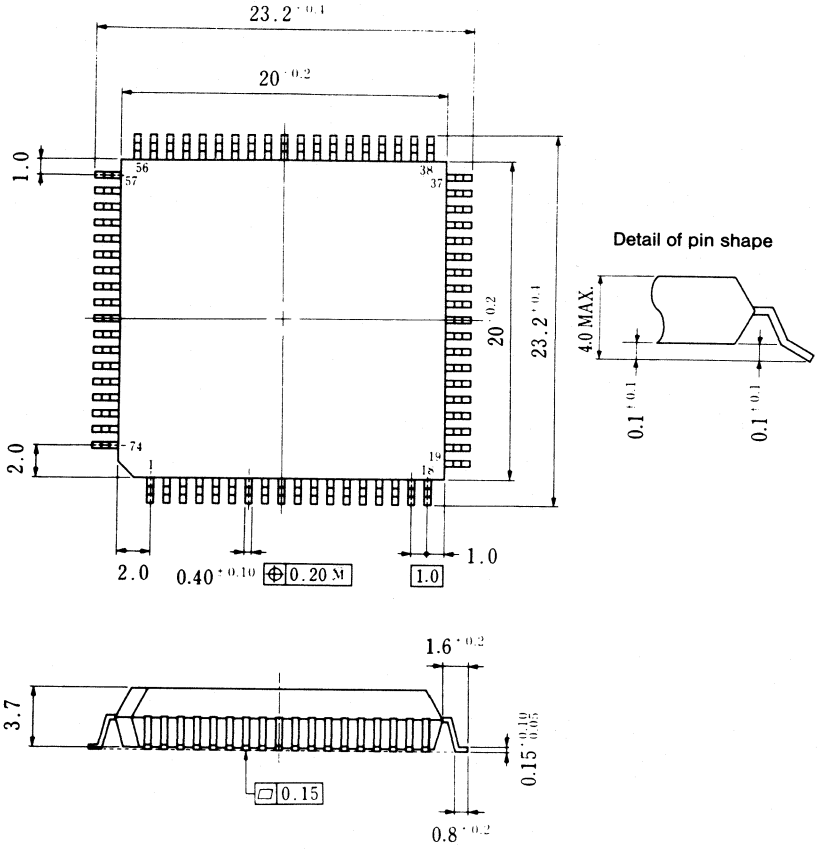
P64GC-80-AB8

Note: Small 0.8 mm pin pitch package

68 pin PLCC (Units: mm)



74-pin plastic QFP (Units: mm)



S74GJ-100-5BJ

Description

The μPD78P214 is an 8-bit single-chip microcomputer with the onchip mask ROM of the μPD78214 replaced with EPROM. Since the μPD78P214 is a user-programmable microcomputer, it is suitable for system development evaluation and small production.
Use this data sheet together with μPD78212-/213/214 data sheet.

Features

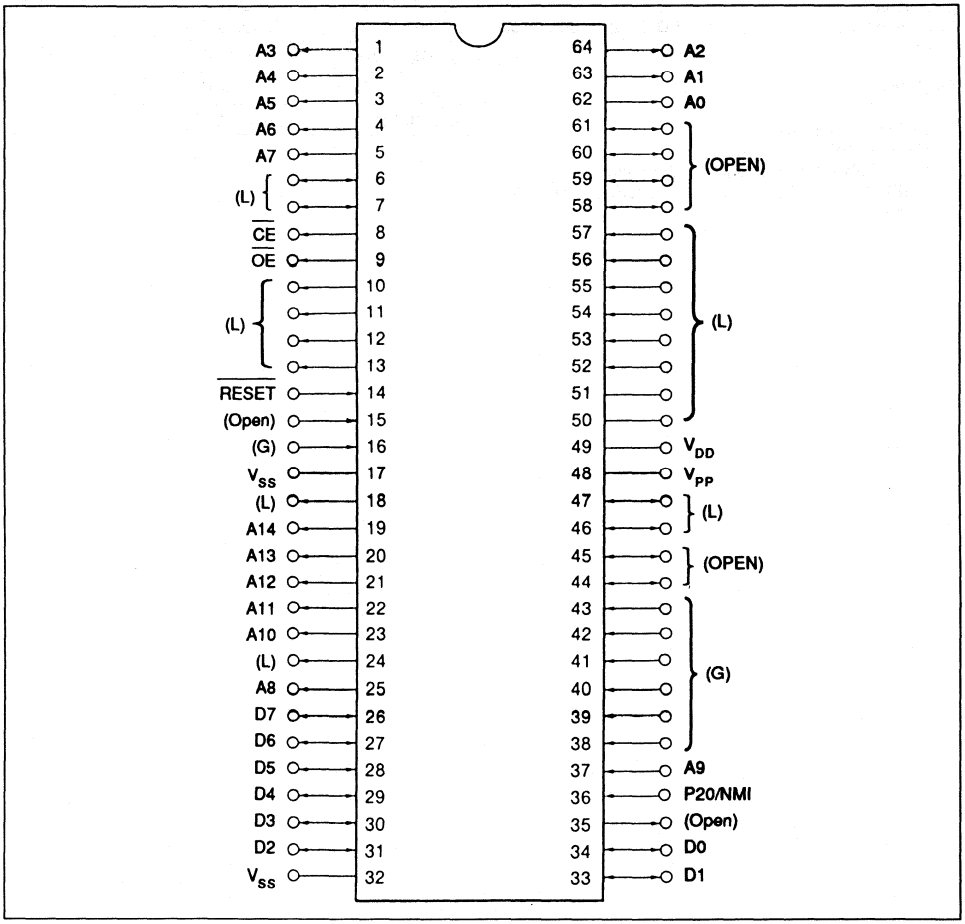
- μPD78214 compatible
- On-chip EPROM
  - μPD78P214DW: Reprogrammable version
  - μPD78P214CW/GC/GJ/GQ/L: One-time programable version

Ordering Information

Ordering Code	Package	ROM
μPD78P214DW	64-pin SDIP ceramic with window	16K UVPROM
μPD78P214CW	64-pin SDIP	16K OTPROM
μPD78P214GQ-36	64-pin QUIP	
μPD78P214GC	64-pin QFP	
μPD78P214GJ	74-pin QFP	
μPD78P214L	68-pin PLCC	

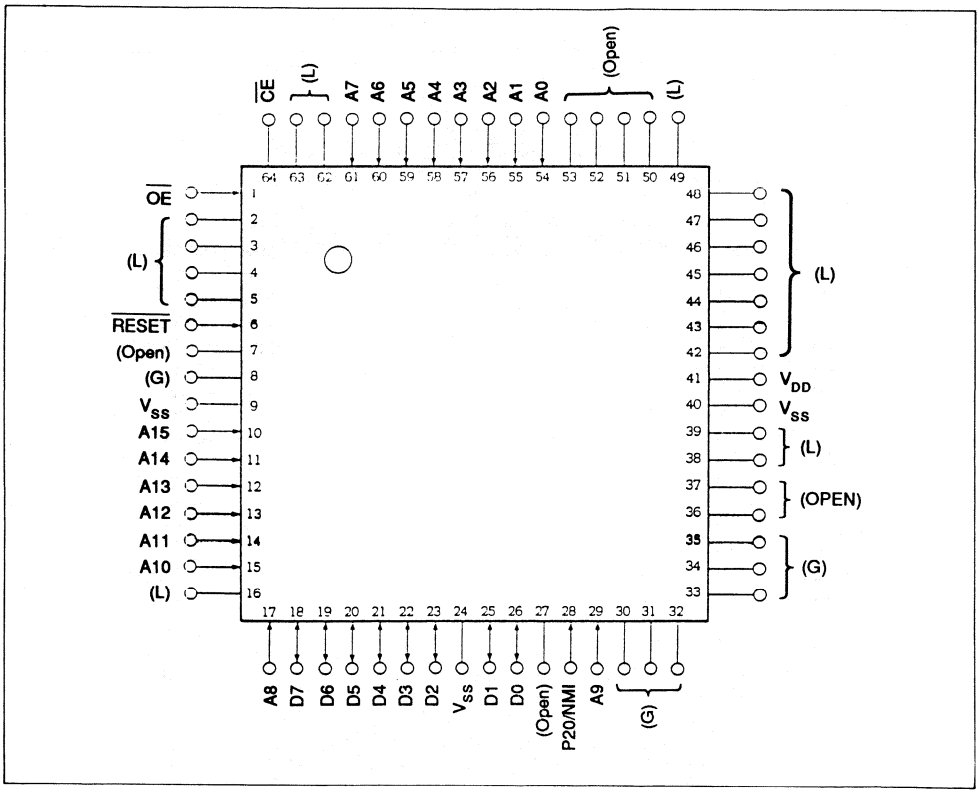
Pin Configurations (top view)

For pin configurations in Normal Mode operation corresponding pin functions tables, please refer to μPD78212/213/214 data sheet. Pin configurations in PROM programming mode (P20/NMI = 12.5V, RESET = L).
(a) 64-pin plastic shrink DIP, 64-pin plastic QUIP, and 64-pin ceramic shrink DIP with a window.



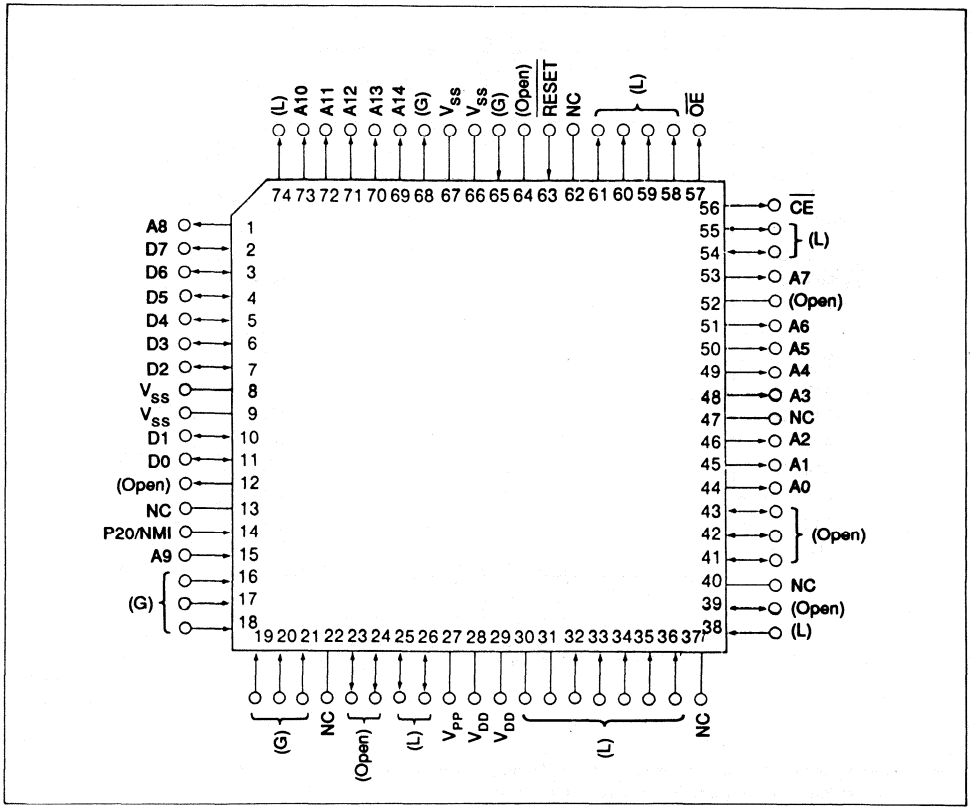
Note: Processing for pins wich are not used in the PROM programming mode is indicated in parentheses.
L: Connect these pins indepently to V_{ss} via a resistor.
G: Connect these pins to V_{ss}.
Open: No connection required.

(b) 64-pin plastic QFP



Note: Processing for pins wich are not used in the PROM programming mode is indicated in parentheses.
L: Connect these pins independently to V_{SS} via a resistor.
G: Connect these pins to V_{SS}.
Open: No connection required.

(c) 74-pin plastic QFP



Note: Processing for pins wich are not used in the PROM programming mode is indicated in parentheses.

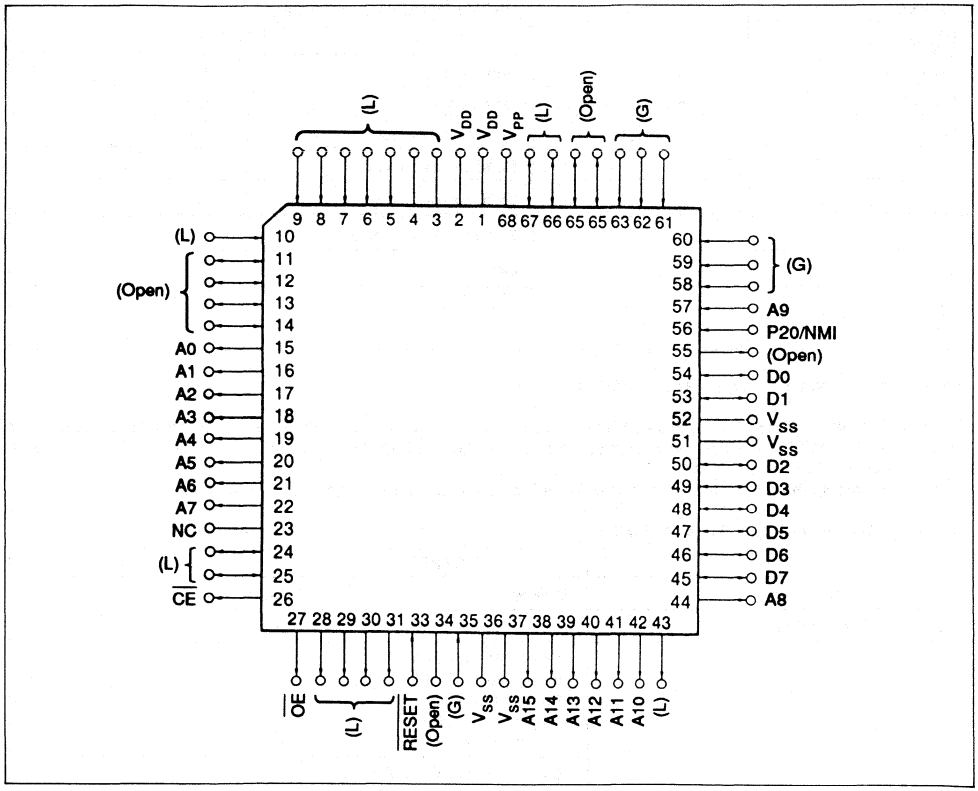
L: Connect these pins independently to V_{SS} via a resistor.

G: Connect these pins to V_{SS}.

Open: No connection required.

Remarks: NC; not connected internally.

(d) 68-pin PLCC



Note: Processing for pins wich are not used in the PROM programming mode is indicated in parentheses.

L: Connect these pins independently to V_{SS} via a resistor.

G: Connect these pins to V_{SS}.

Open: No connection required.

Remarks: NC; not connected internally.

Pin Funktions in PROM Programming Mode (P20/NMI = 12.5V, $\overline{\text{RESET}}$ = L)

Pin Name	Input/Output	Function
P20/NMI	Input	PROM programming mode set
RESET		
A0 to A14		Address bus
D0 to D7	Input/Output	Data bus
CE	Input	PROM enable input
OE		Read strobe for Prom
V_{PP}	—	Write power supply
V_{DD}		Positive power supply
V_{SS}		GND
NC		—
IC		

Differences Between μPD78P214 and μPD78214

Since the μPD78P214 is a product with the μPD78214 on-chip mask ROM replaced with a rewriteable EPROM, functions other than those related to EPROM, such as write/verify, are the same as those of the μPD78214. The Table below shows the differences between μPD78P214 and μPD78214.
For details regarding the CPU functions and on-chip hardware, refer to the μPD78214 user's manual and relevant manuals.

Differences between μPD78P214 and μPD78214

Item	μPD78P214	μPD78214
On-chip program memory	EPROM	Mask ROM
Eprom programming pin	Yes	No
Package	• 64-pin plastic shrink DIP • 64-pin plastic QUIP • 68-pin PLCC • 64-pin plastic QFP • 74-pin plastic QFP	
	• 64-pin ceramic shrink DIP with window (Reprogrammable)	—

Programming

The on-chip program memory of the μPD78P214 is a 16384 x 8-bit electrically programmable PROM.
For PROM programming, the PROM programming mode is set using the NMI and RESET pins.
The programming characteristics are compatible with the μPD27C256A.
Note: Carry out programming in the addres range from 0000H to 3FFFH. In case of a PROM writer wich cannot specify programming addresses, write FFH at address 4000H. (Data write operation exept for FFH is not quaranteed.) NEC reserves address 4000H for future functional extention.

Operation Mode

When +6V and +12.5V are applied to V_{DD} pin and V_{PP} pin, respectivaly, the μPD78P214 is set to the program-wrrite/verify mode. This mode can be reset to the operation mode described in Table 3-1 by setting CE and OE pins.
In the read mode, the μPD78P214 can read the PROM contents.

PROM Programming Operation Mode

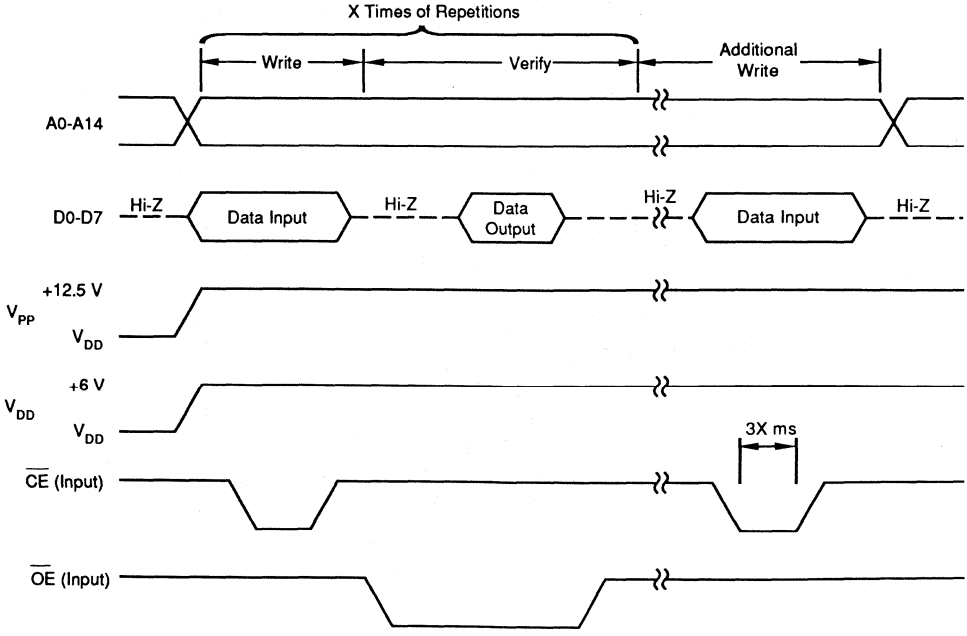
Mode \ Pin	NMI	$\overline{RESET}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}	D0 to D7
Program write	12.5 V	L	L	H	+12.5 V	+6 V	Data output
Program verify			H	L			Data ouput
Program inhibit			H	H			High impedance
Read			L	L	+5 V	+5 V	Data output
Output disable			L	H			High impedance
Standby			H	L/H			High impedance

Note: When V_{PP} is set to +12.5 V and V_{DD} is set to +6 V, it is inhibited to set both $\overline{CE}$ and $\overline{OE}$ to L.

PROM Write Procedure

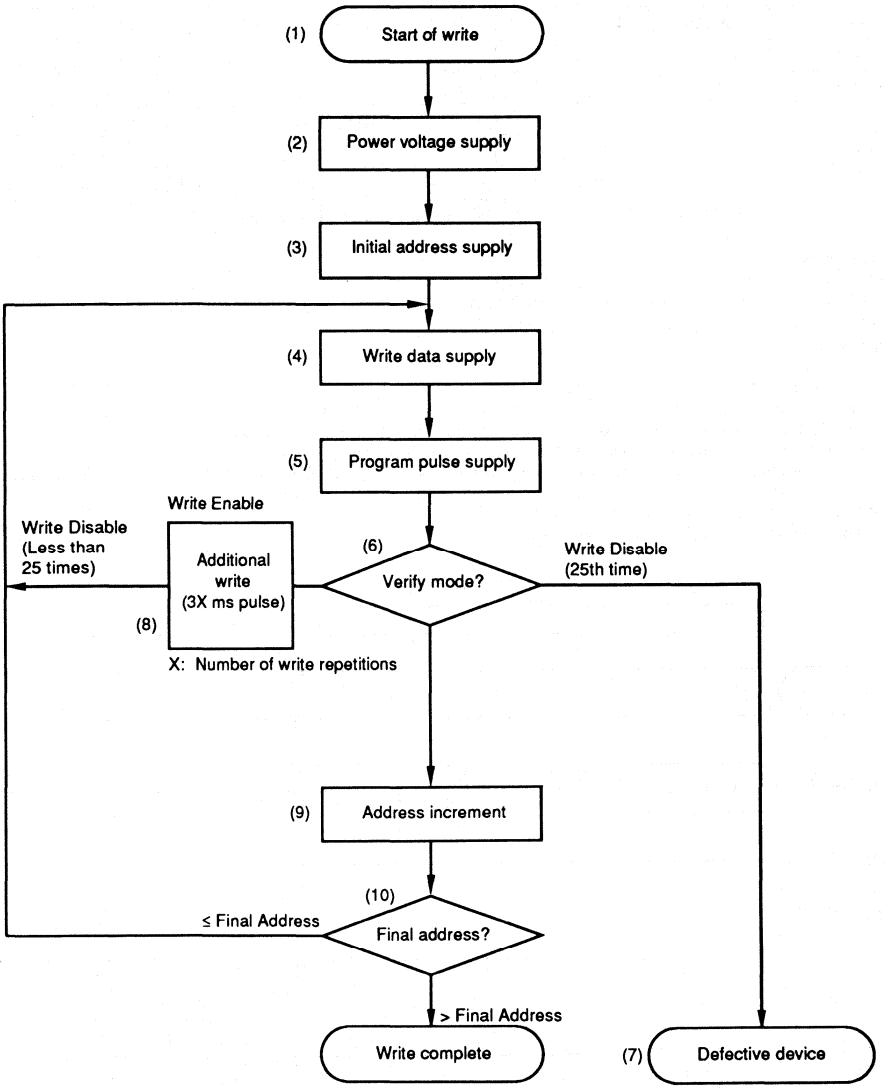
PROM write can be executed at high speeds using the following procedure:

(1) Fix the RESET pin to the low level. Apply +12.5 V to the NMI pin. Treat all other inused pins as shown in the pin configuration.
(2) Apply +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin.
(3) Supply the initial address.
(4) Supply write data.
(5) Supply a 1 ms program pulse (active low) to the CE pin.
(6) Set the verify mode. If data has been written, procedure to step (9). If data has not been written, go to (8) and repeat steps (4) through (6). If data cannot yet be written after repeating the three steps 25 times, proceed to step (7).
(7) Stop carrying out the write operation assuming that the device is defective.
(8) Supply write data and then suppy (number of repetitions of steps (4) through (6): X) x 3 ms program pulse (additional write).
(9) Increment the address.
(10) Repeat steps (4) through (9) up to the final addresss.
The timings in steps (2) through (8) are shown in Figure 3-1.



PROM Write/Verify Timings

Write Operation Flowchart

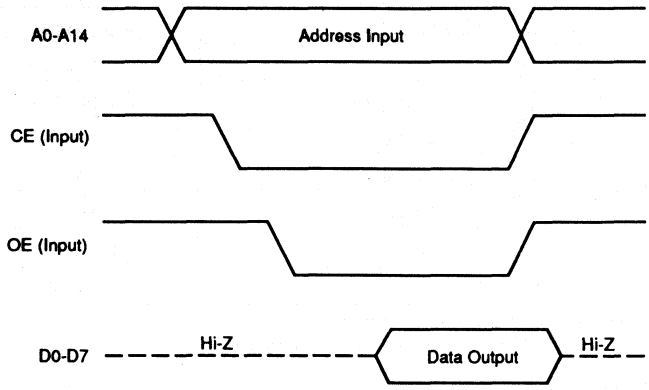


PROM Read Procedure

PROM contents can be read onto the external data bus (D0 to D7) using the following procedure:

(1) Fix the RESET pin to the low level. Apply +12.5 V to the NMI pin. Treat all other unused pins as shown in the pin configuration.
(2) Apply +5 V to the V_{DD} and V_{PP} pins.
(3) Input the address of the data to be read to the A0 to A14 pins.
(4) Set the read mode D0 to D7 pins.
The timing in steps (2) through (5) are shown in Figure 3-3.

PROM Read Timings



Erase Characteristics (μPD78P214DW only)

The μPD78P214DW can erase the programmed data content (FFH) by applying light having wavelengths of less than about 400 nm.
To erase the μPD78P214DW program memory contents, normally apply ultraviolet rays having a weavelength of 254 nm. The total radiation required to erase the μPD78P214DW contents completely is a minimum of 15 W s/cm^2 (ultraviolet strength x erase time). The erase time is approximately 15 to 20 minuten (when a 12000 μW/cm^2 ultraviolet lamp is used). The erase time may possible become longer due to deterioration in the performance of the ultraviolet lamp or fouling of the package window. For the erase operation, place the μPD78P214DW within 2.5 Cm from the ultraviolet lamp. Use the ultraviolet lamp with the filter removed.

Erase Window Sealing (μPD78P214DW only)

Except when erasing EPROM contents, apply a protective seal to the erase window. This is important to prevent the EPROM contents from being inadvertently erased due to light other than erase lamp or the internal circuits other than the EPROM from malfunctioning due to light.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		–0.5 ~ +7.0	V
	AV_{REF}		–0.5 ~ +V_{DD}	V
	AV_{SS}		–0.5 ~ +0.5	V
Input Voltage	V_{I1}	note 1 Pins	–0.5 ~ V_{DD} +0.5	V
	V_{I2}	except note 1 Pins	–0.5 ~ AV_{REF} +0.5	V
	V_{I3}	note 2 Pins	–0.5 ~ +13.5	V
Output Voltage	V_O		–0.5 ~ V_{DD} +0.5	V
Low Level Output Current	I_{OL}	One Output Pin	15	mA
		All Output Pins	100	mA
High Level Output Current	I_{OH}	One Output Pin	–10	mA
		All Output Pin	–50	mA
Operating Temperature	t_{OPT}		–40 ~ +85	°C
Storage Temperature	t_{STG}		–65 ~ +150	°C

Note 1: P70/AN0 – P75/AN5, P66/$\overline{WAIT}$/AN6, P67/$\overline{REFRQ}$/AN7
Note 2: P20/NMI, $\overline{EA}$/V_{PP} and P21/INTP0/A9 pins in the PROM programming mode

Recommended Operating Conditions

Clock Frequency	Operating Temperature (Ta)	Operating Voltage (V_{DD})
4 MHz ≤ f_{XX} ≤ 12 MHz	–40°C ~ +85°C	+5.0V±10%

Capacitance (Ta = 25°C, V_{DD} = V_{ss} = 0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_1	f_C = 1 MHz Unmeasured Pins Returned to 0V			20	pF
Output Capacitance	C_0				20	pF
In/Output Capacitance	C_{10}				20	pF

DC Characteristics (Ta = - 40°C ~ +85°C, V_{DD} = + 5.0V ± 10%, V_{SS} = OV)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	except note1 and note2	2.2		V_{DD}	V
	V_{IH2}	note1 Pins	2.2		AV_{REF}	V
	V_{IH3}	note2 Pins	$0.8V_{DD}$		V_{DD}	V
Output Low Voltage	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
	V_{OL2}	I_{OL} = 8.0 mA note3 Pins			1.0	V
Output High Voltage	V_{OH1}	I_{OH} = – 1.0 mA	V_{DD} -1.0			V
	V_{OH2}	I_{OH} = – 100μA	V_{DD} -0.5			V
	V_{OH3}	I_{OH} = – 5.0 mA note 4 Pins	2.0			V
Input Leak. Current	I_{LI}	$OV \leq V_I \leq V_{DD}$			±10	μA
Output Leak. Current	I_{LO}	$OV \leq V_O \leq V_{DD}$			±10	μA
AV_{REF} Current	AI_{REF}	Operation Mode f_{XX} = 12 MHz		1.5	5	μA
V_{DD} Supply Current	I_{DD1}	Operation Mode f_{XX} = 12 MHz		20	40	mA
	I_{DD2}	HALT Mode f_{XX} = 12 MHz		7	20	mA
Data Retention Voltage	V_{DDDR}	STOP Mode	2.5		5.5	V
Data Retention Current	I_{DDR}	STOP MODE V_{DDDR} = 2.5 V		2	20	μA
		STOP MODE V_{DDDR} = 5V ± 10%		5	50	μA
Pull-up Resistance	R_L	V_I=OV	15	40	80	kΩ

Note1: X1, X2 $\overline{\text{RESET}}$, P20/NMI, P21/INTPO, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{\text{SCK}}$, P33/SB0, and $\overline{\text{EA}}$ Pins
Note2: P70/AN0-P75/AN5, P66/WAIT/AN6, P67/REFRQ/AN7
Note3: P40/AD0 – P47/AD7, P50/A08 – P57/A15
Note4: P00 – P07

AC Characteristics (Ta = −40°C ~ +85°C, V_{DD} = +5.0V ± 10%, V_{SS} = 0V)
Memory Read/Write Operation:

Parameter	Symbol	Test Condition	Min	Max	Unit
X1 Input Cycle Time	t_{CYX}		82	250	ns
Address Setup Time to ASTB ↓	t_{SAST}		52		ns
Address Hold Time After ASTB ↓	t_{HSTA}	R_L=5kΩ, C_L=50pF	25		ns
Address to $\overline{RD}$ ↓ delay Time	t_{DAR}		129		ns
Address Float To $\overline{RD}$ ↓ Time	t_{FAR}		11		ns
Address to Data Input Time	t_{DAID}			228	ns
ASTB ↓ to Data Input Time	t_{DSTID}			181	ns
$\overline{RD}$ ↓ to Data Input Time	t_{DRID}			99	ns
ASTB ↓ to $\overline{RD}$ ↓ delay Time	t_{DSTR}		52		ns
Data Hold After $\overline{RD}$ ↑	t_{HRID}		0		ns
$\overline{RD}$ ↑ to Address Active Time	t_{DRA}		124		ns
$\overline{RD}$ ↑ to ASTB ↑ delay Time	t_{DRST}		124		ns
$\overline{RD}$ Low Level Width	t_{WRL}		124		ns
ASTB High Level Width	t_{WSTH}		52		ns
Address to $\overline{WR}$ ↓ delay Time	t_{DAW}		129		ns
ASTB ↓ to Data Output Time	t_{DSTOD}			142	ns
$\overline{WR}$ ↓ to Data Output Time	t_{DWOD}			60	ns
ASTB ↓ to $\overline{WR}$ ↓ delay Time	t_{DSTW1}		52		ns
	t_{DSTW2}	Refresh Mode	129		ns
Data Setup Time to $\overline{WR}$ ↑	t_{SODWR}		146		ns
Data Setup Time to $\overline{WR}$ ↓	t_{SODWF}	Refresh Mode	22		ns
Data Hold Time After $\overline{WR}$ ↑	t_{HWOD}	(2)	20		ns
$\overline{WR}$ ↑ to ASTB ↑ delay Time	t_{DWST}		42		ns
$\overline{WR}$ Low Level Width	t_{WWL1}		196		ns
	t_{WWL2}	Refresh Mode	114		ns
Address to $\overline{WAIT}$ ↓ Input Time	t_{DAWT}			146	ns
ASTB ↓ to $\overline{WAIT}$ ↓ Input Time	t_{DSTWT}			84	ns
X1 Low Setup Time to $\overline{WAIT}$ ↑	t_{SWTX}		0		ns
X1 Low Hold Time to $\overline{WAIT}$ ↑	t_{HWTX}		0		ns

Note: (1) This Table show the value at f_{XX} = 12MHz and C_L = 100pF.

(2) C_L = 100 pF R_L = 2KΩ

Serial Operation:

Parameter	Symbol	Test Condition	Min	Max	Unit
$\overline{SCK}$ Cycle Time	tCYSK	External Clock Input	1.0		μs
		Internal 16 Devide Out.	1.3		μs
		Internal 64 Devide Out.	5.3		μs
$\overline{SCK}$ Low Level Width	tWSKL	External Clock Input	420		ns
		Internal 16 Devide Out.	556		ns
		Internal 64 Devide Out.	2.5		μs
$\overline{SCK}$ High Level Width	tWSKH	External Clock Input	420		ns
		Internal 16 Devide Out.	556		ns
		Internal 64 Devide Out.	2.5		μs
SI, SB0 Setup Time to $\overline{SCK}$ ↑	tSSSK		150		ns
SI, B0, Hold Time After $\overline{SCK}$ ↑	tHSSK		400		ns
SB0 Output Delay Time to $\overline{SCK}$ ↓	tDSBSK1	CMOS Push-pull Output	0	300	ns
	tDSBSK2	Open-drain Out.R_L = 1 KΩ	0	800	ns
$\overline{SCK}$ High Setup Time to SB0 ↓	tHSBSK	SBI mode	4		tCYX
$\overline{SCK}$ High Hold Time After SB0 ↓	tSSBSK		4		tCYX
SB0 Low Level Width	tWSBL		4		tCYX
SB0 High Level Width	tWSBH		4		tCYX

Note: This Table show the value at f_{XX} = 12MHz and C_L = 100pF.

Other Operation:

Parameter	Symbol	Test Condition	Min	Max	Unit
NMI Low Level Width	tWNIL		10		μs
NMI High Level Width	tWNIH		10		μs
INTP0-INTP5 Low Level Width	tWITL		24		tCYX
INTP0-INTP5 High Level Width	tWITH		24		tCYX
$\overline{RESET}$ Low Level Width	tWRSL		10		μs
$\overline{RESET}$ High Level Width	tWRSH		10		μs

External Clock Timing:

Parameter	Symbol	Test Condition	Min	Max	Unit
X1 Input Low Level Width	tWXL		30	130	ns
X1 Input High Level Width	tWXH		30	130	ns
X1 Input Rise Time	tXR		0	30	ns
X1 Input Fall Time	tXF		0	30	ns
X1 Input Cycle Time	tCYX		82	250	ns

AD Converter Characteristics (Ta = -40°C ~ +85°C, V_{DD} = +5.0V ± 10%, 4V ≤ AV_{REF} ≤ V_{DD}, AV_{SS} = V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution			8			bit
Absolute Accuracy					0.8%	LSB
		Ta=-10°C~+70°C 3.4V≤AV_{REF}≤V_{DD}			0.8%	LSB
		Ta=-10°C~+70°C			0.4%	LSB
Quantization Error					±1/2	LSB
Conversion Time	t_{CONV}	83ns ≤ t_{CYX} ≤ 125ns	360			t_{CYX}
		125ns ≤ t_{CYX} ≤ 250ns	240			t_{CYX}
Sampling Time	t_{SAMP}	83ns ≤ t_{CYX} ≤ 125ns	72			t_{CYX}
		125ns ≤ t_{CYX} ≤ 250ns	48			t_{CYX}
Analog Input Voltage	V_{IAN}		0		AV_{REF}	V
Analog Input	R_{AN}			1000		MΩ
Reference Voltage	AV_{REF}		3.4		V_{DD}	V
AV_{REF} Current	AI_{REF}	Operation Mode, f_{XX} = 12MHz		1.5	5.0	mA
		STOP MODE		0.2	1.5	mA

Other operation

Parameter	Symbol	Conditions	Min	Max	Units
NMI low level width	tWNIL		10		μs
NMI high level width	tWNIH		10		μs
INTP0-INTP5 low level width	tWITL		24		tCYX
INTP0-INTP5 high level width	tWITH		24		tCYX
$\overline{RESET}$ low level width	tWRSL		10		μs
$\overline{RESET}$ high level width	tWRSH		10		μs

Definition of bus timing depending on cycle time t_{CYX} TA = -40°C ~ +85°C, V_{DD} = +5.0V ±10%, V_{SS} = 0V

Parameter	Symbol	Specification	Limit	12MHz	Unit
X1 Input Cycle Time	t_{CYX}		Min	82	ns
Address Setup Time to ASTB ↓	t_{SAST}	t_{CYX}-30	Min	52	ns
Address to $\overline{RD}$ ↓ delay Time	t_{DAR}	2t_{CYX}-35	Min	129	ns
Address Float to $\overline{RD}$ ↓ Time	t_{FAR}	t_{CYX}/2-30	Min	11	ns
Adress to Data Input Time	t_{DAID}	(4+2n) t_{CYX}-100	Max	228	ns
ASTB ↓ to Data Input Time	t_{DSTID}	(3+2n) t_{CYX}-65	Max	181	ns
$\overline{RD}$↓ to Data Input Time	t_{DRID}	(2+2n) t_{CYX}-65	Max	99	ns
ASTB ↓ to $\overline{RD}$ ↓ delay Time	t_{DSTR}	t_{CYX}-30	Min	52	ns
$\overline{RD}$ ↑ to Address Active Time	t_{DRA}	2t_{CYX}-40	Min	124	ns
$\overline{RD}$ ↑ to ASTB ↑ delay Time	t_{DRST}	2t_{CYX}-40	Min	124	ns
$\overline{RD}$ Low Level Width	t_{WRL}	(2+2n) t_{CYX}-40	Min	124	ns
ASTB High Level Width	t_{WSTH}	t_{CYX}-30	Min	52	ns
Address to $\overline{WR}$ ↓ delay Time	t_{DAW}	2t_{CYX}-35	Min	129	ns
ASTB ↓ to Data Output Time	t_{DSTOD}	t_{CYX}+60	Max	142	ns
ASTB ↓ to $\overline{WR}$ ↓ delay Time	t_{DSTW1}	t_{CYX}-30	Min	52	ns
	t_{DSTW2}	2t_{CYX}-35 Refresh Mode	Min	129	ns
Data Setup Time to$\overline{WR}$ ↑	t_{SODWR}	(3+2n)t_{CYX}-100	Min	146	ns
Data Setup Time to $\overline{WR}$ ↓	t_{SODWF}	t_{CYX}-60 Refresh Mode	Min	22	ns
$\overline{WR}$↑ to ASTB ↑ delay Time	t_{DWST}	t_{CYX}-40	Min	42	ns
$\overline{WR}$ Low Level Width	t_{WWL1}	(3+2n) t_{CYX}-50	Min	196	ns
Refresh Mode	t_{WWL2}	(2+2n) t_{CYX}-50 (Refresh Mode)	Min	114	ns
Address to $\overline{WAIT}$ ↓ Input Time	t_{DAWT}	3t_{CYX}-100	Max	146	ns
ASTB ↓ Input time	t_{DSTWT}	2t_{CYX}-80	Max	84	ns

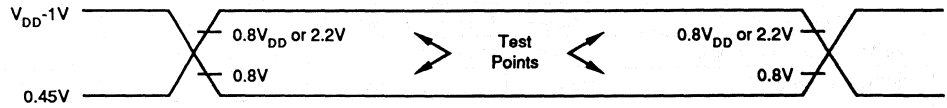
Note: n means number of wait Cycles

Memory Data Retention Characteristic (Ta = –40°C to +85°C)

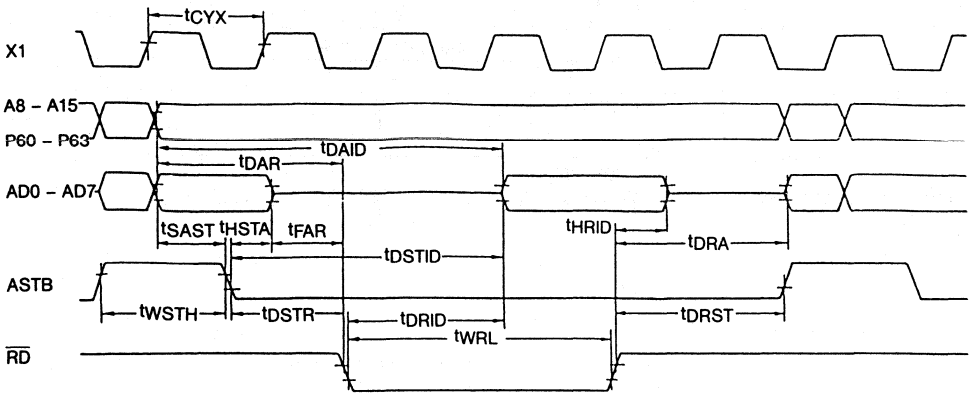
Parameter	Symbol	Test Condition	MIN.	TVP.	MAX.	Unit
Data retention Voltage	V_{DDDR}	STOP Mode	2.5		5.5	V
Data retention Current	I_{DDDR}	V_{DDDR}=2.5V		2	20	μA
		V_{DDDR}=5V±10%		5	50	μA
V_{DD} Rise Time	t_{RVD}		200			μs
V_{DD} Fall Time	t_{FVD}		200			μs
V_{DD} Hold Time (for STOP mode setting)	t_{HVD}		0			ms
STOP Release Signal Time	t_{DREL}		0			ms
Oscillation Stabilize Wait Time	t_{wait}	Crystal Oscillator	30			ms
		Ceramic Oscillator	5			ms
Input Low Voltage	V_{IL}	Note Pins	0		$0.1V_{DDDR}$	V
Input High Voltage	V_{IH}	Note Pins	$0.9V_{DDDR}$		V_{DDDR}	V

Note: $\overline{RESET}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{SCK}$, P33/SO/SB0, and $\overline{EA}$ Pins

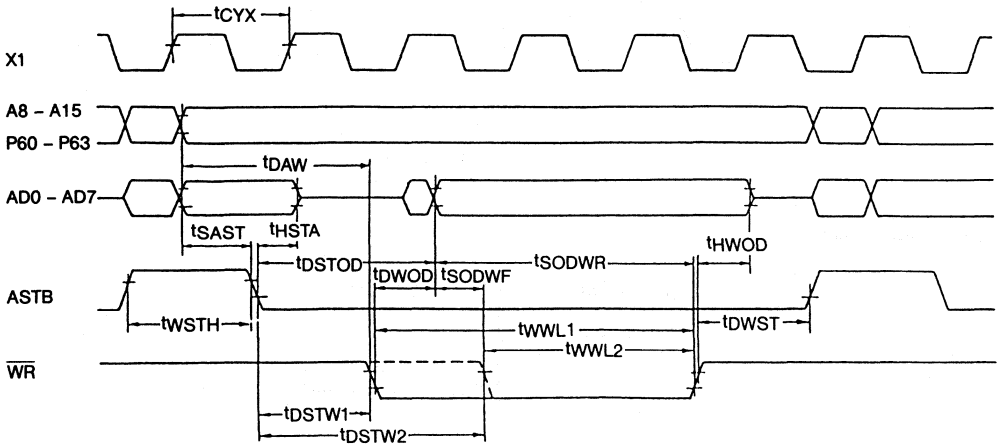
AC Timing Test Points



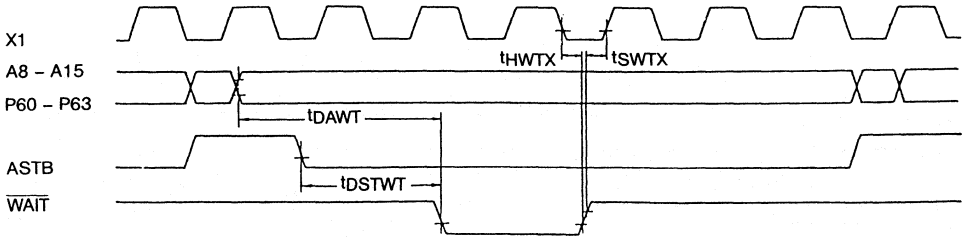
Timing Waveforms
Read Operation



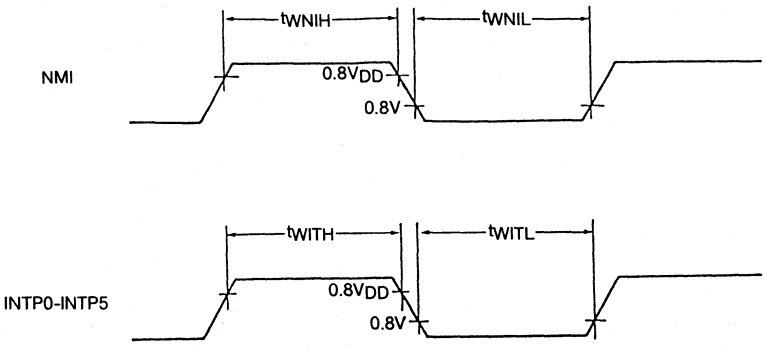
Write Operation



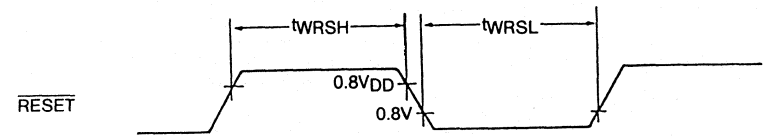
$\overline{\text{WAIT}}$ Input Timing



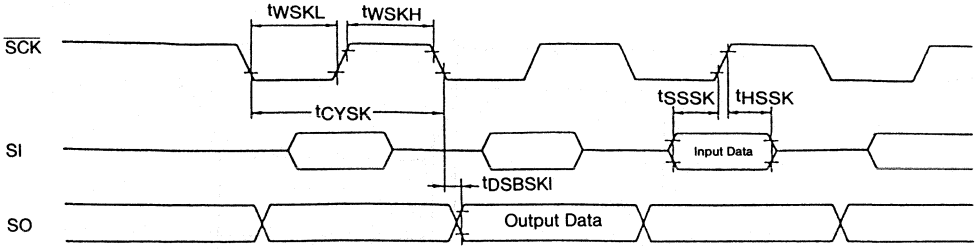
Interrupt Input Timing



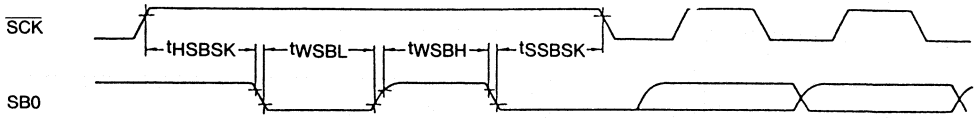
Reset Input Timing



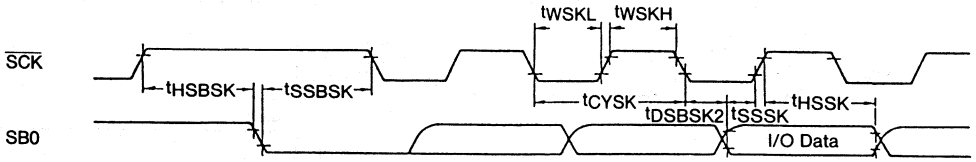
Serial Operation
Serial I/O Mode



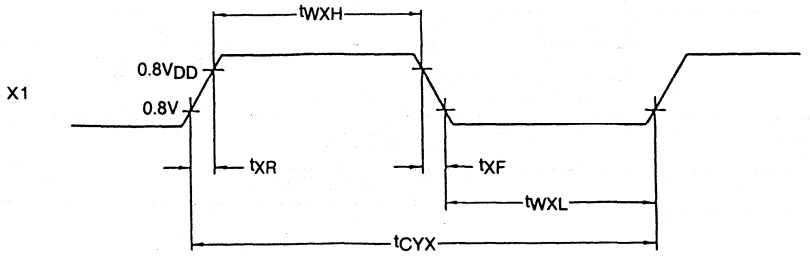
SBI Mode
Bus Release Operation Transmit



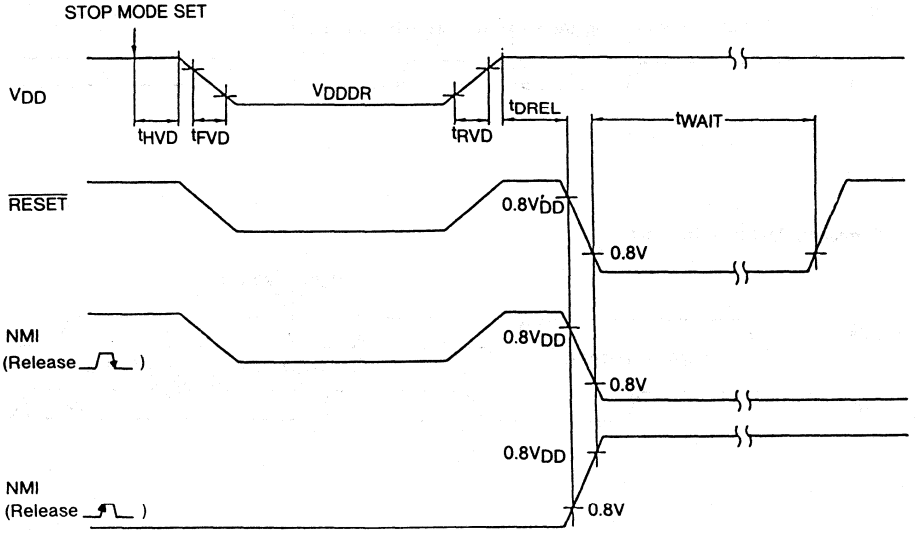
Command Operation Transmit



Clock Timing



Data Hold Characteristics



DC Programming Characteristics
($Ta = 25 \pm 5°C$, V_{IP} (Note 1) $= 12.5 \pm 0.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Symbol (Note 2)	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	V_{IH}		2.4		$V_{DDP}+0.3$	V
Low level input voltage	V_{IL}	V_{IL}		−0.3		0.8	V
Input leak current	V_{LIP}	V_{LI}	$0 \le V1 \le V_{DDP}$			10	μA
High level output voltage	V_{OH1}	V_{OH2}	$I_{OH} = -400$ μA	2.4			V
	V_{OH2}	V_{OH2}	$I_{OH} = -100$ μA	$V_{DD}-0.7$			V
Low level output voltage	V_{OL}	V_{OL}	$I_{OL} = 2.1$ mA			0.45	V
Output leak current	I_{LO}		$0 \le V_O \le V_{DDP}$, $\overline{OE} = V_{IH}$			10	μA
NMI pin high voltage input current	I_{IP}					±10	μA
V_{DDP} power voltage	V_{DDP}	V_{CC}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} power voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	$V_{PP} = V_{DDP}$			V
V_{DDP} power current	I_{DD}	I_{CC}	Program memory write mode		5	30	mA
			Program memory read mode $\overline{CE} = V_{IL}$, $V_I = VIH$		5	30	mA
V_{PP} power current	I_{PP}	I_{PP}	Program memory write mode $\overline{CE} = VIL$, $\overline{OE} = VIH$		5	30	mA
			Program memory read mode		1	100	μA

Note 1: Voltage applied to P20/NMI pin.
2: Corresponding pin symbols of the μPD27C256A.

2

Program Operation

AC Characteristics (Ta = 25 ± 5°C, V_{IP} (Note 1) = 12.5 ± 0.5V, V_{DD} = 6 ± 0.25V, V_{PP} = 12.5 ± 0.3V, V_{SS} = 0V)

Parameter	Symbol	Symbol (Note 2)	Condition	Min.	Typ.	Max.	Unit
Address setup tme (vs. $\overline{CE}$ ↓)	t_{SAC}	t_{AS}		2			μs
Data → $\overline{OE}$ ↓ delay time	t_{DDOO}	t_{OES}		2			μs
Input data setup time (vs. $\overline{CE}$ ↓)	t_{SIDC}	t_{DS}		2			μs
Address hold time (vs. $\overline{CE}$ ↑)	t_{HCA}	t_{AH}		2			μs
Input data hold time (vs. $\overline{CE}$ ↑)	t_{HCID}	t_{DH}		2			μs
Output data hold time (vs. $\overline{CE}$ ↑)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} setup time (vs. $\overline{CE}$ ↓)	t_{SVPC}	t_{VPS}		1			ms
V_{DDP} setup time (vs. $\overline{CE}$ ↓)	t_{SVDC}	t_{VCS}		1			ms
Initial program pulse width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{WL2}	t_{OPW}		2.85		78.75	ms
NMI high voltage input setup time (vs. $\overline{CE}$ ↓)	t_{SPC}			2			μs
$\overline{OE}$ ↓ → Data output time	t_{DOOD}	t_{OE}				150	ns

Note 1: Voltage applied to P20/NMI pin.
2: Corresponding pin symbols of the μPD27C256A.

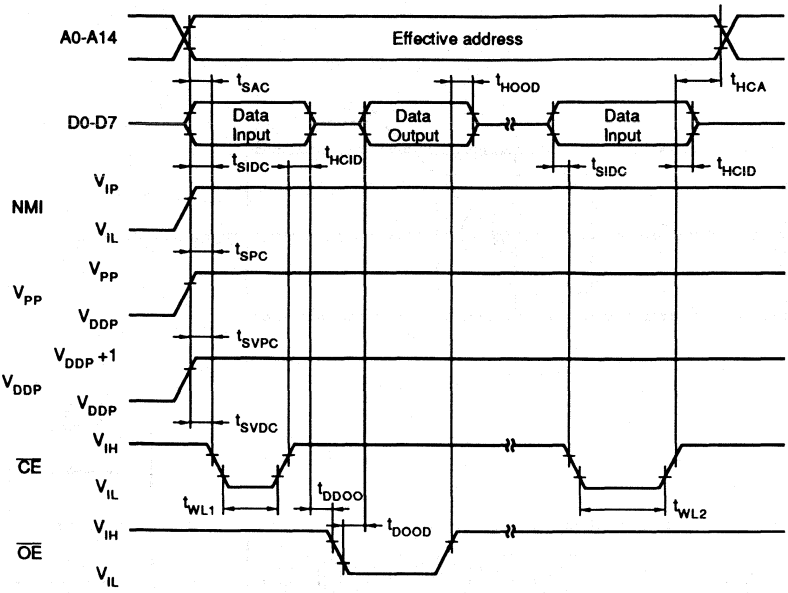
Read Operation

AC Characteristics (Ta = 25 ± 5°C, V_{IP} (Note 1) = 12.5 ± 0.5V, V_{DD} = 5 ± 0.5V, V_{PP} = V_{CC}, V_{SS} = 0V)

Parameter	Symbol	Symbol (Note 2)	Condition	Min.	Typ.	Max.	Unit
Address data output tme	t_{DAOD}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			200	ns
$\overline{CE}$ ↓ → Data ouput time	t_{DCOD}	t_{CE}	$\overline{OE}$ = V_{IL}			200	ns
$\overline{OE}$ ↓ → Data output time	t_{DOOD}	t_{OE}	$\overline{CE}$ = V_{IL}			75	ns
Data hold time (vs. $\overline{OE}$ ↑)	t_{HCOD}	t_{DF}	$\overline{CE}$ = V_{IL}	0		60	ns
Data hold time (vs. address)	t_{HAOD}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

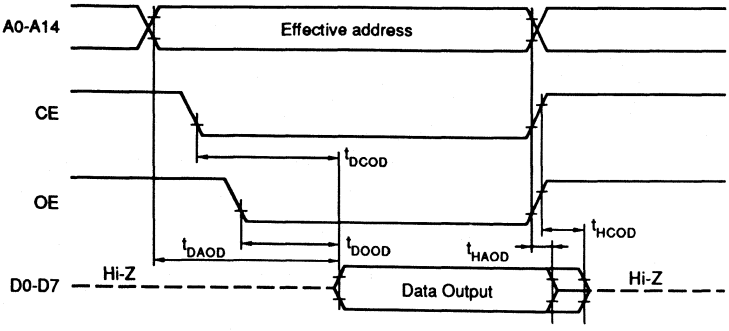
Note 1: Voltage applied to P20/NMI pin.
2: Corresponding pin symbols of the μPD27C256A.

PROM write mode timing

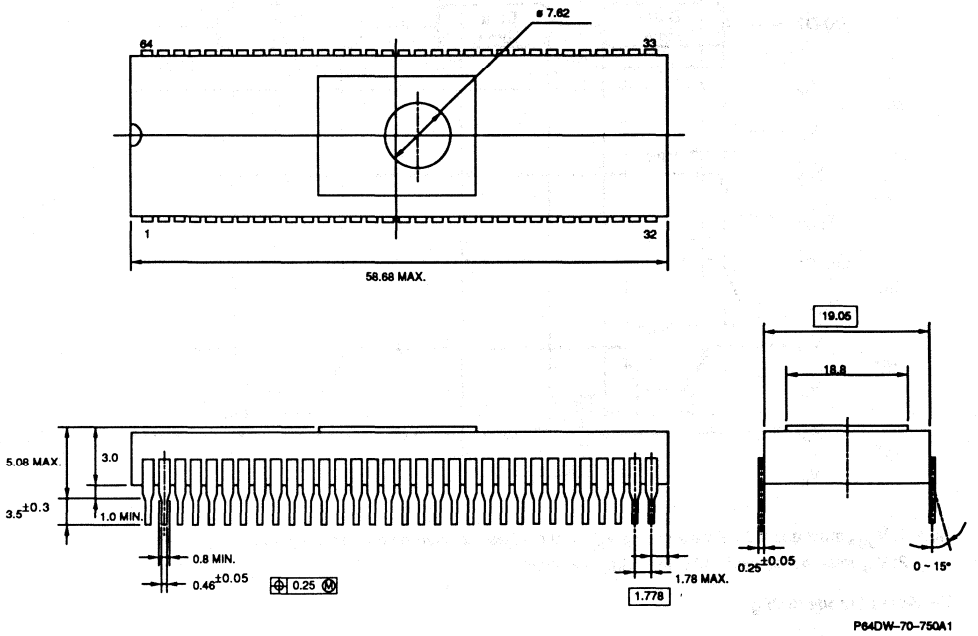


Note 1: V_{DDP} must applied before applying V_{PP}. It should be removed before removing V_{PP}.
2: V_{PP} must not exceed +13V, including overshoot.

PROM read mode timing



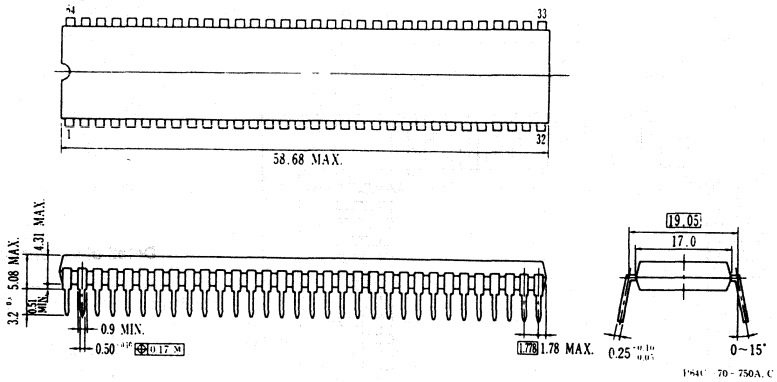
64-Pin Ceramic Shrink DIP (CERDIP) (with window) (750 mil) Configuration (Unit: mm)



P64DW-70-750A1

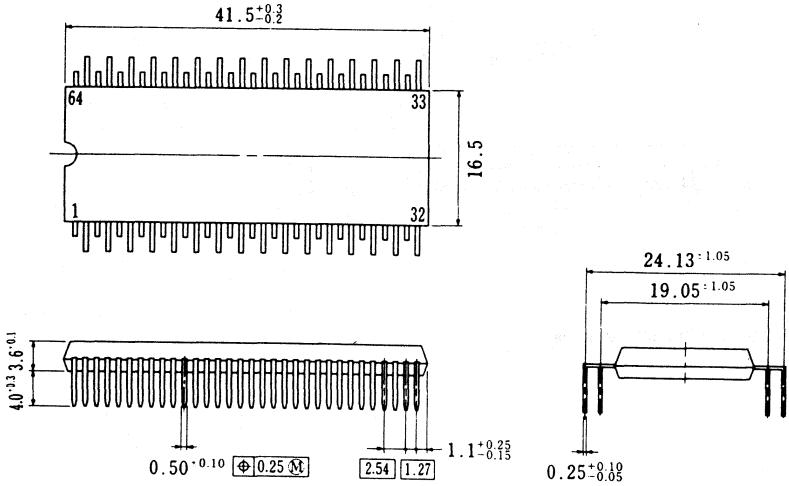
Package Dimensions

64 pin plastic shrink DIP (750mil) (Units: mm)



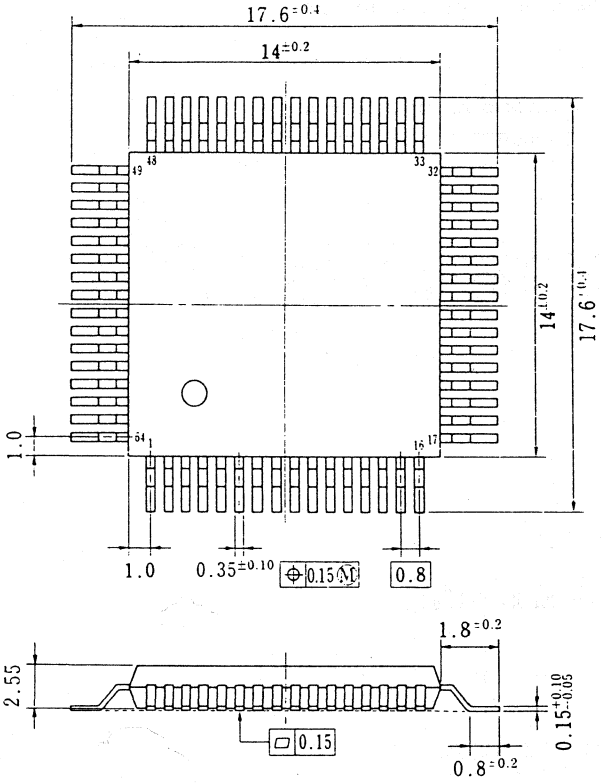
P64C-70-750A,C

64 pin plastic QUIP (Units: mm)

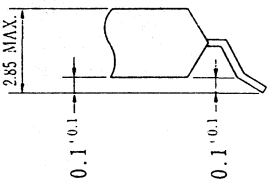


P64GQ-100-36

64-pin plastic QFP (Units: mm)



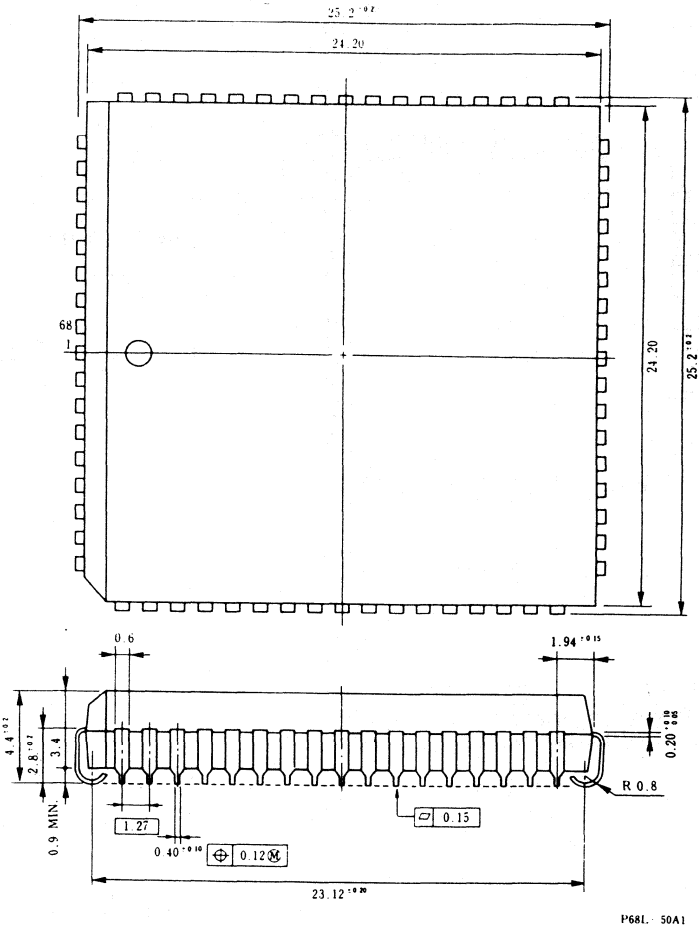
Detail of pin shape



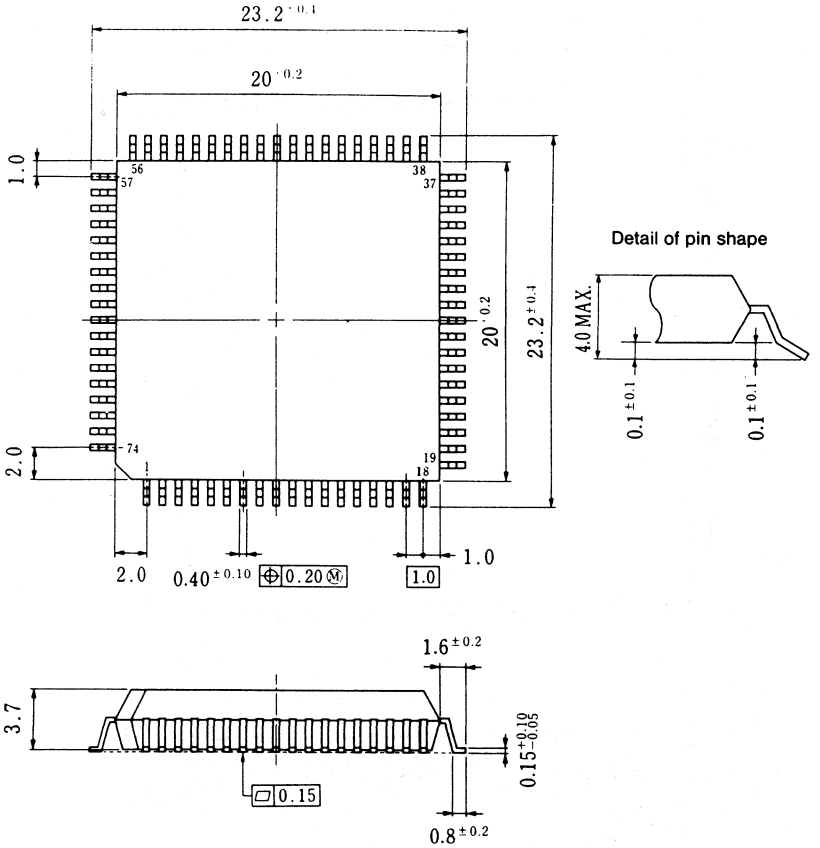
P64GC-80-AB8

Note: Small 0.8 mm pin pitch package

68 pin PLCC (Units: mm)



74-pin plastic QFP (Units: mm)



S74GJ – 100 – 5BJ

Description

The μPD78224/μPD78220 is a highly integrated, high-performance CMOS 8-bit, single-chip microcomputer which contains an 8-bit CPU (μCOM-78K/II family).
The μPD78224 has an internal 16K-byte mask ROM and 640-byte RAM; thus, the memory size of the μPD78224 can be said to be the largest among this class of microcomputers.
The μPD78220 is identical to the μPD78224 except that it has no built-in ROM, but direct-accesses external memory instead.
For prototyping and preproduction the OTP version μPD78P224 is available.

Ordering Information

Part Number	Package Type	ROM
μPD78220L	84-PIN PLCC	ROM-Less
μPD78220GJ	94-PIN QFP	
μPD78224L-xxx	84-PIN PLCC	16-K Mask ROM
μPD78224GJ-xxx	94-PIN QFP	
μPD78P224L	84-PIN PLCC	16-K OTPROM
μPD78P224GJ	94-PIN QFP	

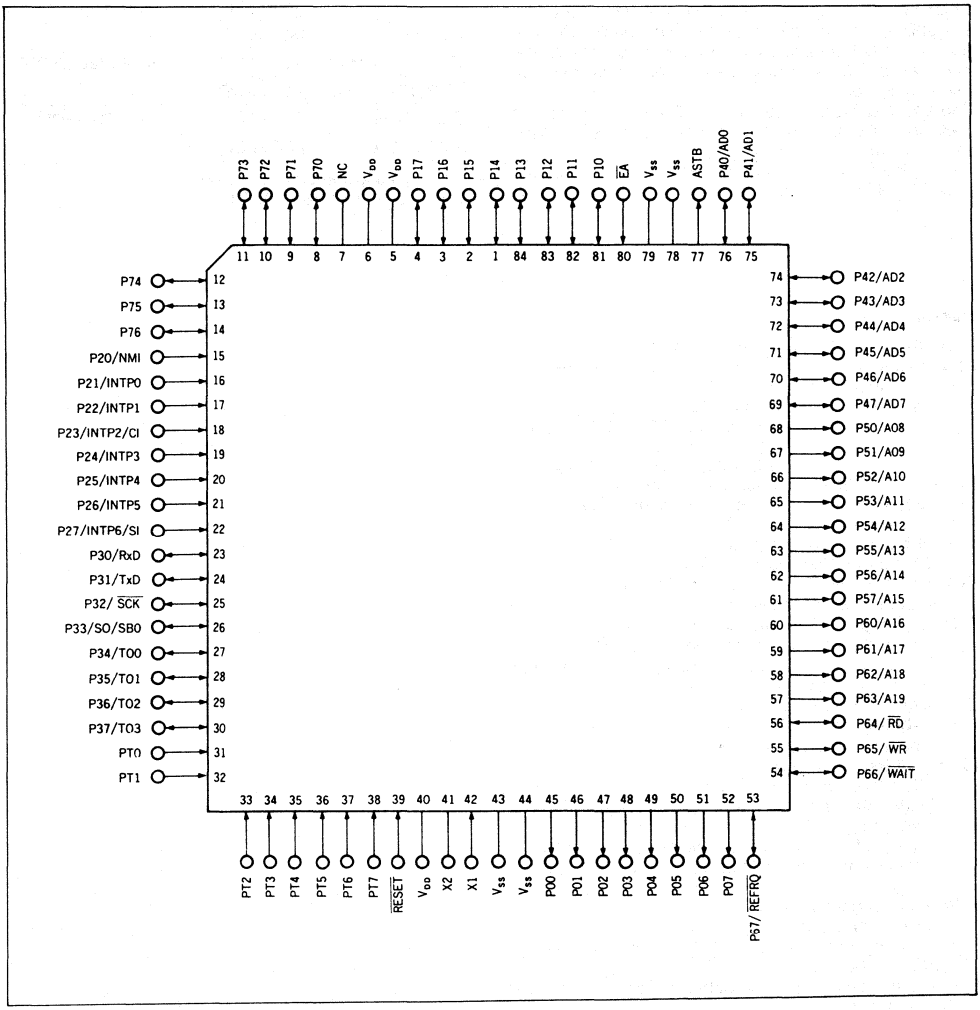
PLCC: plastic leaded chip carrier
QFP: Quad Flat Pack (SMD)

Features

- ☐ μCOM-78K/II family single-chip microcomputer
- ☐ High-speed instruction-execution time realized by employing a multi-internal bus
  - Instruction cycle: 333ns at 12MHz (with internal ROM: μPD78224)
    500ns at 12 MHz (with external ROM: μPD78220)
- ☐ Instruction set suitable for control applications
  - Multiplication/division instructions (8-bit x 8-bit, 16-bit / 8-bit)
  - 16-bit arithmetic instructions
  - Bit manipulation instructions
- ☐ A large amount of data can be handled using the 1M-byte data-memory expansion function
- ☐ Internal high-performance interrupt controller
  - Two levels of priority order (programmable)
  - Two different interrupt handling modes (vector interrupt function/macro service function)
- ☐ Multifunction timer/counter
  - 16-bit timer/counter: 1 channel
  - 8-bit timer/counter: 3 channel
- ☐ Large internal memories
  - ROM: 16K bytes (μPD78224)
  - RAM: 640 bytes
- ☐ Input/output
  - A total of 71 input pins including pins having a comparator function (the μPD78220 has 53 input pins)
- ☐ Powerful serial interface
  - UART: 1 channel
  - Clock-synchronized serial I/O (NEC standard serial bus): 1 channel
- ☐ Real-time output port capable of controlling two stepping motor systems
- ☐ CMOS
- ☐ Single power supply

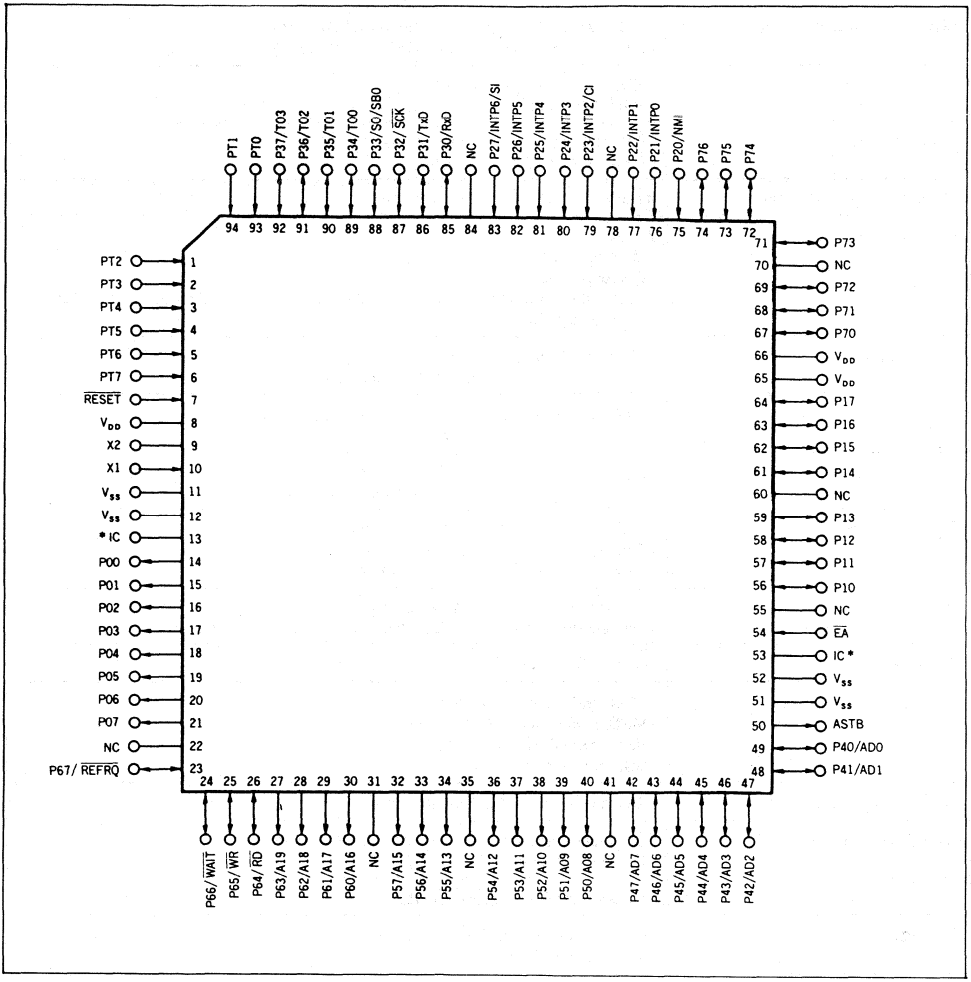
Pin Configuration

84-Pin PLCC (Top View)



Pin Configuration

94-Pin QFP (Top View)



*Note: IC has to be connected to V_{SS}

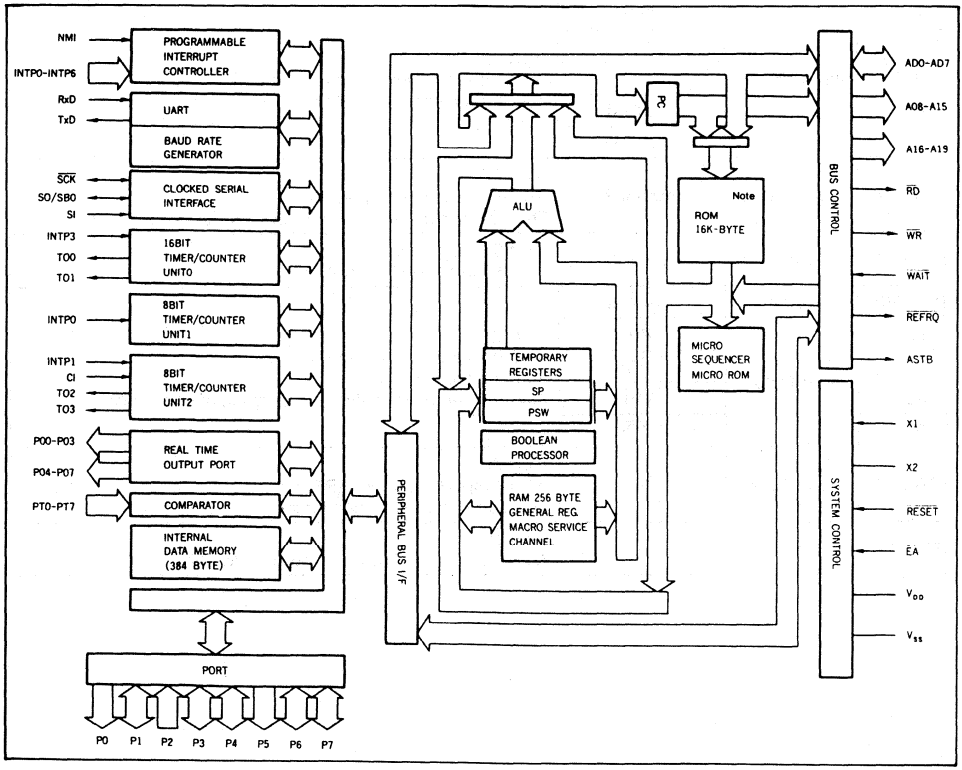
Functions table

Function	Description
Number of instructions	65
Minimum instruction-execution time	• 333ns at 12MHz (with external ROM: μPD78224) • 500ns at 12MHz (with external ROM: μPD78224)
Built-in Memory	• ROM: 16k bytes (μPD78224) • RAM: 640 bytes
Address space	• Program memory space: 64k bytes • Data memory space: 1M bytes
General purpose register	8 bits x 8 x 4 banks (memory mapped)
I/O lines	71 total • Input port pins : 8 • Output port pins : 20 • Input/output port pins : 35 (Of these 20, 8 are capable of directly drive LEDs) • With comparator : 8
Timer/counter	• 16-bit timer/counter: Capture register: 1 Compare register: 2
	• 8-bit timer/counter 1: Capture/compare register: 1 Compare register: 1
	• 8-bit timer/counter 2: Capture register: 1 Compare register: 2
Serial interface	• UART : 1 channel • Clock-synchronized serial I/O : 1 channel • Exclusive internal baud rate generator
Interrupts	• 17 interrupt sources (External: 8, Internal: 9) • Two interrupt-handling modes (Vector interrupt/macro service)
Stand-by	HALT/STOP mode
Powerful instruction set	• 16-bit arithmetic instructions • Multiplication/devision instructions • Bit manipulation instructions • BCD adjust instructions
Inputs with comparator	4-bit precision, variable threshold level
Real-time output ports	Port output function interlocked with the internal timer • Two 4-bit channels
Other	Pseudo-static RAM refresh function
Package	• 84-pin PLCC (Plastic Leaded Chip Carrier) • 94-pin plastic QFP

P00-P07	:	Port 0	$\overline{SCK}$	:	Serial Clock
P10-P17	:	Port 1	SB0	:	Serial Bus
P20-P27	:	Port 2	SI	:	Serial Input
P30-P37	:	Port 3	SO	:	Serial Output
P40-P47	:	Port 4	NMI	:	Nonmaskable Interrupt
P50-P57	:	Port 5	INTP0-INTP6	:	Interrupt from Peripherals
P60-P67	:	Port 6	AD0-AD/	:	Address Data Bus
P70-P77	:	Port 7	A08-A15	:	A16-A19 : Address Bus
PT0-PT7	:	Port T	$\overline{RD}$	:	Read Strobe
TO0-TO3	:	Timer Output	$\overline{WR}$	:	Write Strobe
CI	:	Clock Input	$\overline{WAIT}$	:	Wait
RxD	:	Receive Data	ASTB	:	Address Strobe
TxD	:	Transmit Data	$\overline{EA}$	:	External Access
X1, X2	:	Crystal			
$\overline{REFRQ}$	:	Refresh Request			
$\overline{RESET}$	:	Reset			
NC	:	Non-connection			
IC	:	Internally Connected			

2

Block Diagram



Note: μPD78220 is without the 16K ROM

Pin Functions

1. Ports

Pin name	Input/output	Dual function pin	Function
P00-P07	Output	–	(Port 0) An 8-bit output-only port (P0). This port can also be used as an 8-bit real-time output port or as two 4-bit real-time output ports.
P10-P17	Input/Output	–	(Port 1) An 8-bit input/output port (P1). This port can be specified for input/output in bit units.
P20	Input	NMI	(Port 2) An 8-bit input-only port (P2).
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24-P26		INTP3-INTP5	
P27		INTP6/SI	
P30	Input/Output	RxD	(Port 3) An 8-bit special input/output port (P3). This port can bei specified for input/output in bit units.
P31		TxD	
P32		$\overline{SCK}$	
P33		SO/SB0	
P34-P37		TO0-TO3	
P40-P47	Input/Output	AD0-AD7	(Port 4) An 8-bit input/output port (P4). This port can be specified for input/output in 8-bit units.
P50-P57	Output	A08-A15	(Port 5) An 8-bit output-only port (P5).
P60-P63	Output	A16-A19	(Port 6) An 8-bit input/output port (P6). P60-P63 are output only. P64-P67 can be specified for input/output in bit units.
P64	Input/Output	$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$	
P67		$\overline{REFRQ}$	
P70-P76	Input/Output	–	(Port 7) A 7-bit input/output port (P7). This port can be specified for input/output in bit units.
PT0-PT7	Input	–	(Port T) An 8-bit input-only port with comparator (PT).

2. Others than Ports

Pin name	Input/output	Dual function pin	Function
TO0-TO3	Output	P34/P37	Timer output pin.
CI	Input	P23/INTP2	8-bit timer/counter No. 2 external clock input pin.
RxD	Input	P30	Serial data input pin.
TxD	Output	P31	Serial data output pin.
SCK	Output	P32	Serial clock input/output pin.
SB0	Input/Output	P33/SO	Serial data input/output pin (SBI mode).
SI	Input	P27/INTP6	Serial data input pin (3-line serial I/O mode).
SO	Output	P33/SB0	Serial data output pin (3-line serial I/O mode).
NMI	Input	P20	Non-maskable interrupt request input pin for which the rising or falling edge can be specified as the detection edge by the mode register.
INTP0	Input	P21	External interrupt request input pin for which the effective edge can be specified by the mode register.
INTP1		P22	
INTP2		P23/CI	
INTP3-INTP5		P24-P26	
INTP6		P27/SI	
AD0-AD7	Input/Output	P40-P47	Time-division multiplexed address/data bus (when the external memory is connected).
A08-A15	Output	P50-P57	Address output port (when the external memory is connected).
A16-A19	Output	P60-P63	Upper address output pin (when the external memory is expanded).
$\overline{RD}$	Output	P64	Strobe signal output pin for external memory read operation.
$\overline{WR}$	Output	P65	Strobe signal output pin for external memory write operation.
$\overline{WAIT}$	Input	P66	Wait signal input pin.
ASTB	Output	–	This pin outputs a timing signal to externally latch the address information for accessing the external memory.
$\overline{EA}$	Input	–	Normally, the $\overline{EA}$ pin is set to 1 (high). When the EA pin is set to 0 (low), the ROM-less mode is initiated, and the external memory is accessed.
X1, X2		–	A crystal for the system clock is connected across these pins. The X1 pin is used to input the external clock.
$\overline{REFRQ}$	Output	P67	When a pseudo-static memory is externally connected, this pin is used to output the refresh pulse to the pseudo-static memory.
$\overline{RESET}$	Input	–	Low-level-active system reset input pin.
V_{DD}		–	Positive power supply pin.
V_{SS}		–	GND
NC		–	Unused
IC		–	Internal connection pin. Connect this pin to V_{SS} (GND).

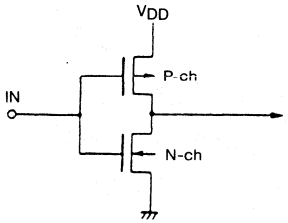
I/O Circuits
The type of I/O circuit of each pin and recommended connections for unused pins are shown in following table. The different types of I/O circuits are shown afterwards.

Input/Output types of each pin and what to do when not used:

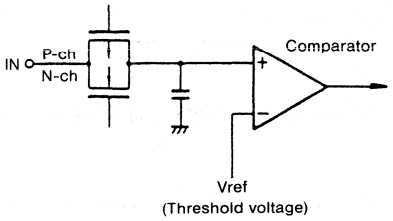
Pin	I/O Type	Input/Output	Recommended connection when not used
P00-P07	4	Output	No connection required
P10-P17	5	Input/Output	Connect to V_{DD} with pull-up resistor
P20/NMI	2	Input	
P21/INTP0			
P22/INTP1			
P23/INTP2/CI			
P24/INTP3-P26/INTP5			
P27/INTP6/SI			
P30/RxD	5	Input/Output	
P31/TxD			
P32/$\overline{SCK}$	8		
P33/SO/SB0	9		
P34/TO0-TO3	5		
P40/AD0-P47/AD7			
P50/A08-P57/A15	4	Output	No connection required
P60/A16-P63/A19			
P64/$\overline{RD}$	5	Input/Output	Connect to V_{DD} with pull-up resistor
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/$\overline{REFRQ}$			
P70-P76			
PT0-PT7	7	Input	Connect to V_{DD} or V_{SS}
ASTB	4	Output	No connection required
$\overline{EA}$	1	Input	–
$\overline{RESET}$	2	Input	–

Pin I/O Circuits

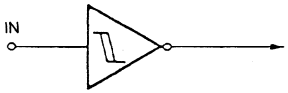
TYPE 1



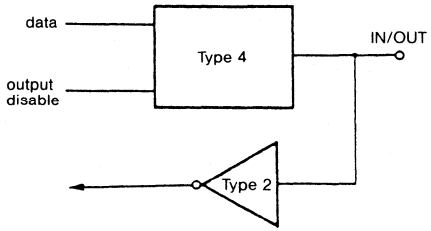
TYPE 7



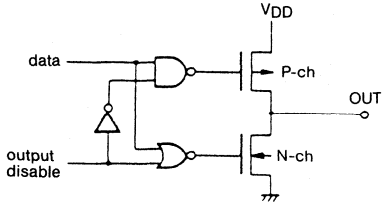
TYPE 2



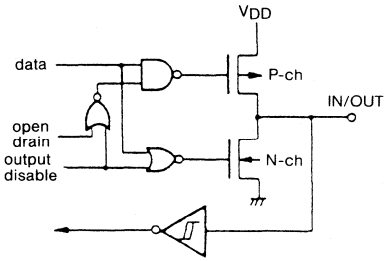
TYPE 8



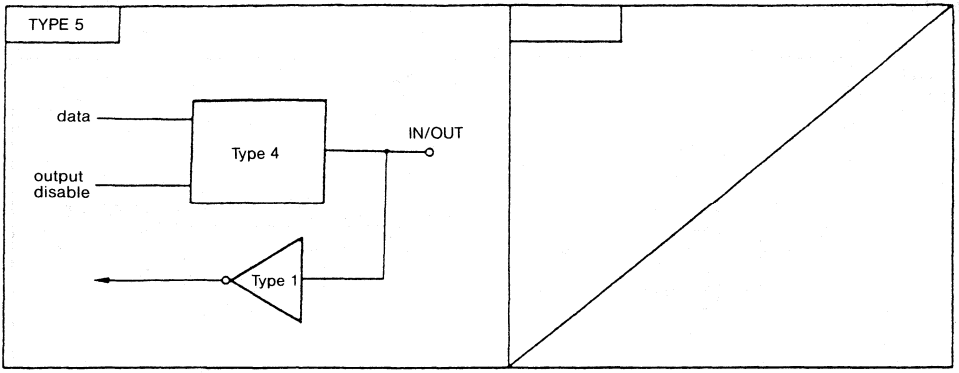
TYPE 4



TYPE 10



2


TYPE 5
data
output
disable
Type 4
IN/OUT
Type 1

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Condition	Ratings	Unit
Power Supply Voltage	V_{DD}		− 0.5 to + 7.0	V
Input Voltage	V_I		− 0.5 to V_{DD} + 0.5	V
Output Voltage	V_O		− 0.5 to V_{DD} + 0.5	V
High Level Output Current	I_{OH}	One Output Pin	− 2	mA
		All Output Pin Total	− 50	mA
Low Level Coutput Current	I_{OL}	One Output Pin	Peak 30	mA
			Average 15	mA
		All Output Pin Total	Peak 150	mA
			Average 100	mA
Operating Temparature	T_{OPT}		− 40 to + 85	°C
Storage Temparature	T_{STG}		− 65 to + 150	°C

2

Recommended Operating Conditions

Parameter	Ta	V_{DD}
OSC frequency 4 MHz ≦ f_{XTAL} ≦ 12 MHz	− 40°C to + 85°C	+ 5.0 V ± 5%
	− 10°C to + 70°C	+ 5.0 V ± 10%

Capacitance (Ta = 25°C, V_{DD} = V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Capacitance	C_I	f_C = 1 MHz			20	pF
Output Capacitance	C_O	Unmeasured Pins			20	pF
In/Output Capacitance	C_{IO}	Returned to 0V			20	pF

DC Characteristics

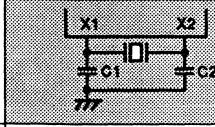
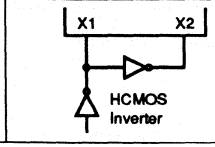
$T_a = -10°C$ to $+70°C$, $V_{DD} = +5.0V \pm 10\%$, $V_{SS} = 0V$
$T_a = -40°C$ to $+85°C$, $V_{DD} = +5.0V \pm 5\%$, $V_{SS} = 0V$

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	except PTn		0		0.8	V
Input High Voltage	V_{IH1}	except note 1 and PTn		2.2		V_{DD}	V
	V_{IH2}	note 1 Pins		0.8 V_{DD}		V_{DD}	V
Output Low Voltage	V_{OL1}	$I_{OL} = 2.0$ mA				0.45	V
	V_{OL2}	$I_{OL} = 8.0$ mA, Port 1				1.0	V
Output High Voltage	V_{OH1}	$I_{OH} = -1.0$ mA		$V_{DD}-1.0$			V
	V_{OH2}	$I_{OH} = -100$ μA		$V_{DD}-0.5$			V
Input Leak. Current	I_{LI}	$0V \leqq V_I \leqq V_{DD}$				±10	μA
Output Leak. Current	I_{LO}	$0V \leqq V_O \leqq V_{DD}$				±10	μA
Pull-up current	I_{IPT}	V_I (PT pin) = 0V			−150	−400	μA
V_{DD} power supply current	I_{DD1}	Operating mode, $f_{XX} = 12$ MHz			16	40	mA
	I_{DD2}	HALT mode, $f_{XX} = 12$ MHz			7	20	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5		5.5	V
Data retention current	I_{DDDR}	STOP mode	$V_{DDDR} = 2.5$ V		2	20	μA
			$V_{DDDR} = 5V \pm 10\%$		5	50	μA

Note: X1, X2, $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4, P26/INTP5, P27/INTP6/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0, and $\overline{\text{EA}}$ pins.

Oscillator Characteristics

Ta=–10°C to +70°C, V_{DD}=+5.0V ±10%, V_{SS}=0V
Ta=–40°C to +85°C, V_{DD}=+5.0V ±5%, V_{SS}=0V

Resonator	Recommended Circuit	Parameter	MIN.	MAX.	Units
Ceramic or crystal resonator (Note)		Oscillation frequency (f_{XX})	4	12	MHz
External Clock		X1 Input frequency (f_X)	4	12	MHz
		X1 input rise, fall time (tr, tf)	0	30	ns
		X1 input high, low level range (t_{OH}, t_{OL})	30	130	ns

Note 1: Oscillator circuit must be positioned as close as possible to the X1 and X2 pins.
2: No other signal line must be wired within the shaded area.

Crystal Oscillators (Ta = –40°C to +85°C)

Manufacturer	Product name	Frequency (MHz)	Recommended circuit constants (pF)	
			C1	C2
Kinseki	HC-18/U	12	27	27
	HC-43/U			
	HC-49/U (Note)			

Note: When HC-49/U is used, the operation temperature range is Ta = –20°C to +70°C.

Ceramic Oscillator (Ta = –40°C to +85°C)

Manufacturers	Product Types	Recommended Capacitors	
		C1 (pF)	C2 (pF)
Murata	CSA10.0MT040	100	100
	CSA12.0MT040 (Note)	100	100
Kyocera (Kyoto Ceramic)	KBR-10.0M	33	33

Note: When CSA12, OMT040 is used, the operation temperature range is –20°C to +85°C.

AC Characteristics
$T_a = -10°C$ to $+70°C$, $V_{DD} = +5.0V \pm 10\%$, $V_{SS} = 0V$
$T_a = -40°C$ to $+85°C$, $V_{DD} = +5.0V \pm 5\%$, $V_{SS} = 0V$
Read/write operation

Parameter	Symbol	Conditiones	MIN.	MAX.	Units
X1 input clock cycle time	t_{CYX}		82	250	ns
Address set up time (against ASTB↓)	t_{SAST}		52		ns
Address hold time (against ASTB↓)	t_{HSTA}	$R_L = 5K\Omega$, $C_L = 50pF$	25		ns
Address → $\overline{RD}$↓ delay time	t_{DAR}		129		ns
Address float time (against $\overline{RD}$↓)	t_{FAR}		11		ns
Address → data input time	t_{DAID}			228	ns
ASTB↓ → data input time	t_{DSTID}			181	ns
$\overline{RD}$↓ → data input time	t_{DRID}			99	ns
ASTB↓ → $\overline{RD}$↓ delay time	t_{DSTR}		52		ns
Data hold time (against $\overline{RD}$↑)	t_{HRID}		0		ns
$\overline{RD}$↑ → address active time	t_{DRA}		124		ns
$\overline{RD}$↑ → ASTB↑ delay time	t_{DRST}		124		ns
$\overline{RD}$ low level width	t_{WRL}		124		ns
ASTB high level width	t_{WSTH}		52		ns
Address → $\overline{WR}$↓ delay time	t_{DAW}		129		ns
ASTB↓ → data output time	t_{DSTOD}			142	ns
$\overline{WR}$↓ → data output time	t_{DWOD}			60	ns
ASTB↓ → $\overline{WR}$↓ delay time	t_{DSTW1}		52		ns
	t_{DSTW2}	Refresh mode	129		ns
Data set up time (against $\overline{WR}$↑)	t_{SODWR}		146		ns
Data set up time (against $\overline{WR}$↓) Note 1	t_{SODWF}	Refresh mode	22		ns
Data hold time (against $\overline{WR}$↑) Note 2	t_{HWOD}		20		ns
$\overline{WR}$↑ → ASTB↑ delay time	t_{DWST}		42		ns
$\overline{WR}$ low level width	t_{WWL1}		196		ns
	t_{WWL2}	Refresh mode	114		ns
Address → $\overline{WAIT}$↓ input time	t_{DAWT}			146	ns
$\overline{ASTB}$ → WAIT↓ input time	t_{DSTWT}			84	ns
$\overline{WAIT}$ hold time (against X1↓)	t_{HWTX}		0		ns
$\overline{WAIT}$ set up time (against X1↑)	t_{SWTX}		0		ns

Remarks: Values in the table are for fxx = 12MHz, $C_L = 100pF$.
Note 1: When accessing a pseudo-static RAM (μPD4168, etc.) which clocks in data at the falling edge of the $\overline{WR}$ signal, use t_{SODWF} instead of t_{SODWR} as the data set up time.
Note 2: The hold time includes the time during which V_{OH} and V_{OL} are retained under the following load conditions; $C_L = 100pF$ and $R_L = 2k\Omega$.

Serial operation

Parameter	Symbol	Conditiones		MIN.	MAX.	Units
Serial clock cycle time	t_{CYSK}	Input	External clock	1.0		μs
		Output	Internal clock/16	1.2		μs
			Internal clock/64	4.8		μs
Serial clock low level width	t_{WSKL}	Input	External clock	420		ns
		Output	Internal clock/16	500		ns
			Internal clock/64	2.0		μs
Serial clock high level width	t_{WSKH}	Input	External clock	420		ns
		Output	Internal clock/16	500		ns
			Internal clock/64	2.0		μs
SI, SB0 set up time to $\overline{SCK}$↑	t_{SSSK}			150		ns
SI, SB0 hold time after $\overline{SCK}$↑	t_{HSSK}			400		ns
SO/SB0 output delay time to $\overline{SCK}$↓	t_{DSBSK1}	CMOS push-pull output (3-line serial I/O mode)		0	300	ns
	t_{DSBSK2}	Open-drain output (SBI mode), $R_L = 1K\Omega$		0	800	ns
SB0 low set up time to $\overline{SCK}$ ↓	t_{HSBSK}	SBI mode		2		t_{CYX}
SB0 high hold time to $\overline{SCK}$ ↑	t_{SSBSK}			2		t_{CYX}
SB0 low level width	t_{WSBL}			4		t_{CYX}
SB0 high level width	t_{WSBH}			4		t_{CYX}

Note: This table shows the values for fxx = 12MHz, C_L = 100pF.

Other operation

Parameter	Symbol	Conditiones	MIN.	MAX.	Units
NMI low level width	t_{WNIL}		10		μs
NMI high level width	T_{WNIH}		10		μs
INTP0-INTP6 low level width	t_{WITL}		24		t_{CYX}
INTP0-INTP6 high level width	t_{WITH}		24		t_{CYX}
$\overline{RESET}$ low level width	t_{WRSL}		10		μs
$\overline{RESET}$ high level width	t_{WRSH}		10		μs

External clock timing

Parameter	Symbol	Conditiones	MIN.	MAX.	Units
X1 input low level width	t_{WXL}		30	130	ns
X1 input high level width	T_{WXH}		30	130	ns
X1 input rise time	t_{XR}		0	30	ns
X1 input fall time	t_{XF}		0	30	ns
X1 input clock cycle time	t_{CYX}		82	250	ns

Comparator characteristics
$T_a = -10\,°C$ to $+70\,°C$, $V_{DD} = +5.0V \pm 10\%$, $V_{SS} = 0V$
$T_a = -40\,°C$ to $+85\,°C$, $V_{DD} = +5.0V \pm 5\%$, $V_{SS} = 0V$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Comparison accuracy	V_{ACOMP}				100	mV
Comparison time	t_{COMP}		128		256	t_{CYX}
Sampling time	t_{SAMP}		62			t_{CYX}
PT input voltage	V_{IPT}		0		V_{DD}	V

Definition of bus timing depending on t_{CYX}

Parameter	Symbol	Calculation formula	MIN./ MAX.	12 MHz	Units
X1 input cycle time	t_{CYX}		MIN.	82	ns
Address set up time to ASTB↓	t_{SAST}	$t_{CYX}-30$	MIN.	52	ns
Address to $\overline{RD}$↓ delay time	t_{DAR}	$2t_{CYX}-35$	MIN.	129	ns
Address float to $\overline{RD}$↓ time	t_{FAR}	$t_{CYX}/2-30$	MIN.	11	ns
Address to data input time	t_{DAID}	$(4+2n)t_{CYX}-100$	MAX.	228	ns
ASTB↓ to data input time	t_{DSTID}	$(3+2n)t_{CYX}-65$	MAX.	181	ns
$\overline{RD}$↓ to data input time	t_{DRID}	$(2+2n)t_{CYX}-65$	MAX.	99	ns
ASTB↓ to $\overline{RD}$↓ delay time	t_{DSTR}	$t_{CYX}-30$	MIN.	52	ns
$\overline{RD}$↑ to address active time	t_{DRA}	$2t_{CYX}-40$	MIN.	124	ns
$\overline{RD}$↑ to ASTB↑ delay time	t_{DRST}	$2t_{CYX}-40$	MIN.	124	ns
$\overline{RD}$ low level width	t_{WRL}	$(2+2n)t_{CYX}-40$	MIN.	124	ns
ASTB high level width	t_{WSTH}	$t_{CYX}-30$	MIN.	52	ns
Address to $\overline{WR}$↓ delay time	t_{DAW}	$2t_{CYX}-35$	MIN.	129	ns
ASTB↓ to data output time	t_{DSTOD}	$t_{CYX}+60$	MAX.	142	ns
ASTB↓ to $\overline{WR}$↓ delay time	t_{DSTW1}	$t_{CYX}-30$	MIN.	52	ns
	t_{DSTW2}	$2t_{CYX}-35$ (Refresh mode)	MIN.	129	ns
Data set up time to $\overline{WR}$↑	t_{SODWR}	$(3+2n)t_{CYX}-100$	MIN.	146	ns
Data set up time to $\overline{WR}$↓	t_{SODWF}	$t_{CYX}-60$ (Refresh mode)	MIN.	22	ns
$\overline{WR}$↑ to ASTB↑ delay time	t_{DWST}	$t_{CYX}-40$	MIN.	42	ns
$\overline{WR}$ low level width	t_{WWL1}	$(3+2n)t_{CYX}-50$	MIN.	196	ns
	t_{WWL2}	$(2+2n)t_{CYX}-50$ (Refresh mode)	MIN.	114	ns
Address to $\overline{WAIT}$↓ input time	t_{DAWT}	$3t_{CYX}-100$	MAX.	146	ns
ASTB↓ to $\overline{WAIT}$↓ input time	t_{DSTWT}	$2t_{CYX}-80$	MAX.	84	ns

Remarks: n indicates the number of WAIT states.

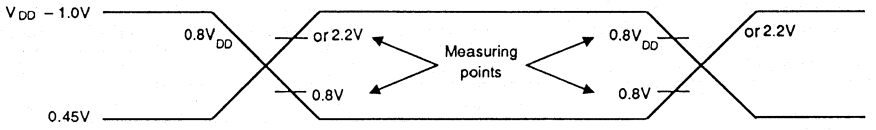
Data Retention Characteristics
Ta = −10°C to +70°C, V_{DD} = +5.0V ±10%, V_{SS} = 0V
Ta = −40°C to +85°C, V_{DD} = +5.0V ±5%, V_{SS} = 0V

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Units
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	V_{DDDR}=2.5V		2	20	μA
		V_{DDDR} = 5V ±10% Ta = −10 to +70°C		5	20	μA
		V_{DDDR}=5V±10%		5	50	μA
V_{DD} rise time	t_{RVD}		200			μs
V_{DD} fall time	t_{FVD}		200			μs
V_{DD} retention time (for STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stabilize wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Low level input voltage	V_{IL}		0		$0.1V_{DDDR}$	V
High level input voltage	V_{IH}		$0.9V_{DDDR}$		V_{DDDR}	V

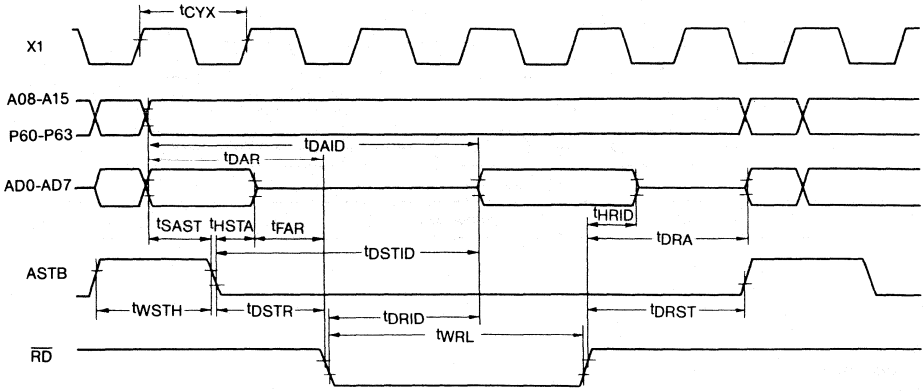
Note: $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4, P26/INTP5, P27/INTP6/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0, and $\overline{\text{EA}}$ Pins.

2

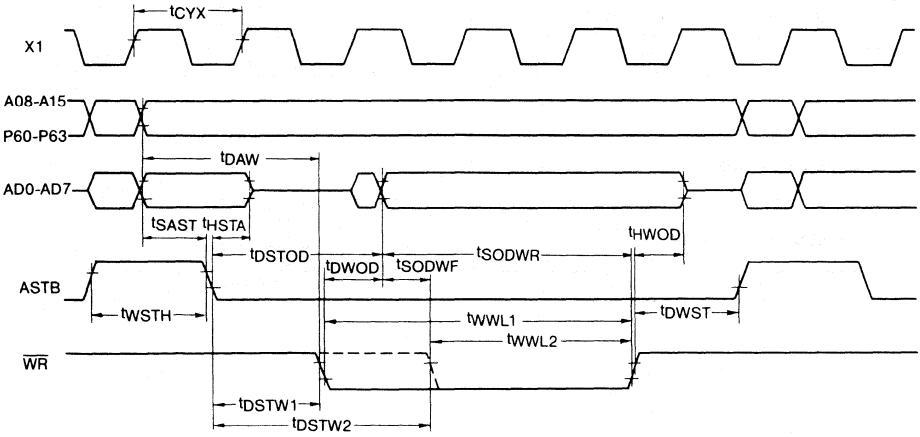
AC timing measurement points



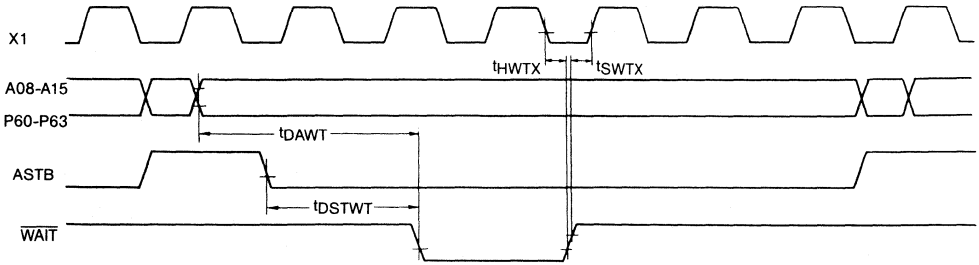
Timing Wave-Forms
Read Operation



Write Operation

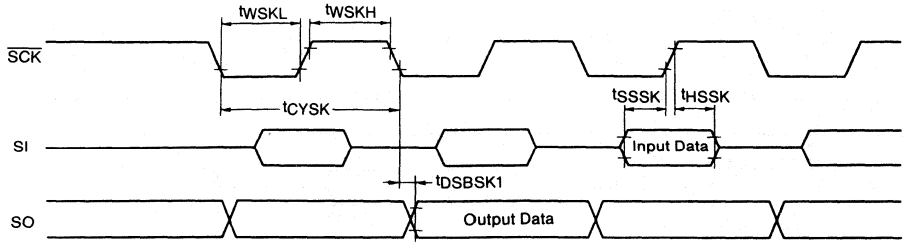


External Wait Input

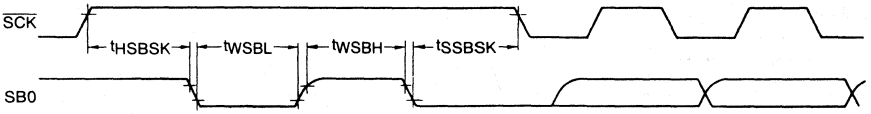


2

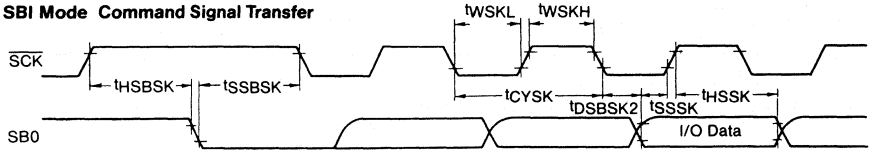
Serial Operation
3-Line Serial I/O Mode



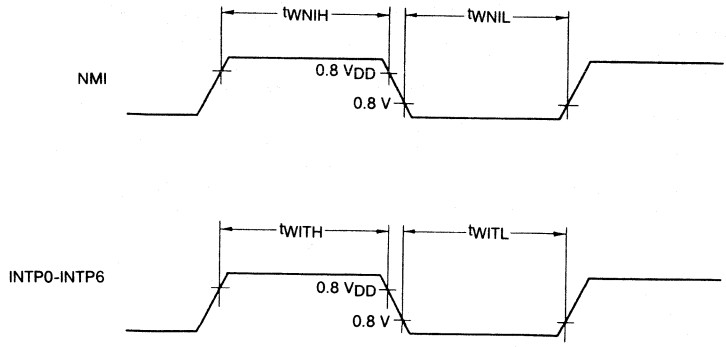
SBI Mode
Bus Release Signal Transfer



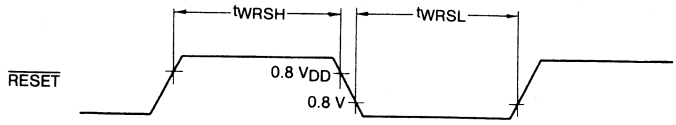
SBI Mode Command Signal Transfer



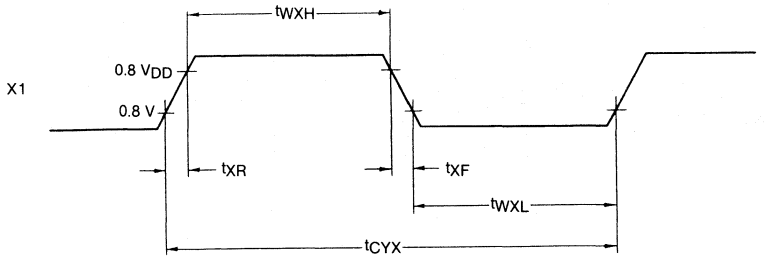
Interrupt Input Timing



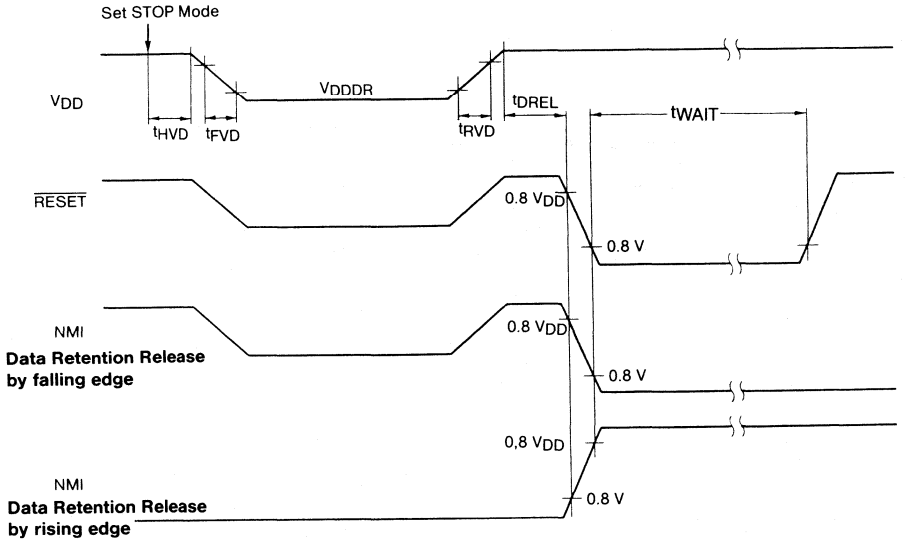
Reset Input Timing



External Clock Timing

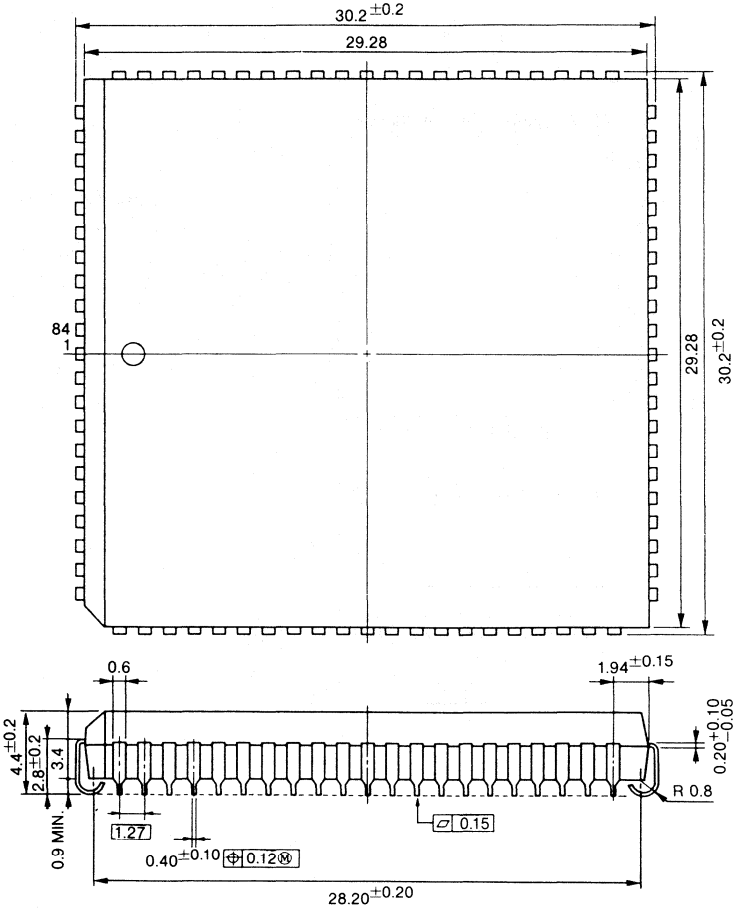


Data Retention Timing



Package Dimensions (unit: mm)

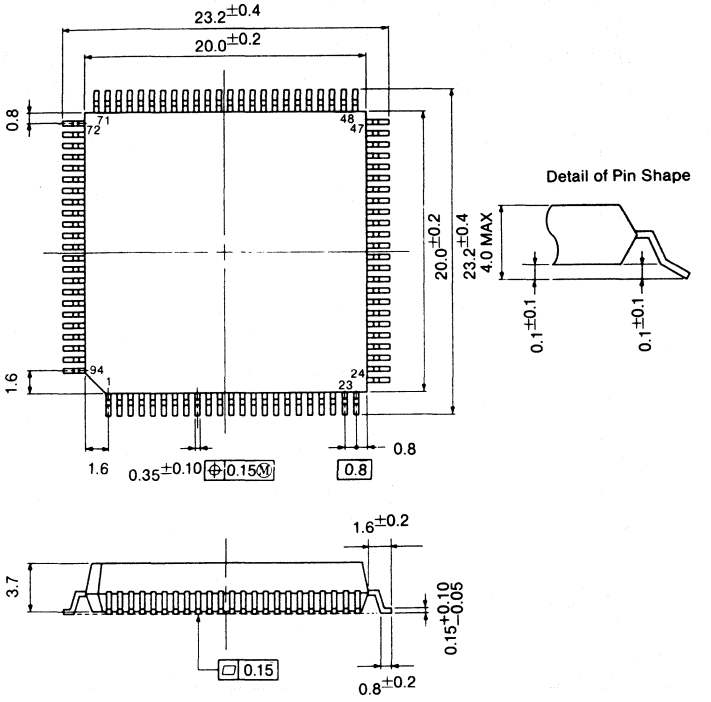
84-PIN PLCC



P84L-50A3

Package Dimensions (unit: mm)

94-PIN FLAT (QFP)



S94GJ-80-5BG

Recommended Soldering Conditions

For the μPD78220/μPD78224,soldering must be performed under the following conditions. For other soldering methods, please consult with NEC sales personnel.

(1) μPD78220L, μPD78224L–xxx

Method	Condition	Remarks
VPS (Note 1)	Peak temperature: 215°C, one time	Pre-baking required (Note 2)
Pin partial heating	300°C max. , 10 seconds max.	

Note 1: Vapor phase soldering
2: 4 hours min. at 125°C or 48 hours min. at 70°C.
For aluminum dry packing product, pre-baking is not necessary when mounting within 48 hours after unpacking.

Note: Do not dip soldering μPD78220L/μPD78224L–xxx or use infra-red soldering.

(2) μPD782240GJ–5BG, μPD78224GJ–xxx–5BG

Method	Condition
Pin partial heating	300°C max. , 10 seconds max.

Note: Do not dip solder μPD78220GF–5BG/μPD78224GJ–xxx–5BG or use infra-red, or VPS soldering.

2

Description

The μPD78P224 is a version of the μPD78224 in which the built-in mask ROM is replaced with a one-time PROM. Consequently a program can be written to the μPD78P224 by the user, thus making it possible to evaluate the μPD78224 when developing a system or when making limited production runs. Use this data sheet together with the μPD78220/224 data sheet.

Features

- μPD78224–compatible
- Built-in one-time PROM: 16,384 x 8 bits
- PROM programming characteristics:
  μPD27C256A–compatible can be programmed using a general purpose PROM writer

Ordering Information

Order code	Package	ROM
μPD78P224GJ	94-PIN QFP	16-K OTPROM
μPD78P224L	84-PIN PLCC	

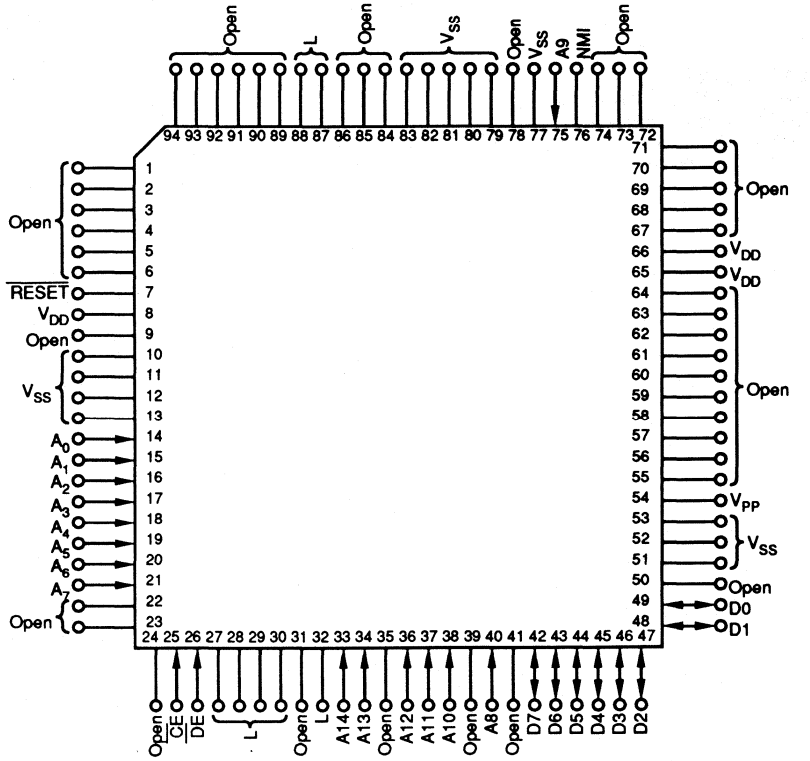
QFP: Quad Flat Pack (SMD)
PLCC: Plastic Leaded Chip Carrier

Pin Configuration (top view)

For pin configurations in Normal Mode operation and corresponding pin functions tables, please refer to μPD78220/224 data sheet.

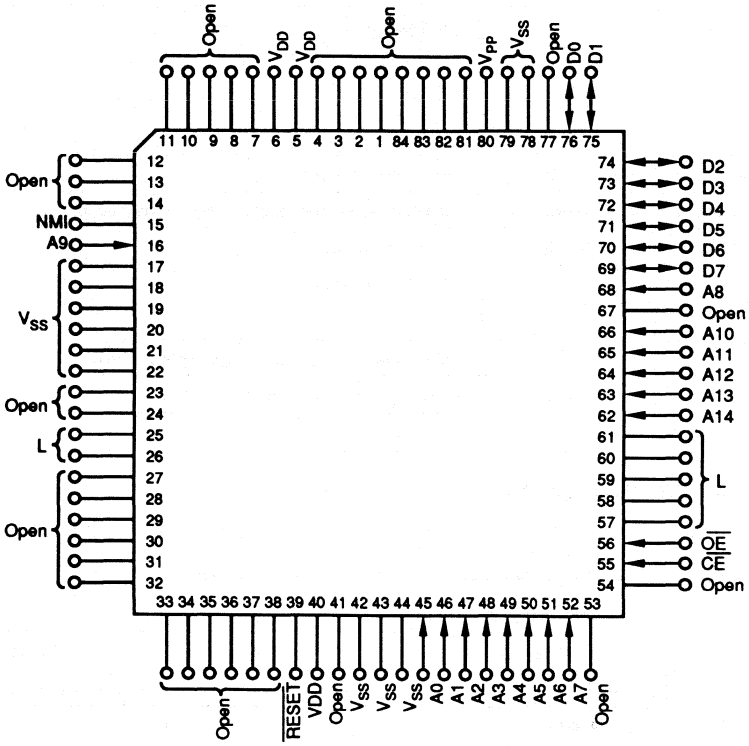
Pin Configuration in PROM programming mode

(a) 94-pin plastic QFP



Notes: 1. L : Individually connect to V_{SS} through a pull-down resistor.
2. V_{SS} : Connect to GND.
3. Open : Leave unconnected.
4. $\overline{RESET}$: Set to low level.
5. NMI : Set to +12.5V.

(b) 84-pin PLCC



Notes: 1. L : Individually connect to V_{SS} through a pull-down resistor.
2. V_{SS} : Connect to GND.
3. Open : Leave unconnected.
4. $\overline{RESET}$: Set to low level.
5. NMI : Set to +12.5V.

Pin Functions in PROM Programming Mode

Pin Name	Input/Output	Shared pin*	Function
A0-A7	Input	P00-P07	Address input pin
A8		P50	
A9		P21/INTP0	
A10-A14		P52-P56	
D0-D7	Input/Output	P40-P47/AD0-AD7	Data input/output pin
CE	Input	P65/WR	Chip enable input pin/programmable pulse input pin
OE	Input	P64/RD	Output enable input pin
NMI		P20	PROM mode set pin
$\overline{\text{RESET}}$		—	
V_{PP}		$\overline{\text{EA}}$	Program write/verify high voltage application pin
V_{DD}		—	Positive power supply pin
V_{SS}		—	GND

Difference Between μPD78P224 and μPD78224, 78220

The μPD78P224 is a version of the μPD78224 of which the built-in mask ROM is replaced with a one-time PROM. Table 2-1 shows the differences between these three products.
For details concerning the CPU and built-in hardware, refer to the μPD78224 user's manual.

Differences between μPD78P224 and μPD78224, 78220

Item	μPD78P224	μPD78224	μPD78220
Program memory	• One-time PROM	• Mask ROM	• Not built-in ROM
	• 000H-3FFFH • 16384 x 8-bit		–
Pin function	In addition to the pin functions provided with the μPD78224, for the μPD78P224, pin functions related to one-time PROM write/verify/read operations are added. (Refer to 3, "PROM Programming")		
Package	• 84-pin PLCC • 94-pin Plastic QFP		

PROM Programming

The built-in program memory of the μPD78P224 is a 16,384 x 8-bit electrically programmable one-time PROM. To write a program to this one-time PROM, set the μPD78P224 to the PROM programming mode using the NMI and $\overline{\text{RESET}}$ pins, and use the pins listed in the table below.
The programming characteristics of the μPD78P224 is same as that of the μPD27C256A.

Functions of Pins in PROM Write/Verify Mode

Pin Name	Function
NMI	Inputs high voltage for setting the μPD78P224 to the PROM programming mode.
$\overline{\text{RESET}}$	Input low level for setting the μPD78P224 to the PROM mode
V_{PP}	Input PROM programming voltage
A0-A14	Inputs address
D0-D7	Inputs data (in write operation) or outputs data (in verify/read operation)
$\overline{\text{CE}}$	Chip enable input pin
$\overline{\text{OE}}$	Output enable input pin
V_{DD}	Power supply pin
V_{SS}	GND

Note: When programming, program addresses from 0000H to 3FFFH. For a PROM writer which cannot specify address, FFH must be written to address 4000H. If data other than FFH is written to address 4000H, normal operation of the μPD78P224 cannot be guaranteed. Address 4000H is reserved for future functional expansion by NEC.

PROM Programming Operation Mode

When +6V is applied to the V_{DD} pin and +12.5V to the V_{PP} pin, the μPD78P224 enters the program write/verify mode. Operation in this mode is determined according to the setting of CS and OE pins as indicated in the table below.
Additionally, when set to the read mode, the μPD78P224 can read the contents of PROM.

Operation Mode for PROM Programming

Mode \ Pin	NMI	$\overline{\text{RESET}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	V_{PP}	V_{DD}	D0-D7
Program write	+12.5V	L	L	H	+12.5V	+6V	Data input
Program verify			H	L			Data output
Program inhibit			H	H			High Z
Read out			L	L			Data output
Output disable			L	H	+5V	+5V	High Z
Standby			H	L/H			High Z

Note: When +12.5V is applied to V_{PP} and +6V to V_{DD}, both $\overline{\text{CE}}$ and $\overline{\text{OE}}$ cannot be set to low level (L) simultaneously.

Recommended Conditions for Unused Pins

Recommended conditions for unused pins which are not used for programming the PROM are given in following table.

Pin	Recommended Connection
P10-P17	No connection required
P22-P27 X1	Connect to V_{SS}
P30-P31	No connection required
P32-P33	Connect to V_{SS} individually using a pull-down resistor
P34-P37 P51	No connection required
P57 P60-P63	Connect to V_{SS} individually using a pull-down resistor
P66-P67 P70-P76 PT0-PT7 ASTB X2	No connection required

PROM Write Procedure

Data can be written to the PROM using the following procedure. High speed data write operation is possible.

(1) Fix the RESET pin to low level. Apply +12.5V to the NMI pin and connect the unused pins as indicated in Table 3-3.

(2) Apply +6V to the V_{DD} pin and +12.5V to the V_{PP} pin.

(3) Provide the initial address.

(4) Provide write data.

(5) Provide 1ms program pulse (active low) to the CE pin.

(6) Verify mode. If the data has been written, proceed to (8), if not, repeat (4) to (6). If the data cannot be correctly written after25 attempts, go to (7).

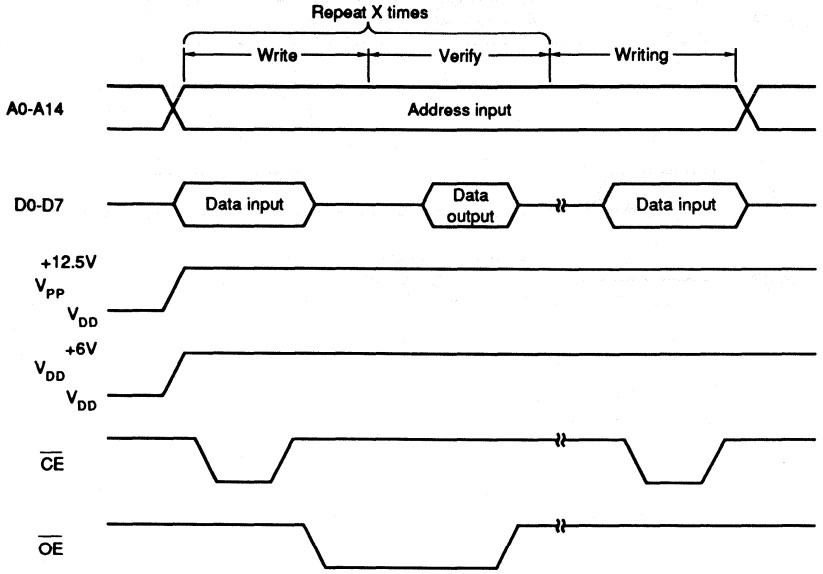
(7) Classify as defective and stop write operation.

(8) Provide write data and supply program pulse (for additional writting) for 3ms times the number of repeats performed betwwen (4) to (6).

(9) Increment the address.

(10) Repeat (4) to (9) until the end address.

The Figure below shows the timing for this sequence from (2) to (8).



PROM Write/Verify timing

PROM Read Procedure

Data can be read out to the external data bus (D0-D7) from the PROM using the following procedure.

(1) Fix the $\overline{RESET}$ pin to low level. Apply +12.5V to the NMI pin and connect the unused pins as indicated in Table 3-3.

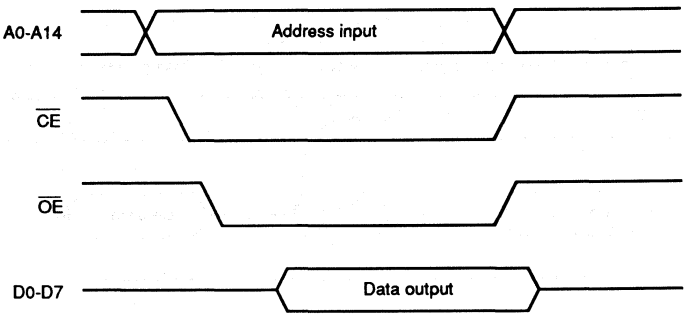
(2) Apply +5V to the V_{DD} pin and V_{PP} pin.

(3) Input the address of the data to read to A0 to A14 pins.

(4) Read mode

(5) Data is output to the D0 to D7 pins.

The Figure below shows the timing for this sequence from (2) to (5).



Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Condition	Ratings	Unit
Power Supply Voltage	V_{DD}		−0.5 to +7.0	V
Input Voltage	V_{I1}		−0.5 to V_{DD} + 0.5	V
	V_{I2}	Note	−0.5 to +13.5	V
Output Voltage	V_O		−0.5 to V_{DD} + 0.5	V
High Level Output Current	I_{OH}	One Output Pin	−2	mA
		All Output Pin Total	−50	mA
Low Level Output Current	I_{OL}	One Output Pin	Peak 30	mA
			Average 15	mA
		All Output Pin Total	Peak 150	mA
			Average 100	mA
Operating Temperature	T_{OPT}		−40 to +85	°C
Storage Temperature	T_{STG}		−65 to +150	°C

Note: Only P20/NMI, $\overline{EA}/V_{PP}$, and P21/INTP0/A9 pins are available when μPD78P224 is set to the PROM programming mode.

Recommended Operating Conditions

Parameter	Ta	V_{DD}
OSC frequency 4 MHz ≤ f_{XTAL} ≤ 12 MHz	−40°C to +85°C	+5.0 V ± 5%
	−10°C to +70°C	+5.0 V ± 10%

Capacitance (Ta = 25°C, $V_{DD} = V_{SS} = 0V$)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Capacitance	C_I	fC = 1 MHz			20	pF
Output Capacitance	C_O	Unmeasured Pins			20	pF
In/Output Capacitance	C_{IO}	Returned to 0V			20	pF

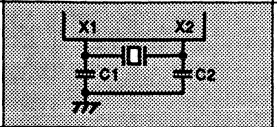
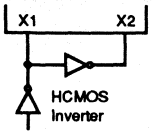
DC Characteristics

$T_a = -10\,°C$ to $+70\,°C$, $V_{DD} = +5.0V \pm 10\%$, $V_{SS} = 0V$
$T_a = -40\,°C$ to $+85\,°C$, $V_{DD} = +5.0V \pm 5\%$, $V_{SS} = 0V$

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	except PTn		0		0.8	V
Input High Voltage	V_{IH1}	except note 1 and PTn		2.2		V_{DD}	V
	V_{IH2}	note 1 Pins		0.8 V_{DD}		V_{DD}	V
Output Low Voltage	V_{OL1}	$I_{OL} = 2.0$ mA				0.45	V
	V_{OL2}	$I_{OL} = 8.0$ mA, Port 1				1.0	V
Output High Voltage	V_{OH1}	$I_{OH} = -1.0$ mA		$V_{DD} - 1.0$			V
	V_{OH2}	$I_{OH} = -100$ μA		$V_{DD} - 0.5$			V
Input Leak. Current	I_{LI}	$0V \leqq V_I \leqq V_{DD}$				±10	μA
Output Leak. Current	I_{LO}	$0V \leqq V_O \leqq V_{DD}$				±10	μA
Pull-up current	I_{IPT}	V_I (PT pin) = 0V			−150	−400	μA
V_{DD} power supply current	I_{DD1}	Operating mode, $f_{XX} = 12$ MHz			16	40	mA
	I_{DD2}	HALT mode, $f_{XX} = 12$ MHz			7	20	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5		5.5	V
Data retention current	I_{DDDR}	STOP mode	$V_{DDDR} = 2.5$ V		2	20	μA
			$V_{DDDR} = 5V \pm 10\%$		5	50	μA

Note: X1, X2, $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4, P26/INTP5, P27/INTP6/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0, and $\overline{\text{EA}}$ pins.

Oscillator Characteristics
Ta=−10°C to +70°C, V_{DD}=+5.0V ±10%, V_{SS}=0V
Ta=−40°C to +85°C, V_{DD}=+5.0V ±5%, V_{SS}=0V

Resonator	Recommended Circuit	Parameter	MIN.	MAX.	Units
Ceramic or crystal resonator (Note)		Oscillation frequency (f_{XX})	4	12	MHz
External Clock		X1 Input frequency (f_X)	4	12	MHz
		X1 input rise, fall time (tr, tf)	0	30	ns
		X1 input high, low level range (t_{OH}, t_{OL})	30	130	ns

Note 1: Oscillator circuit must be positioned as close as possible to the X1 and X2 pins.
2: No other signal line must be wired within the shaded area.

Crystal Oscillators (Ta = −40°C to +85°C)

Manufacturer	Product name	Frequency (MHz)	Recommended circuit constants (pF)	
			C1	C2
Kinseki	HC-18/U	12	27	27
	HC-43/U			
	HC-49/U (Note)			

Note: When HC-49/U is used, the operation temperature range is Ta = −20°C to +70°C.

Ceramic Oscillator (Ta = −40°C to +85°C)

Manufacturers	Product Types	Recommended Capacitors	
		C1 (pF)	C2 (pF)
Murata	CSA10.0MT040	100	100
	CSA12.0MT040 (Note)	100	100
Kyocera (Kyoto Ceramic)	KBR-10.0M	33	33

Note: When CSA12, OMT040 is used, the operation temperature range is −20°C to +85°C.

AC Characteristics
$T_a = -10°C$ to $+70°C$, $V_{DD} = +5.0V \pm 10\%$, $V_{SS} = 0V$
$T_a = -40°C$ to $+85°C$, $V_{DD} = +5.0V \pm 5\%$, $V_{SS} = 0V$
Read/write operation

Parameter	Symbol	Conditiones	MIN.	MAX.	Units
X1 input clock cycle time	t_{CYX}		82	250	ns
Address set up time (against ASTB↓)	t_{SAST}		52		ns
Address hold time (against ASTB↓)	t_{HSTA}	$R_L = 5K\Omega$, $C_L = 50pF$	25		ns
Address → $\overline{RD}$↓ delay time	t_{DAR}		129		ns
Address float time (against $\overline{RD}$↓)	t_{FAR}		11		ns
Address → data input time	t_{DAID}			228	ns
ASTB↓ → data input time	t_{DSTID}			181	ns
$\overline{RD}$↓ → data input time	t_{DRID}			99	ns
ASTB↓ → $\overline{RD}$↓ delay time	t_{DSTR}		52		ns
Data hold time (against $\overline{RD}$↑)	t_{HRID}		0		ns
$\overline{RD}$↑ → address active time	t_{DRA}		124		ns
$\overline{RD}$↑ → ASTB↑ delay time	t_{DRST}		124		ns
$\overline{RD}$ low level width	t_{WRL}		124		ns
ASTB high level width	t_{WSTH}		52		ns
Address → $\overline{WR}$↓ delay time	t_{DAW}		129		ns
ASTB↓ → data output time	t_{DSTOD}			142	ns
$\overline{WR}$↓ → data output time	t_{DWOD}			60	ns
ASTB↓ → $\overline{WR}$↓ delay time	t_{DSTW1}		52		ns
	t_{DSTW2}	Refresh mode	129		ns
Data set up time (against $\overline{WR}$↑)	t_{SODWR}		146		ns
Data set up time (against $\overline{WR}$↓) Note 1	t_{SODWF}	Refresh mode	22		ns
Data hold time (against $\overline{WR}$↑) Note 2	t_{HWOD}		20		ns
$\overline{WR}$↑ → ASTB↑ delay time	t_{DWST}		42		ns
$\overline{WR}$ low level width	t_{WWL1}		196		ns
	t_{WWL2}	Refresh mode	114		ns
Address → $\overline{WAIT}$↓ input time	t_{DAWT}			146	ns
$\overline{ASTB}$ → WAIT↓ input time	t_{DSTWT}			84	ns
$\overline{WAIT}$ hold time (against X1↓)	t_{HWTX}		0		ns
$\overline{WAIT}$ set up time (against X1↑)	t_{SWTX}		0		ns

Remarks: Values in the table are for fxx=12MHz, $C_L = 100pF$.
Note 1: When accessing a pseudo-static RAM (μPD4168, etc.) which clocks in data at the falling edge of the $\overline{WR}$ signal, use t_{SODWF} instead of t_{SODWR} as the data set up time.
Note 2: The hold time includes the time during which V_{OH} and V_{OL} are retained under the following load conditions; $C_L = 100pF$ and $R_L = 2k\Omega$.

Serial operation

Parameter	Symbol	Conditiones		MIN.	MAX.	Units
Serial clock cycle time	t_{CYSK}	Input	External clock	1.0		μs
		Output	Internal clock/16	3		μs
			Internal clock/64	5.3		μs
Serial clock low level width	t_{WSKL}	Input	External clock	420		ns
		Output	Internal clock/16	556		ns
			Internal clock/64	2.5		μs
Serial clock high level width	t_{WSKH}	Input	External clock	420		ns
		Output	Internal clock/16	556		ns
			Internal clock/64	2.5		μs
SI, SB0 set up time to $\overline{SCK}$↑	t_{SSSK}			150		ns
SI, SB0 hold time after $\overline{SCK}$↑	t_{HSSK}			400		ns
SO/SB0 output delay time to $\overline{SCK}$↓	t_{DSBSK1}	CMOS push-pull output (3-line serial I/O mode)		0	300	ns
	t_{DSBSK2}	Open-drain output (SBI mode), $R_L = 1K\Omega$		0	800	ns
SB0 high hold time to $\overline{SCK}$ ↑	t_{HSBSK}	SBI mode		4		t_{CYX}
SB0 low set up time to $\overline{SCK}$ ↓	t_{SSBSK}			4		t_{CYX}
SB0 low level width	t_{WSBL}			4		t_{CYX}
SB0 high level width	t_{WSBH}			4		t_{CYX}

Note: This table shows the values for fxx = 12MHz, C_L = 100pF.

Other operation

Parameter	Symbol	Conditiones	MIN.	MAX.	Units
NMI low level width	t_{WNIL}		10		μs
NMI high level width	T_{WNIH}		10		μs
INTP0-INTP6 low level width	t_{WITL}		24		t_{CYX}
INTP0-INTP6 high level width	t_{WITH}		24		t_{CYX}
$\overline{RESET}$ low level width	t_{WRSL}		10		μs
$\overline{RESET}$ high level width	t_{WRSH}		10		μs

External clock timing

Parameter	Symbol	Conditiones	MIN.	MAX.	Units
X1 input low level width	t_{WXL}		30	130	ns
X1 input high level width	T_{WXH}		30	130	ns
X1 input rise time	t_{XR}		0	30	ns
X1 input fall time	t_{XF}		0	30	ns
X1 input clock cycle time	t_{CYX}		82	250	ns

Comparator characteristics
$T_a = -10°C$ to $+70°C$, $V_{DD} = +5.0V \pm 10\%$, $V_{SS} = 0V$
$T_a = -40°C$ to $+85°C$, $V_{DD} = +5.0V \pm 5\%$, $V_{SS} = 0V$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Comparison accuracy	V_{ACOMP}				100	mV
Comparison time	t_{COMP}		128		256	t_{CYX}
Sampling time	t_{SAMP}		62			t_{CYX}
PT input voltage	V_{IPT}		0		V_{DD}	V

Definition of bus timing depending on t_{CYX}

Parameter	Symbol	Calculation formula	MIN./ MAX.	12 MHz	Units
X1 input cycle time	t_{CYX}		MIN.	82	ns
Address set up time to ASTB↓	t_{SAST}	$t_{CYX}-30$	MIN.	52	ns
Address to $\overline{RD}$↓ delay time	t_{DAR}	$2t_{CYX}-35$	MIN.	129	ns
Address float to $\overline{RD}$↓ time	t_{FAR}	$t_{CYX}/2-30$	MIN.	11	ns
Address to data input time	t_{DAID}	$(4+2n)t_{CYX}-100$	MAX.	228	ns
ASTB↓ to data input time	t_{DSTID}	$(3+2n)t_{CYX}-65$	MAX.	181	ns
$\overline{RD}$↓ to data input time	t_{DRID}	$(2+2n)t_{CYX}-65$	MAX.	99	ns
ASTB↓ to $\overline{RD}$↓ delay time	t_{DSTR}	$t_{CYX}-30$	MIN.	52	ns
$\overline{RD}$↑ to address active time	t_{DRA}	$2t_{CYX}-40$	MIN.	124	ns
$\overline{RD}$↑ to ASTB↑ delay time	t_{DRST}	$2t_{CYX}-40$	MIN.	124	ns
$\overline{RD}$ low level width	t_{WRL}	$(2+2n)t_{CYX}-40$	MIN.	124	ns
ASTB high level width	t_{WSTH}	$t_{CYX}-30$	MIN.	52	ns
Address to $\overline{WR}$↓ delay time	t_{DAW}	$2t_{CYX}-35$	MIN.	129	ns
ASTB↓ to data output time	t_{DSTOD}	$t_{CYX}+60$	MAX.	142	ns
ASTB↓ to $\overline{WR}$↓ delay time	t_{DSTW1}	$t_{CYX}-30$	MIN.	52	ns
	t_{DSTW2}	$2t_{CYX}-35$ (Refresh Mode)	MIN.	129	ns
Data set up time to $\overline{WR}$↑	t_{SODWR}	$(3+2n)t_{CYX}-100$	MIN.	146	ns
Data set up time to $\overline{WR}$↓	t_{SODWF}	$t_{CYX}-60$ (Refresh mode)	MIN.	22	ns
$\overline{WR}$↑ to ASTB↑ delay time	t_{DWST}	$t_{CYX}-40$	MIN.	42	ns
$\overline{WR}$ low level width	t_{WWL1}	$(3+2n)t_{CYX}-50$	MIN.	196	ns
	t_{WWL2}	$(2+2n)t_{CYX}-50$ (Refresh mode)	MIN.	114	ns
Address to $\overline{WAIT}$↓ input time	t_{DAWT}	$3t_{CYX}-100$	MAX.	146	ns
ASTB↓ to $\overline{WAIT}$↓ input time	t_{DSTWT}	$2t_{CYX}-80$	MAX.	84	ns

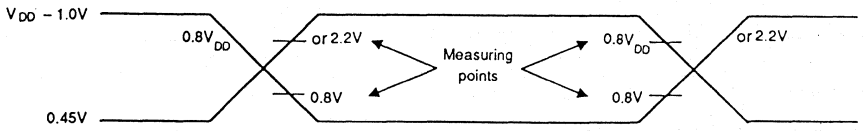
Remarks: n indicates the number of WAIT states.

Data Retention Characteristics
Ta = −10°C to +70°C, V_{DD} = +5.0V ±10%, V_{SS} = 0V
Ta = −40°C to +85°C, V_{DD} = +5.0V ±5%, V_{SS} = 0V

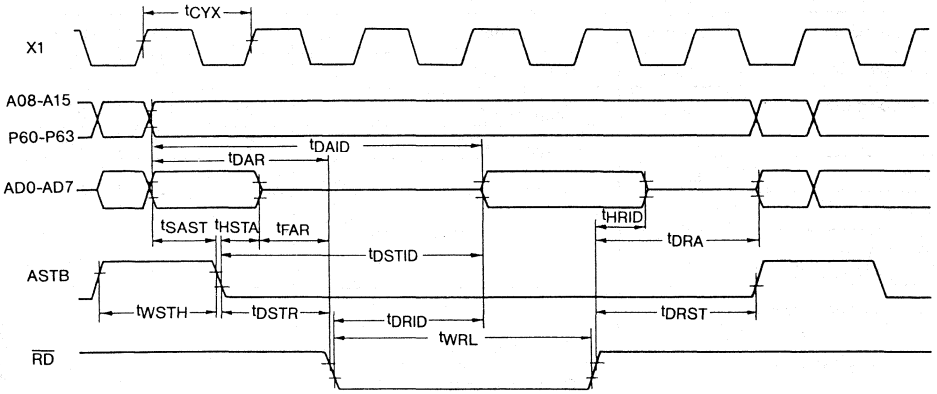
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Units
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	V_{DDDR}=2.5V		2	20	μA
		V_{DDDR}=5V±10%		5	50	μA
V_{DD} rise time	t_{RVD}		200			μs
V_{DD} fall time	t_{FVD}		200			μs
V_{DD} retention time (for STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stabilize wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Low level input voltage	V_{IL}		0		$0.1V_{DDDR}$	V
High level input voltage	V_{IH}		$0.9V_{DDDR}$		V_{DDDR}	V

Note: $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4, P26/INTP5, P27/INTP6/SI, P32/SCK, P33/SO/SB0, and EA Pins.

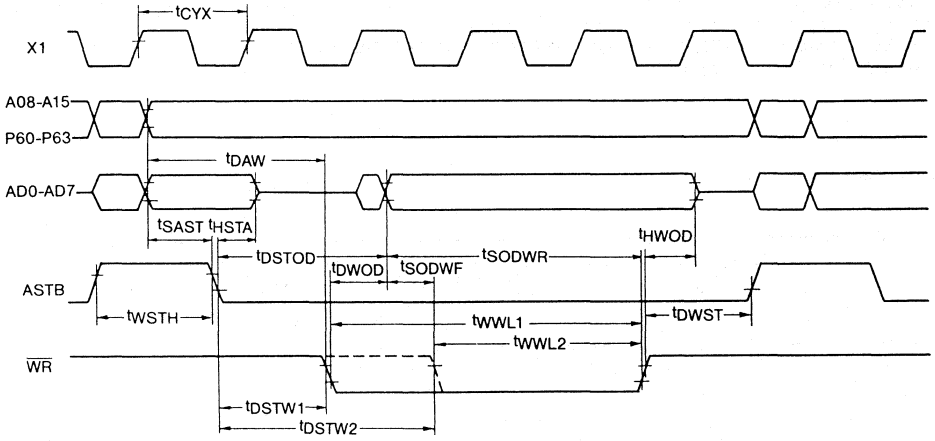
AC timing measurement points



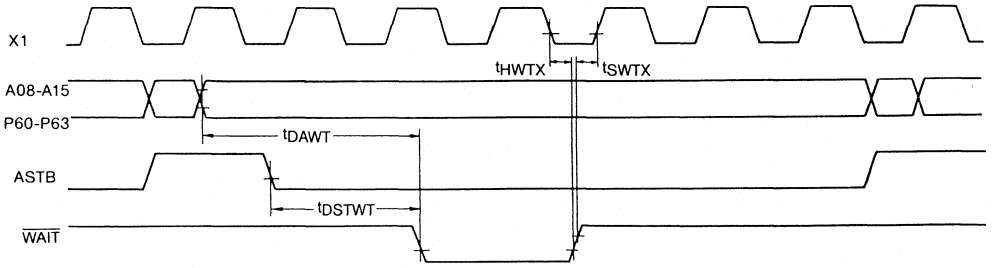
Timing Wave-Forms
Read Operation



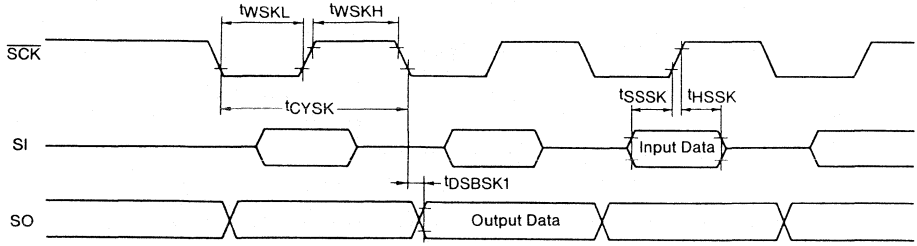
Write Operation



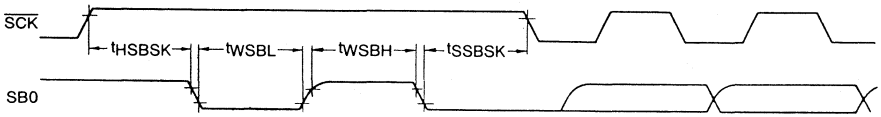
External Wait Input



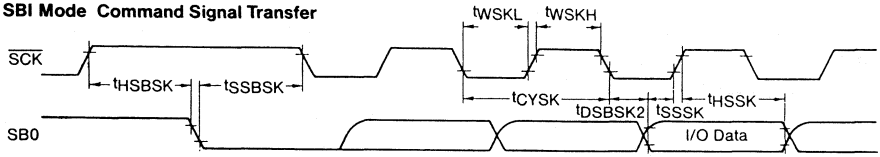
Serial Operation
3-Line Serial I/O Mode



SBI Mode
Bus Release Signal Transfer

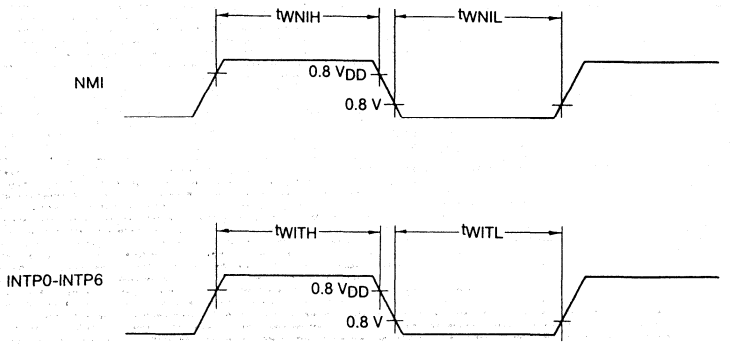


SBI Mode Command Signal Transfer

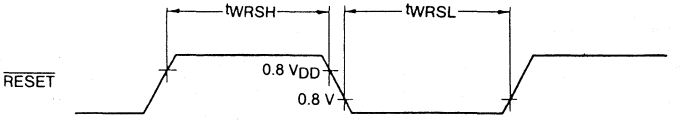


2

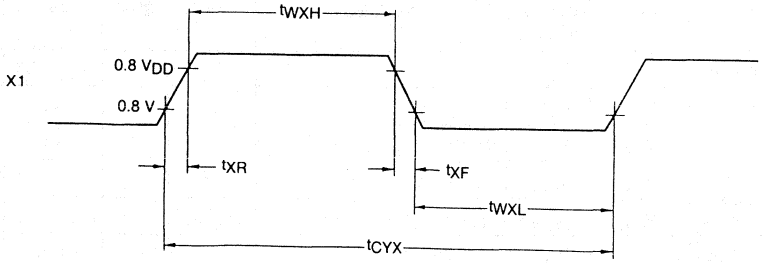
Interrupt Input Timing



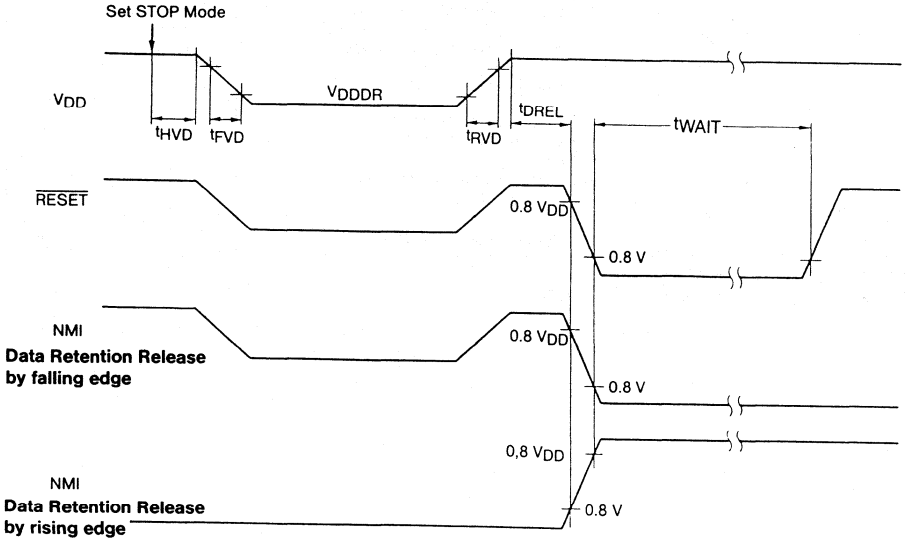
Reset Input Timing



External Clock Timing



Data Retention Timing



DC Programming Characteristics
(Ta = 25 ± 5°C, V_{IP} (Note 1) = 12.5 ± 0.5V, V_{SS} = 0V)

Parameter	Symbol	Symbol (Note 2)	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	V_{IH}		2.4		V_{DDP}+0.3	V
Low level input voltage	V_{IL}	V_{IL}		–0.3		0.8	V
Input leak current	V_{LIP}	V_{LI}	$0 \le V1 \le V_{DDP}$			10	μA
High level output voltage	V_{OH1}	V_{OH1}	I_{OH} = –400 μA	2.4			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DD}–0.7			V
Low level output voltage	V_{OL}	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output leak current	I_{LO}		$0 \le V_O \le V_{DDP}$, $\overline{OE}$ = V_{IH}			10	μA
NMI pin high voltage input current	I_{IP}					±10	μA
V_{DDP} power voltage	V_{DDP}	V_{DD}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} power voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V_{PP} = V_{DDP}			V
V_{DDP} power current	I_{DD}	I_{DD}	Program memory write mode		5	30	mA
			Program memory read mode $\overline{CE}$ = V_{IL}, V_I = VIH		5	30	mA
V_{PP} power current	I_{PP}	I_{PP}	Program memory write mode $\overline{CE}$ = VIL, $\overline{OE}$ = VIH		5	30	mA
			Program memory read mode		1	100	μA

Note 1: Voltage applied to P20/NMI pin.
2: Corresponding pin symbols of the μPD27C256A.

Program Operation

AC Characteristics (Ta = 25 ± 5°C, V_{IP} (Note 1) = 12.5 ± 0.5V, V_{DD} = 6 ± 0.25V, V_{PP} = 12.5 ± 0.3V, V_{SS} = 0V)

Parameter	Symbol	Symbol (Note 2)	Condition	Min.	Typ.	Max.	Unit
Address setup tme (vs. $\overline{CE}$ ↓)	t_{SAC}	t_{AS}		2			μs
Data → $\overline{OE}$ ↓ delay time	t_{DDOO}	t_{OES}		2			μs
Input data setup time (vs. $\overline{CE}$ ↓)	t_{SIDC}	t_{DS}		2			μs
Address hold time (vs. $\overline{CE}$ ↑)	t_{HCA}	t_{AH}		2			μs
Input data hold time (vs. $\overline{CE}$ ↑)	t_{HCID}	t_{DH}		2			μs
Output data hold time (vs. $\overline{CE}$ ↑)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} setup time (vs. $\overline{CE}$ ↓)	t_{SVPC}	t_{VPS}		1			ms
V_{DDP} setup time (vs. $\overline{CE}$ ↓)	t_{SVDC}	t_{VCS}		1			ms
Initial program pulse width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{WL2}	t_{OPW}		2.85		78.75	ms
NMI high voltage input setup time (vs. $\overline{CE}$ ↓)	t_{SPC}			2			μs
$\overline{OE}$ ↓ → Data output time	t_{DOOD}	t_{OE}				150	ns

Note 1: Voltage applied to P20/NMI pin.
2: Corresponding pin symbols of the μPD27C256A.

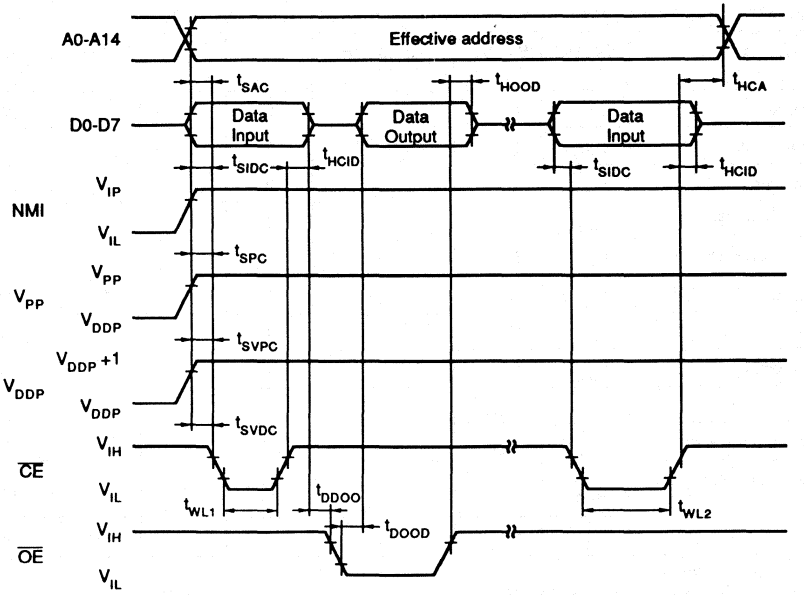
Read Operation

AC Characteristics (Ta = 25 ± 5°C, V_{IP} (Note 1) = 12.5 ± 0.5V, V_{DD} = 5 ± 0.5V, V_{PP} = V_{CC}, V_{SS} = 0V)

Parameter	Symbol	Symbol (Note 2)	Condition	Min.	Typ.	Max.	Unit
Address data output tme	t_{DAOD}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			200	ns
$\overline{CE}$ ↓ → Data ouput time	t_{DCOD}	t_{CE}	$\overline{OE}$ = V_{IL}			200	ns
$\overline{OE}$ ↓ → Data output time	t_{DOOD}	t_{OE}	$\overline{CE}$ = V_{IL}			75	ns
Data hold time (vs. $\overline{OE}$ ↑)	t_{HCOD}	t_{DF}	$\overline{CE}$ = V_{IL}	0		60	ns
Data hold time (vs. address)	t_{HAOD}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Note 1: Voltage applied to P20/NMI pin.
2: Corresponding pin symbols of the μPD27C256A.

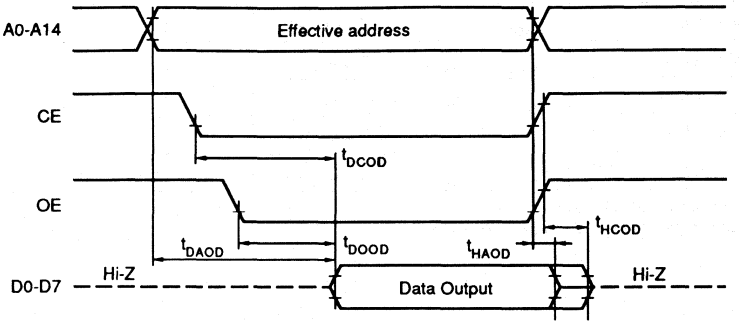
PROM write mode timing



Note 1: V_{DDP} must applied before applying V_{PP}. It should be removed before removing V_{PP}.

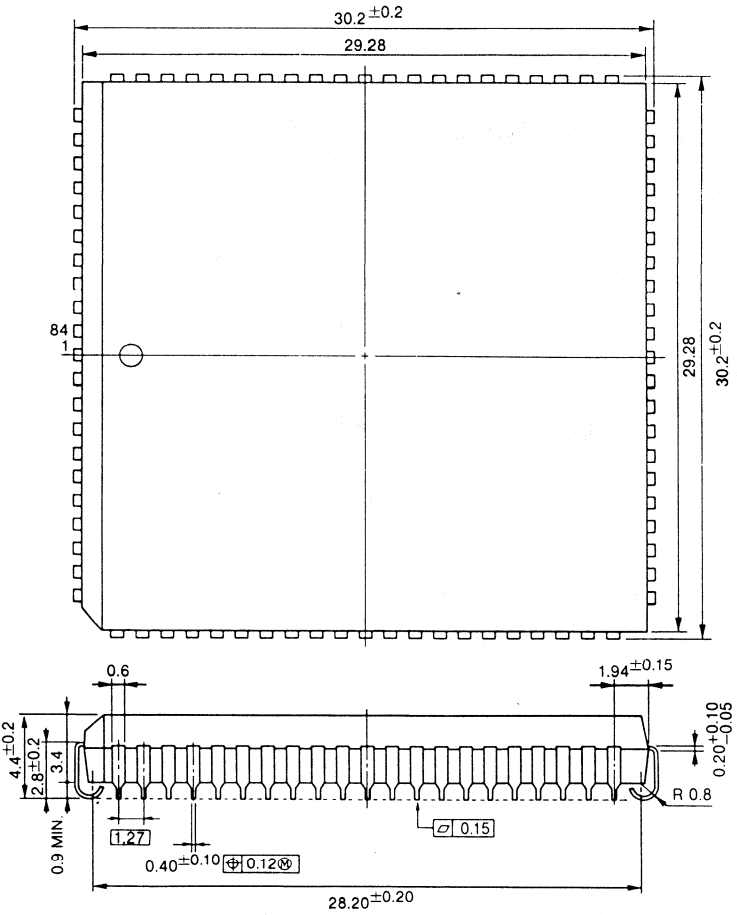
2: V_{PP} must not exceed +13V, including overshoot.

PROM read mode timing



Package Dimensions (unit: mm)

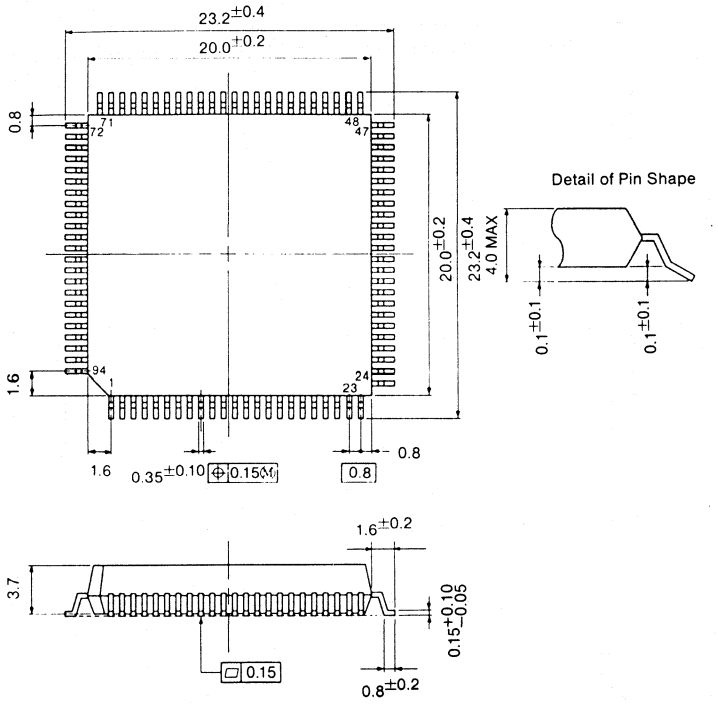
84-PIN PLCC



P84L-50A3

Package Dimensions (unit: mm)

94-PIN FLAT (QFP)



S94GJ-80-5BG

Recommended Soldering Conditions

For the μPD78P224, soldering must be under the following conditions. For other soldering methods, please consult with NEC sales personnel.

(1) μPD78P224L

Method	Condition	Remarks
VPS (Note 1)	Peak temperature: 215°C, one time	Pre-baking required (Note 2)
Pin partial heating	300°C max., 10 seconds max.	

Note 1: Vapor phase soldering
2: 16 hours min. at 125°C.
For aluminium dry packing product, pre-baking is not necessary when mounting within 48 hours after unpacking.

Note: Do not dip solder μPD78P224L or use infra-red soldering.

(2) μPD78P224GJ-5BG

Method	Condition
Pin partial heating	300°C max., 10 seconds max.

Note: Do not dip solder μPD78P224GJ-5BG or use infra-red, or VPS soldering.

Description

The μPD78312 is a CMOS single-chip 16-bit microcomputer, designed fo real-time control applications. It includes a 16-bit CPU, ROM, RAM, an A/D converter, a general-purpose serial communication interface, and a multipurpose pulse input/output unit. In addition, the μPD78312 can be interfaced to external memory, either ROM or RAM. There is also available a ROM-less version, the μPD78310, which can be used with up to 64K bytes of external memory. The first version has been enhanced in order to realize a true 4 phase mode on the up/down counter, especially for controlling DC motors. A unique Feature implemented in hardware to measure velocity and detect direction very efficiently. This new version is called μPD78310A/312A. It will replace μPD78310/312 completely in near future. New designs should always be done with the 'A'-version.

Features

- ☐ Single-chip microcomputer (μCOM-78K series)
- ☐ 96 (98) instruction with many addressing modes
  - 16-bit arithmetic and move instructions, bit manipulation instructions, multiplication/division instructions, string instructions, user stack manipulation instructions.
- ☐ Instruction cycle: 500nsec at 12 MHz input
- ☐ Internal ROM: 8,192 x 8 bits
- ☐ Internal RAM: 256 x 8 bits
- ☐ Capable of directly addressing (ROM/RAM) up to 64K bytes
- ☐ Memory mapping of on-chip peripheral hardware (special function registers)
- ☐ Multipurpose pulse input/output unit
  - Two 16-bit presetable up/down counters
  - Two 16-bit internal timers
  - Two high-accuracy pulse-width-modulated outputs
  - Two 4 bit real-time output port channels
- ☐ 8-bit A/D converter with 4 input channels and sample-and-hold
- ☐ I/O ports
  - 8 dedicated input lines
  - up to 32 I/O lines (μPD78312)
- ☐ General-purpose serial communication interface (with dedicated baud rate generator)
  - Asynchronous mode, I/O interface mode
- ☐ Interrupt request controller
  - Vectored interrupts
  - Context switching
  - Macro service function
- ☐ Pseudo static memory refresh pulse output
- ☐ Watchdog timer
- ☐ Time base counter
- ☐ Standby function (STOP/HALT)
- ☐ CMOS
- ☐ Single power supply
- ☐ μPD78310A/312A with 4 phase mode on the up/down counter
- ☐ μPD78310A/312A have two additional instructions (in total 98)
- ☐ μPD78P312A programmable versions

Ordering Information

Part Number	Package Type	ROM
μPD78310CW	64-PIN SDIP	Rom-less
μPD78310G-1B	64-PIN QFP	
μPD78310G-36	64-PIN QUIP	
μPD78310L	68-PIN PLCC	
μPD78312CW-xxx	64-PIN SDIP	8K MASK ROM
μPD78312G-xxx-1B	64-PIN QFP	
μPD78312G-xxx-36	64-PIN QUIP	
μPD78312L-xxx	68-PIN PLCC	
μPD78310ACW	64-PIN SDIP	ROM-Less
μPD78310AGF	64-PIN QFP	
μPD78310AGQ-36	64-PIN QUIP	
μPD78310AL	68-PIN PLCC	
μPD78312ACW-xxx	64-PIN SDIP	8K MASK ROM
μPD78312AGF-xxx	64-PIN QFP	
μPD78312AGQ-xxx-36	64-PIN QUIP	
μPD78312AL-xxx	68-PIN PLCC	
μPD78P312ADW	64-PIN SDIP Cer.	8K UVPROM
μPD78P312AR	64-PIN QUIP Cer.	
μPD78P312ACW	64-PIN SDIP	8K OTPROM
μPD78P312AGF	64-PIN QFP	
μPD78P312AGQ-36	64-PIN QUIP	
μPD78P312AL	68-PIN PLCC	

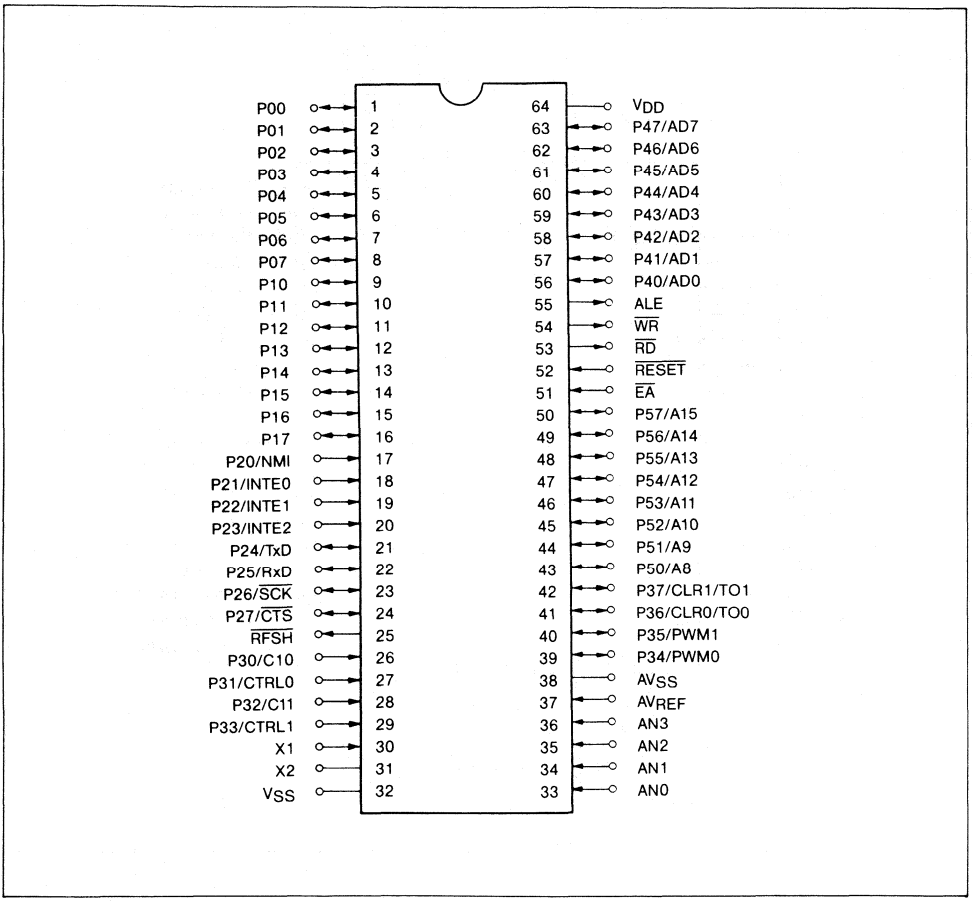
PLCC = plastic leaded chip carrier
QUIP = Quad-in-line package/Bent leads
SDIP = Shrink dual-in-line package
QFP = Quad Flat Pack (SMD)

2

Function Table

Number of basic instructions	96 for 78310/312 98 for 78310A/312A
Minimum instruction execution time	500 ns (when operating at 12 MHz)
Built-in memory	• ROM: 8192 x 8 (μPD78312A only) • RAM: 256 x 8
Memory space	64K bytes
General-purpose register	8 bits x 16 x 8 banks (memory mapping)
I/O line	• Input ports: 8 • I/O ports: 24 (μPD78310A), 40 (μPD78312A) • Output port: 1 • Analog inputs: 4
Multi-function pulse I/O unit	• 16-bit presettable up/down counter x 2 • 16-bit interval timer x 2 • 16-bit free running counter capture function x 2 • High-precision PWM output x 2 • Real-time output port: 4 bits x 2
Serial communication interface	• 8 bits (Send and receive in full duplex mode) • Special baud rate generator included • Asynchronous mode or I/O interface mode
A/D converter	• 8-bit precision (4 analog inputs)
Interrupt function	• 17 sources (external: 4, internal: 13) • 8 priority levels can be programmed. • Three types of interrupt processing modes can be selected. (Vector interrupt function, context switching function and macro service)
Stand-by	STOP mode/HALT mode
Instruction set	16-bit arithmetic/logical instructions, multiply/divide instructions, bit manipulation instructions, BCD correction instructions, user stack manipulation instructions, and string instructions
Others	• Watchdog timer included • 20-bit time base counter included • Pseudo-static RAM refresh function

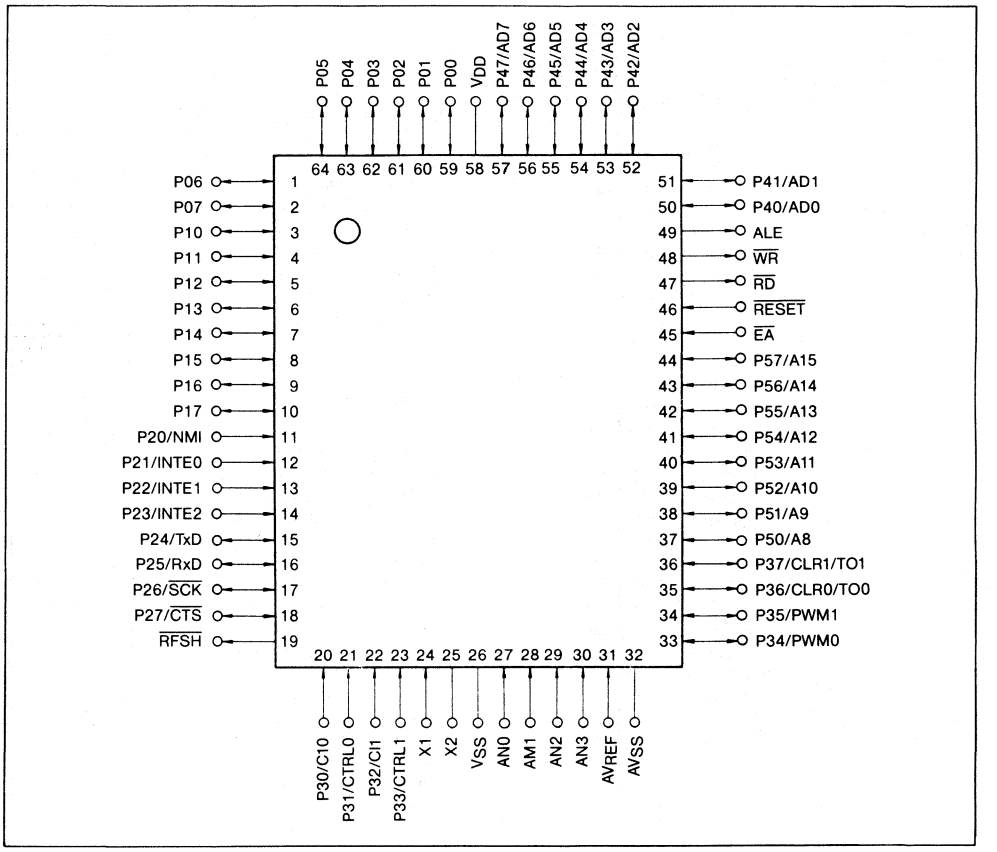
Pin Configurations
64 Pin SDIP and QUIP



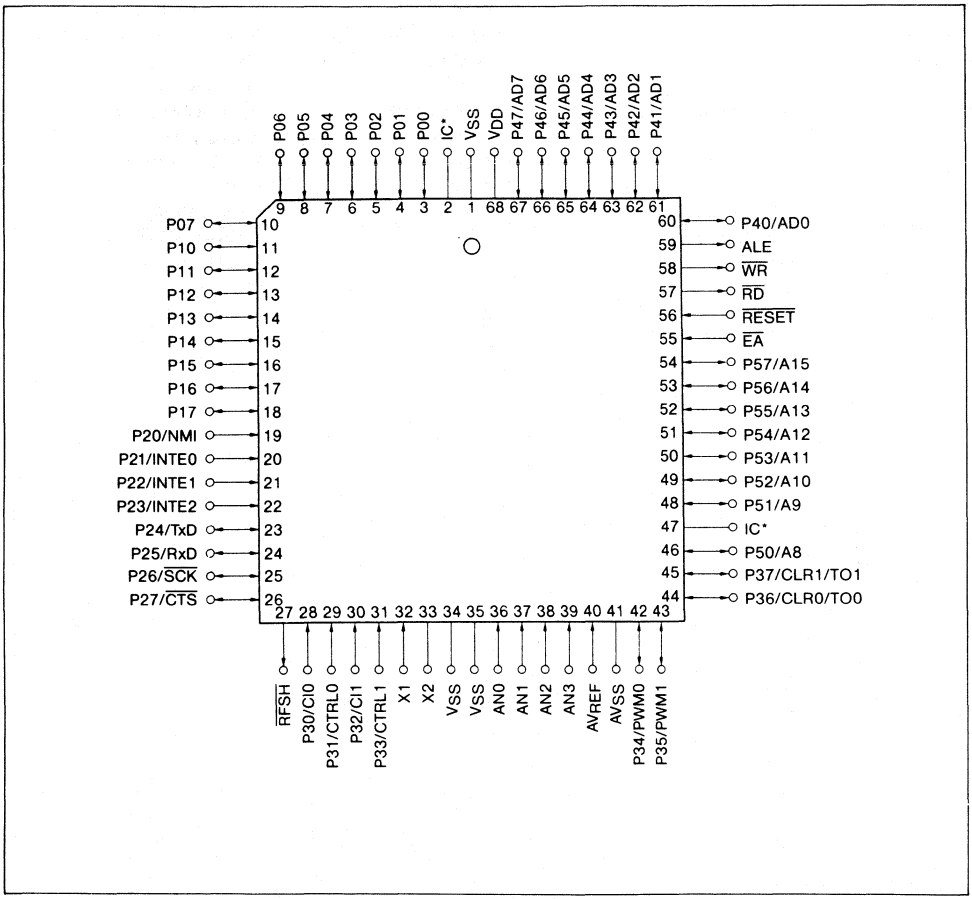
2

Pin Configurations

64 Pin QFP



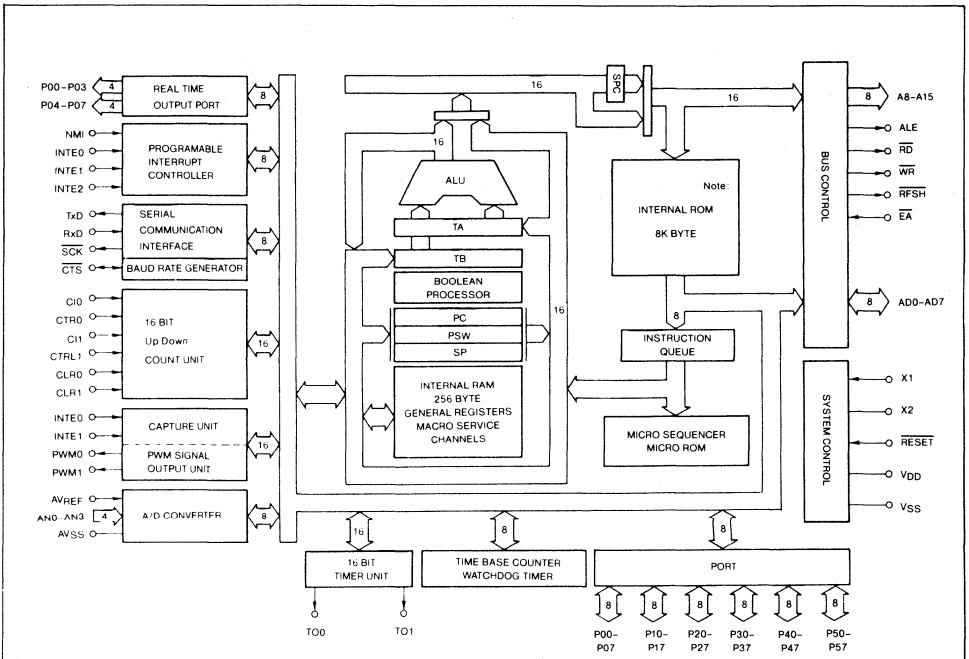
Pin Configurations
68-Pin PLCC



*Note: IC pin has to be connected to V_{SS}

P00-P07	:	Port 0	CI0, CI1	:	Count Pulse Input
P10-P17	:	Port 1	CTRL0, CTRL1	:	Control Pulse Input
P20-P27	:	Port 2	CLR0, CLR1	:	Timer Clear Input
P30-P37	:	Port 3	PWM0, PWM1	:	Pulse Width Modulation Output
P40-P47	:	Port 4	TO0, TO1	:	Timer Output
P50-P57	:	Port 5	NMI	:	Nonmaskable Interrupt
AD0-AD7	:	Address/Data	INTE0-INTE2	:	Interrupt From Externals
A8-A15	:	Address	AN0-AN3	:	Analog Input
$\overline{RD}$	:	Read Strobe	AV_{REF}	:	Reference Voltage
$\overline{WR}$	:	Write Strobe	AV_{SS}	:	Analog V_{SS}
ALE	:	Address Latch Enable	RxD	:	Receive Serial Data
$\overline{EA}$	:	External Access	TxD	:	Transfer Serial Data
$\overline{RFSH}$	:	Refresh	$\overline{SCK}$	:	Serial Clock
X1, X2	:	Crystal	$\overline{CTS}$	:	Clear To Send
$\overline{RESET}$	:	Reset	IC	:	Internally Connected

Block Diagram



Note: μPD78310/μPD78310A are ROM less versions.

Pin Functions

Ports

Pin name	I/O	Dual-function	Function
P00-P07	I/O or real-time output	–	(Port 0) • 8-bit I/O port. Inputs and outputs can be specified bit by bit. • This port also functions as a 2-channel, 4-bit real-time output port.
P10-P17	I/O	–	(Port 1) 8-bit I/O port. Inputs and outputs can be specified bit by bit.
P20	Input	NMI	(Port 2) P20-P23 function as an input port. P24-P27 function as an I/O port. Inputs and outputs can be specified bit by bit.
P21		INTE0	
P22		INTE1	
P23		INTE2	
P24	I/O	TxD	
P25		RxD	
P26		$\overline{SCK}$	
P27		$\overline{CTS}$	
P30	Input	CI0	(Port 3) P30-P33 function as an input port. P34-P37 function as an I/O port. Inputs and outputs can be specified bit by bit.
P31		CTRL0	
P32		CI1	
P33		CTRL1	
P34	I/O	PWM0	
P35		PWM1	
P36		TO0/CLR0	
P37		TO1/CLR1	
P40-P47	I/O	AD0-AD7	(Port 4) 8-bit I/O port. Inputs and outputs can be specified in units of 8 bits.
P50-P57	I/O	A8-A15	(Port 5) 8-bit I/O port. Inputs and outputs can be specified bit by bit .

2

Non-Port Pins

Pin name	I/O	Dual-function	Function
NMI	Input	P20	Nonmaskable interrupt request input pin. The rising or falling edge can be specified as the detective edge through the mode register.
INTE0	Input	P21	External interrupt request input pin. The detective edge can be selected through the mode register.
INTE1		P22	
INTE2		P23	
TxD	I/O	P24	Serial data output pin
RxD	Input	P25	Serial data input pin
$\overline{SCK}$	I/O	P26	Serial clock output pin
$\overline{CTS}$	I/O	P27	• In asynchronous mode, the pin receives an input of a send enable control signal. • In I/O interface mode, the pin functions as a serial clock I/O pin.
CI0	Input	P30	Inputs of external count clocks for the count unit
CI1		P31	
CTRL0	Input	P32	Inputs of a count operation switching control signal for the count unit
CTRL1		P33	
CLR0	Input	P36/TO0	Inputs of a clear signal for the count unit
CLR1		P37/TO1	
PWM0	Output	P34	PWM output pins
PWM1		P35	
TO0	Output	P36/CLR0	Pulse output pins for the timer unit
TO1		P37/CLR1	
AD0-AD7	I/O	P40-P47	Multiplexed address/data bus when an external memory is connected
A8-A15	Output	P50-P57	Address bus when an external memory is connected
$\overline{WR}$	Output	–	External memory write signal output
$\overline{RD}$	Output	–	External memory read signal output
ALE	Output	–	Output pin of a timing signal for externally latching an address output when external memory is accessed
AN0-AN3	Input	–	Analog inputs to the A/D converter
AV_{REF}	–	–	A/D converter reference voltage input
AV_{SS}	–	–	Ground of the A/D converter
X1	Input	–	Crystal or ceramic input for system clock generation. A clock signal provided externally is applied to the X1 pin, and its inverted signal is applied to the X2 pin.
X2	–	–	

Non-Port Pins (Cont'd)

Pin name	I/O	Dual-function	Function
$\overline{RFSH}$	Output	–	Refresh pulse output to an external pseudo-static memory
$\overline{RESET}$	Input	–	System reset input
V_{DD}	–	–	Positive power supply pin
V_{SS}	–	–	Ground pin
IC	–	–	Internally Connected Leave this pin open.

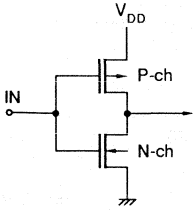
I/O Circuits

The type of I/O circuits of each pin and recommended connections for unused pins are shown in following table. The different types of I/O circuits are shown afterwards.

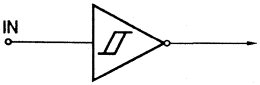
Input/Output type of each pin and what to do when not used

Pin	I/O type	Input/Output	Recommended connection when not used
P00-P07	5	Input/Output	Input: Connected to V_{DD} via a pull-up resistor Output: open
P10-P17	5		
P20/NMI	2	Input	Connected to V_{SS}
P21/INTE0	1		
P22/INTE1			
P23/INTE2			
P24/TxD	5	Input/Output	Input: Connected to V_{DD} via a pull-up resistor Output: open
P25/RxD			
P26/SCK			
P27/CTS			
P30/CI0	1	Input	Connected to V_{SS} or V_{DD}
P31/CTRL0			
P32/CI1			
P33/CTRL1			
P34/PWM0	5	Input/Output	Input: Connected to V_{DD} via a pull-up resistor Output: open
P35/PWM1			
P36/TO0/CLR0	6		
P37/TO1/CLR1			
P40-P47/AD0-AD7	5	Input/Output	
P50-P57/A8-A15	5	Input/Output	
$\overline{WR}$	3	Output	open
$\overline{RD}$			
ALE			
$\overline{EA}$	1	Input	Connected to V_{SS} or V_{DD}
AN0-AN3	7	Input	
$\overline{RFSH}$	3	Output	open
$\overline{RESET}$	2	Input	Connected to V_{SS} or V_{DD}
AV_{REF}, AV_{SS}		Input	Connected to V_{SS}

Type 1

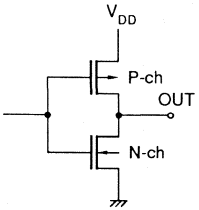


Type 2

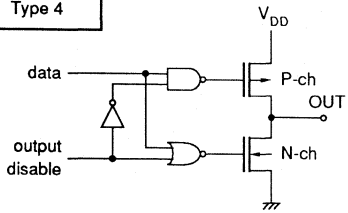


Schmitt trigger input with hysteresis characteristics

Type 3



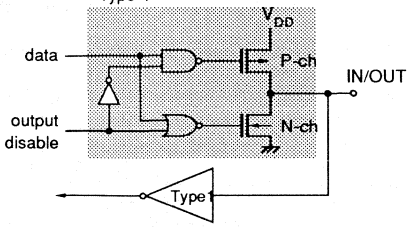
Type 4



Push-pull output which can output high impedance
(Both the positive and negative channels are off).

Type 5

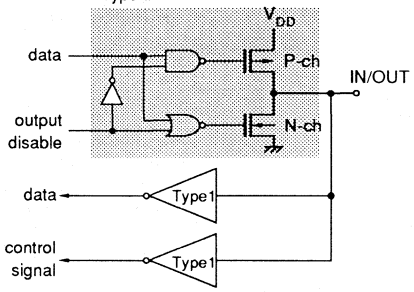
Type 4



I/O circuit consisting of type 4 push-pull output and type 1 input buffer

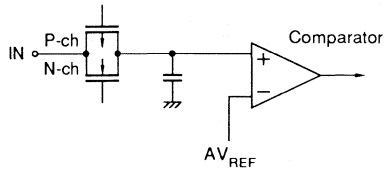
Type 6

Type 4



I/O circuit consisting of type 4 push-pull output and type 1 input buffer

Type 7



(Threshold voltage)

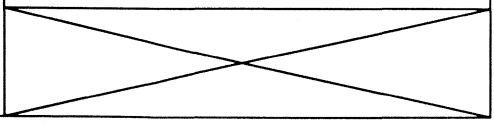


Figure 1-1 Input/Output Circuit of Pins

Difference Between μPD78310A, μPD78312A, and μPD78P312A

The μPD78310A is similar to the μPD78312A except that the μPD78310A does not contain a mask ROM.

The μPD78P312A uses a one-time PROM or EPROM instead of the mask ROM in the μPD78312A.

The Table below lists the differences between these products.
Features other than noted here are common to all three units.

Item		μPD78310A	μPD78312A	μPD78P312A
Program memory		Not included	• Mask ROM • 8192 x 8 bits	• One-time PROM or EPROM • 8192 x 8 bits
Pin function	PROM mode	Not available	Not available	Available
	Ports 4 and 5	Not available (Always function as an address bus and a data bus)	Available	Available
	$\overline{EA}$	Available (Be sure to set the low level.)	Available	Not available
External memory access		64K bytes of external memory can always be accessed regardless of the memory expansion mode register (MM) specification.	External memory can be expanded to 256 bytes, to 4K bytes, to 16K bytes, and to 56K bytes in steps according to the memory expansion mode register (MM) specification.	Same as the μPD78312A
Package	Without window	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QUIP • 64-pin plastic QFP (14 x 20) • 68-pin PLCC		
	With window	None		• 64-pin ceramic DIP (750 mil) • 64-pin ceramic QUIP

Difference Between μPD78312A and μPD78312

The μPD78312A is an extended version of the μPD78312. Following Table lists the differences between the μPD78312A and the μPD78312. Similar differences exist between the μPD78310A and the μPD78310.

Item	μPD78310A μPD78312A	μPD78310 μPD78312
Counter unit mode 4 (4-time mode)	Available	Not available
Start of interval timer count operation by external trigger	Available	Not available
16-bit data transfer instructions between memory and a register pair • MOVW rp1, !addr16 instruction • MOVW !addr16, rp1 instruction	Available	Not available

Design hints:

In some application systems, when external memory is accessed with the μPD78310A, μPD78312A, or μPD78P312A, a glitch of approximately up to 2.0V may appear on the ALE pin.

(1) Generation of glitches

A glitch is likely to appear as the status of the address/data multiplexed bus (port 4) changes from output of address FFH to output of data 00H. The glitch may cause the address latch circuit to malfunction and latch the data being regarded inproperly as the lower address part. This may prevent normal operation of the application product.

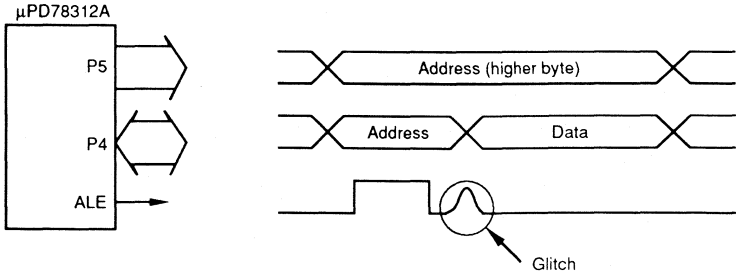


Figure: Generation of a Glitch on the ALE Pin

(2) Protection

To suppress glitch outputs to a level that allows normal operation of an application system, bear the following in mind when mounting the device:

(1) Strengthen patterns for the power supply and ground. (For example, use a multi-layer board.)

(2) Directly mount the device, instead of inserting it into a socket.

(3) Reduce the load capacity of the bus.

The circuit shown in Figure overleaf can be immediately implemented to prevent malfunction.

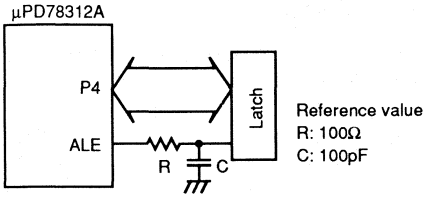


Figure: Sample Protection Circuit

(3) Causes

Possible factors contributing to glitch generation include:

(1) Device factor

As operation becomes faster, switching noise is easier to generate.

(2) System factors

- As the load capacity on the bus increases, an instantaneous quantity of traveling chargeincreases, increasing the chance of generating glitches.
- As the impedance on the power line increases, the more likely it is that glitches may be generated.

Absolute Maximum Ratings
Ta = 25°C

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5~+7.0	V
	AV_{REF}		-0.5~V_{DD}+0.3	V
	AV_{SS}		-0.5~+0.5	V
Input Voltage	V_I		-0.5~+7.0	V
Output Voltage	V_0		-0.5~+7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	- 1	mA
		All Output Pin Total	-25	mA
Operating Temperature	T_{opt}		-10~+70	°C
Storage Temperature	T_{stg}		-65~150	°C

2

Operating Conditions

Parameter / Osc. Freq.	Condition	Ta	V_{DD}
fxx≤12MHz		-10~+70°C	+5.0V±10%

Capacitance (Ta=25°C,V_{DD}=V_{SS}=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f=1MHz			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	C_{IO}				20	pF

DC Characteristics

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL1}	EXCEPT $\overline{EA}$	0		0.8	V
	V_{IL2}	$\overline{EA}$	0		0.5	V
Input High Voltage	V_{IH1}	All except X2, X1, $\overline{RESET}$, P20/NMI	2.2		V_{DD}	V
	V_{IH2}	X2, X1, $\overline{RESET}$, P20/NMI	3.8		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL}=2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH}=-1mA	V_{DD}-1			V
Input Current	I_I	$\overline{RESET}$, P20/NMI, 0. 45V<VI<VCC			±10	μA
Input Leakage Current	I_{LI}				±10	μA
Output Leakage Current	I_{LO}				±10	μA
AV_{REF} Current	AI_{REF}	f_{CLK}=6MHz		1.5	5	mA
V_{DD} Supply Current	I_{DD1}	Operation Mode, f_{CLK}=6MHz		30	60	mA
	I_{DD2}	Halt Mode, f_{CLK}=6MHz		5	15	mA
Data Retention Current	I_{DDDR}	V_{DDDR}=2.5V		3	15	μA
		V_{DDDR}=5.0±10%		10	50	μA
Data Retention Voltage	V_{DDDR}	Stop Mode	2.5			V

AC Characteristics

Read/Write Operation Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions	Min.	Max.	Units
Internal System Clock *1	t_{CYK}		166	1000	ns
Address Setup to ALE ↓	t_{SAL}		150		ns
Address Hold from ALE ↓	t_{HLA}		30		ns
Address to $\overline{RD}$ ↓ delay time	t_{DAR}		230		ns
$\overline{RD}$ ↓ to Address floating	t_{FRA}			0	ns
Address to Data output	t_{DAID}			410	ns
ALE ↓ to Data Input	t_{DLID}			230	ns
$\overline{RD}$ ↓ to Data Input	t_{DRID}			180	ns
ALE ↓ to$\overline{RD}$ ↓ Delay Time	t_{DLR}		60		ns
Data Hold Time from $\overline{RD}$ ↑	t_{HRID}		0		ns
$\overline{RD}$ ↑ to Address active	t_{DRA}		50		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{DRL}		100		ns
$\overline{RD}$ Width Low	t_{WRL}		200		ns
ALE Width High	t_{WLH}		120		ns
Address to $\overline{WR}$ ↓ Delay	t_{DAW}		300		ns
ALE ↓ to Data Output	t_{DLOD}			190	ns
$\overline{WR}$ ↓ to Data Output	t_{DWOD}			100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time*2	t_{DLW}		30		ns
	t_{LW1}	in Refresh Mode	110		ns
Data Setup Time to $\overline{WR}$ ↑	t_{SODWR}		150		ns
Data Setup Time to $\overline{WR}$ ↓	t_{SODWF}	in Refresh Mode	30		ns
Data Hold Time from $\overline{WR}$ ↑	t_{HWOD}		20		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{DWL}		110		ns
$\overline{WR}$ Width Low	t_{WWL}		200		ns

Notes:

*1. Internal System Clock is derived from f_{XTAL} by dividing by 2 or 8, selectable with the STBC register Table above are for following conditions:

f_{XTAL} = 12MHz, SCLK = $f_{XTAL}/2$, tcyc = $2/f_{XTAL}$

*2 During Refresh pulse generation the falling edge of WR is delayed for 1/2 cycle

Serial Operation

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions			Min.	Max.	Units
$\overline{SCK}$ Cycle Time	t_{CYSK}	Output	$\overline{SCK}$	*1	1.33		μs
			$\overline{CTS}$	*2	1.33		μs
		Input	$\overline{CTS}$	*3	1		μs
$\overline{SCK}$ Width Low	t_{WSKL}	Output	$\overline{SCK}$	*1	580		ns
			$\overline{CTS}$	*2	580		ns
		Input	$\overline{CTS}$	*3	420		ns
$\overline{SCK}$ Width High	t_{WSKH}	Output	$\overline{SCK}$	*1	580		ns
			$\overline{CTS}$	*2	580		ns
		Input	$\overline{CTS}$	*3	420		ns
$\overline{CTS}$ Width High/Low	t_{WCSH} t_{WCSL}			*4	3		t_{CLK}
RxD Setup Time to $\overline{CTS}$ ↑	t_{SRXSK}				80		ns
RxD Hold Time from $\overline{CTS}$ ↑	t_{HSKRX}				80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{DSKTX}					210	ns

Notes:
*1: I/O interface mode transmission, data transfer speed 750 kbps
*2: I/O interface mode reception, data transfer speed 750 kbps
*3: I/O interface mode reception, data transfer speed 1 Mbps
*4: Asynchronous mode

A/D Converter Characteristics

Ta=-10°C to +70°C, V_{SS}=AV_{SS}=0V, 3.4V≤V_{AREF}≤V_{DD}, V_{DD}=+5V±10%

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Resolution			8			Bit
Full Scale Error		$4.0 \le AV_{REF} \le V_{DD}$			0.4	%
		$166ns \le t_{CYK} \le 500ns$			0.8	%
Quantization Error					±1/2	LSB
Conversion Time	T_{CONV}	$166ns \le t_{CYK} \le 250ns$	180			t_{cyc}
		$250ns \le t_{CYK} \le 500ns$	120			t_{cyc}
Sampling Time	T_{SAMP}	$166ns \le t_{CYK} \le 250ns$	36			t_{cyc}
		$250ns \le t_{CYK} \le 500ns$	24			t_{cyc}
Input Voltage	V_{IAN}		0		AV_{REF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
Analog Reference Voltage	AV_{REF}		3.4		V_{DD}	V
AV_{REF} Current	AI_{REF}	f_{CLK} = 6MHz		1.5	5.0	mA

Up/Down Counter Input

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions	Min.	Max.	Units
CI0, CI1 High/Low Time	t_{WCIH}, t_{WCIL}		3		t_{CYK}
CTRL0, CTRL1 High/Low Time	t_{WCTH}, t_{WCTL}		3		t_{CYK}
CTRL0, CTRL1 Setup Time against CI ↑	t_{SCTCI}	in Mode 3, CI programmed on rising edge	2		t_{CYK}
CTRL0, CTRL1 Hold Time against CI ↑	t_{HCICT}	in Mode 3, CI programmed on rising edge	5		t_{CYK}
CLR0, CLR1 High/Low Time	t_{WCRH}, t_{WCRL}		3		t_{CYK}

Other Operation

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions	Min.	Max.	Units
NMI Input High/Low	t_{WNIH}, t_{WNIL}		10		μs
INTE0 Input High/Low	t_{W10H}, t_{W10L}		3		t_{CYK}
INTE1 Input High/Low	t_{W11H}, t_{W11L}		3		t_{CYK}
INTE2 Input High/Low	t_{W12H}, t_{W12L}		3		t_{CYK}
$\overline{RESET}$ Input High/Low	t_{WRSH}, t_{WRSL}		10		μs

External clock timing

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions	Min.	Max.	Units
X1 Input High Width	t_{WXH}		30	130	ns
X1 Input Low Width	t_{WXL}		30	130	ns
X1 Rise Time	t_{XR}		0	30	ns
X1 Fall Time	t_{XF}		0	30	ns
X1 Cycle Time	t_{CYX}		83	250	ns

Absolute Maximum Ratings
Ta = 25°C

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5~+7.0	V
	AV_{REF}		-0.5~V_{DD}+0.3	V
	AV_{SS}		-0.5~+0.5	V
Input Voltage	V_I		-0.5~V_{DD}+0.5	V
Output Voltage	V_O		-0.5~V_{DD}+0.5	V
Output Current Low	I_{OL}	at 1 Pin	4.0	mA
		Total of all output pins	100	mA
Output Current High	I_{OH}	at 1 Pin	- 1	mA
		Total of all output pins	-25	mA
Operating Temperature	T_{opt}		-10~+70	°C
Storage Temperature	T_{stg}		-65~+150	°C

Operating Conditions

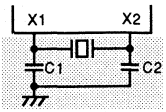
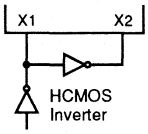
Parameter / Osc. Freq.	Condition	Ta	V_{DD}
4MHz≤f_{XX}≤12MHz		-10~+70°C	+5.0V±10%

Capacitance (Ta=25°C,V_{DD}=V_{SS}=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f = 1MHz 0V on pins other than measured pins			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	C_{IO}				20	pF

Oscillator characteristics

(Ta = -10 to +70°C, V_{DD} = +5.0V ±10%, V_{SS} = AV_{SS} = 0V, 4.0V ≤ AV_{REF} ≤ AV_{DD})

Oscillator	Recommended circuit	Item	Min.	Typ.	Max.	Unit
Ceramic or crystal resonator		Oscillator frequency (f_{XX})	4		12	MHz
			4		12	MHz
External clock		X1 input frequency (f_X)	4		12	MHz
			4		12	MHz
		X1 input rising and falling times (t_{XR}, t_{XF})	0		30	ns
		X1 input high and low level widths (t_{WXH}, t_{WXL})	30		130	ns

Notes 1: The oscillating circuit should be placed as close to the X1 and X2 pins as possible.
2: Do not draw other signal lines in the shaded area.

The following ceramic resonator is used, the following external capacitance is recommended: (Ta = -10°C to +70°C)

Manufacturer	Part No.	Frequency (MHz)	External capacitance (pF)	
			C1	C2
Murata Mfg. Co., Ltd.	CSA12.0MT	12.0	30	30
	CST12.0MT	12.0	included	included

When a crystal resonator is used, the following external capacitance is recommended:
C1 = C2 = 15pF

DC Characteristics

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL1}	EXCEPT $\overline{EA}$		0		0.8	V
	V_{IL2}	$\overline{EA}$		0		0.5	V
Input High Voltage	V_{IH1}	All except X2, X1, $\overline{RESET}$, P20/NMI		2.2		V_{DD}	V
	V_{IH2}	X2, X1, $\overline{RESET}$, P20/NMI		3.8		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL}=2.0mA				0.45	V
Output High Voltage	V_{OH}	I_{OH}=-1mA		V_{DD}-1			V
Input Current	I_I	$\overline{RESET}$, P20/NMI, 0. 45V<VI<VCC				±10	μA
Input Leakage Current	I_{LI}					±10	μA
Output Leakage Current	I_{LO}					±10	μA
AV_{REF} Current	AI_{REF}	f_{CLK}=6MHz			1.5	5	mA
V_{DD} Supply Current	I_{DD1}	Operation Mode, f_{CLK}=6MHz			30	60	mA
	I_{DD2}	Halt Mode, f_{CLK}=6MHz			5	15	mA
Data Retention Current	I_{DDDR}	STOP mode	V_{DDDR}=2.5V		3	15	μA
			V_{DDDR}=5.0±10%		10	50	μA
Data Retention Voltage	V_{DDDR}	Stop Mode		2.5			V

2

AC Characteristics
Read/Write Operation Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions	Min.	Max.	Units
Internal System Clock *1	t_{CYK}		166	1000	ns
Address Setup to ALE ↓	t_{SAL}		150		ns
Address Hold from ALE ↓	t_{HLA}	C_L = 100pF, R_L = 2kΩ *4	30		ns
Address to $\overline{RD}$ ↓ delay time	t_{DAR}		230		ns
$\overline{RD}$ ↓ to Address floating	t_{FRA}			0	ns
Address to Data output	t_{DAID}			410	ns
ALE ↓ to Data Input	t_{DLID}			230	ns
$\overline{RD}$ ↓ to Data Input	t_{DRID}			180	ns
ALE ↓ to$\overline{RD}$ ↓ Delay Time	t_{DLR}		60		ns
Data Hold Time from $\overline{RD}$ ↑	t_{HRID}		0		ns
$\overline{RD}$ ↑ to Address active	t_{DRA}		50		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{DRL}		100		ns
$\overline{RD}$ Width Low	t_{WRL}		200		ns
ALE Width High	t_{WLH}		120		ns
Address to $\overline{WR}$ ↓ Delay	t_{DAW}		300		ns
ALE ↓ to Data Output	t_{DLOD}			190	ns
$\overline{WR}$ ↓ to Data Output	t_{DWOD}			100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time *2	t_{DLW}		30		ns
		in Refresh Mode	110		ns
Data Setup Time to $\overline{WR}$ ↑	t_{SODWR}		150		ns
Data Setup Time to $\overline{WR}$ ↓ *3	t_{SODWF}	in Refresh Mode	30		ns
Data Hold Time from $\overline{WR}$ ↑	t_{HWOD}		20		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{DWL}		110		ns
$\overline{WR}$ Width Low	t_{WWL}		200		ns

Notes:
*1: The internal system clock (f_{CLK}) is obtained by dividing the oscillator clock (f_{XX}) by 2 or 8 according to the STBC register specification. In the above table, f_{XX} = 12 MHz and $f_{CLK} = f_{XX}/2$ are assumed.

*2: When pulses are refreshed, the WR signal goes low a half clock later than the ALE signal, so t_{DLW} is the value in the lower row in the table.

*3: When access is made to a pseudo-static RAM that takes data on the falling edge of the WR signal (such as μPD4168), the data setup time is t_{SODWF}, instead of t_{SODWR}.

*4: The hold time includes the times to maintain V_{OH} and V_{OL} under load conditions C_L = 100pF and R_L = 2kΩ.

Serial Operation

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{SS}=0V

Parameter	Symbol	Test Conditions			Min.	Max.	Units
$\overline{SCK}$ Cycle Time	t_{CYSK}	Output	$\overline{SCK}$	*1	1.33		μs
			$\overline{CTS}$	*2	1.33		μs
		Input	$\overline{CTS}$	*3	1		μs
$\overline{SCK}$ Width Low	t_{WSKL}	Output	$\overline{SCK}$	*1	580		ns
			$\overline{CTS}$	*2	580		ns
		Input	$\overline{CTS}$	*3	420		ns
$\overline{SCK}$ Width High	t_{WSKH}	Output	$\overline{SCK}$	*1	580		ns
			$\overline{CTS}$	*2	580		ns
		Input	$\overline{CTS}$	*3	420		ns
$\overline{CTS}$ Width High/Low	t_{WCSH} t_{WCSL}			*4	3		t_{CLK}
RxD Setup Time to $\overline{CTS}$ ↑	t_{SRXSK}				80		ns
RxD Hold Time from $\overline{CTS}$ ↑	t_{HSKRX}				80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{DSKTX}					210	ns

Notes:
*1: I/O interface mode transmission, data transfer speed 750 kbps
*2: I/O interface mode reception, data transfer speed 750 kbps
*3: I/O interface mode reception, data transfer speed 1 Mbps
*4: Asynchronous mode

A/D Converter Characteristics

Ta=-10°C to +70°C, V_{SS}=AV_{SS}=0V, 4.0V≤V_{AREF}≤V_{DD}, V_{DD}=+5V±10%

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Resolution			8			Bit
Full Scale Error		4.0 ≤ AV_{REF} ≤ V_{DD} 166ns ≤ t_{CYK} ≤ 500ns			0.4	%
Quantization Error					±1/2	LSB
Conversion Time	t_{CONV}	166ns ≤ t_{CYK} ≤ 250ns	180			t_{cyc}
		250ns ≤ t_{CYK} ≤ 500ns	120			t_{cyc}
Sampling Time	t_{SAMP}	166ns ≤ t_{CYK} ≤ 250ns	36			t_{cyc}
		250ns ≤ t_{CYK} ≤ 500ns	24			t_{cyc}
Analog Input Voltage	V_{IAN}		0		AV_{REF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
Analog Reference Voltage	AV_{REF}		4.0		V_{DD}	V
AV_{REF} Current	AI_{REF}	f_{CLK} = 6MHz		1.5	5.0	mA

2

Up/Down Counter Input

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions	Min.	Max.	Units
CI0, CI1 Hjgh/Low Time	t_{WCIH}, t_{WCIL}		3		t_{CYK}
CTRL0, CTRL1 High/Low Time	t_{WCTH}, t_{WCTL}		3		t_{CYK}
CTRL0, CTRL1 Setup Time against CI ↑	t_{SCTCI}	in Mode 3, CI programmed on rising edge	2		t_{CYK}
CTRL0, CTRL1 Hold Time against CI ↑	t_{HCICT}	in Mode 3, CI programmed on rising edge	5		t_{CYK}
CLR0, CLR1 High/Low Time	t_{WCRH}, t_{WCRL}		3		t_{CYK}
CI0/CI1 Setup Time against CTRL	t_{S4CICT}	in Mode 4	6		t_{CYK}
CI0/CI1 Hold Time from CTRL	t_{H4CTCI}	in Mode 4	6		t_{CYK}
CI0/CI1, CTRL0/CTRL1 Cycle Time	t_{CYC4}	in Mode 4		250	KHz

Other Operation

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter		Symbol	Test Conditions	Min.	Max.	Units
NMI	Input High/Low	t_{WNIH}, t_{WNIL}		10		μs
INTE0	Input High/Low	t_{WI0H}, t_{WI0L}		3		t_{CYK}
INTE1	Input High/Low	t_{WI1H}, t_{WI1L}		3		t_{CYK}
INTE2	Input High/Low	t_{WI2H}, t_{WI2L}		3		t_{CYK}
RESET	Input High/Low	t_{WRSH}, t_{WRSL}		10		μs
V_{DD}	Rising/Falling Time	t_{RVD}, t_{FVD}		200		μs

External clock timing

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter		Symbol	Test Conditions	Min.	Max.	Units
X1	Input High Width	t_{WXH}		30	130	ns
X1	Input Low Width	t_{WXL}		30	130	ns
X1	Rise Time	t_{XR}		0	30	ns
X1	Fall Time	t_{XF}		0	30	ns
X1	Cycle Time	t_{CYX}		83	250	ns

Definition of bus timing on t_{CYK}:

Item	Expression	Min./Max.	Unit
t_{SAL}	1.5T – 100	Min.	ns
t_{DAR}	2T – 100	Min.	ns
t_{DAID}	(3.5 + n)T – 170	Max.	ns
t_{DLID}	(2 + n)T – 100	Max.	ns
t_{DRID}	(1.5 + n)T – 70	Max.	ns
t_{DLR}	0.5T – 20	Min.	ns
t_{DRL}	T – 50	Min.	ns
t_{DRA}	0.5T – 30	Min.	ns
t_{WRL}	(1.5 + n)T – 50	Min.	ns
t_{WLH}	T – 40	Min.	ns
t_{DAW}	2T – 100	Min.	ns
t_{DLOD}	0.5T + 110	Max.	ns
t_{DLW}	0.5T – 20 (normal operation)	Min.	ns
	T – 50 (refresh mode)	Min.	ns
t_{SODWR}	(1.5 + n)T – 100	Min.	ns
t_{SODWF}	0.5T – 50	Min.	ns
t_{DWL}	T – 50	Min.	ns
t_{WWL}	(1.5 + n)T – 50	Min.	ns

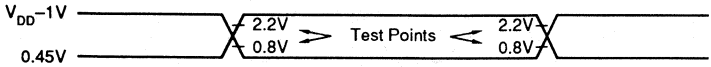
Remarks:

1. n represents the number of wait cycles to be inserted according to the MM register specification.

2. $T = t_{CYK} = 1/f_{CLK}$ (f_{CLK} is the internal system clock frequency.)

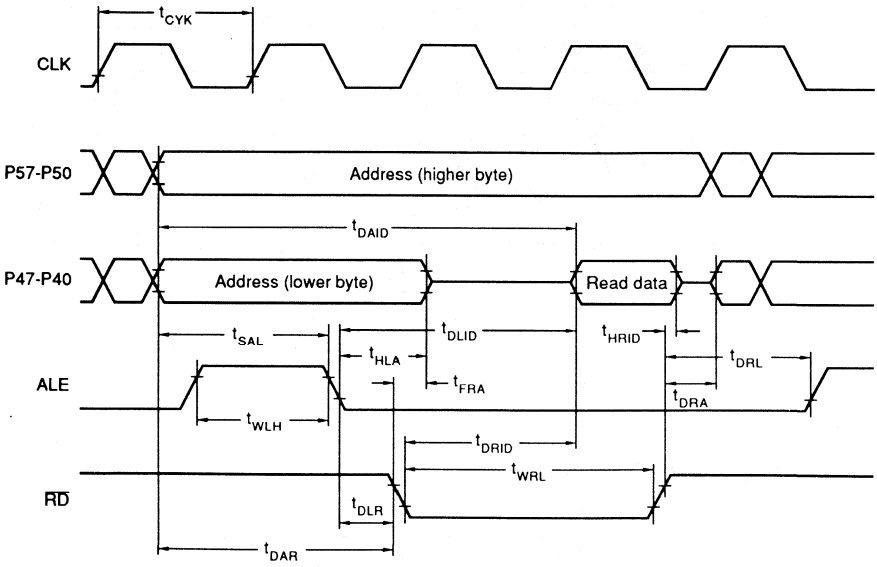
3. Items other than listed above are not dependent on the internal system clock frequency (f_{CLK}).

AC timing test points

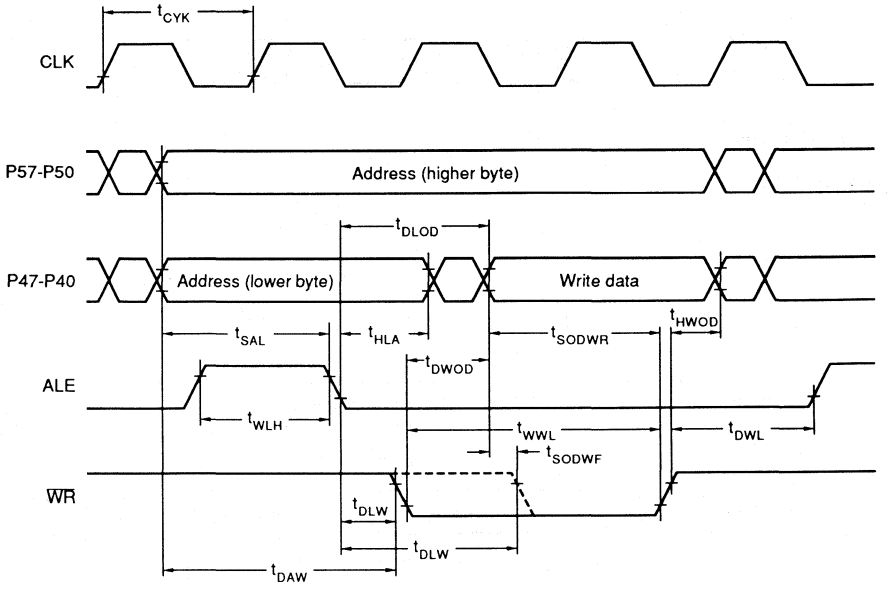


Timing Waveform

Read operation:

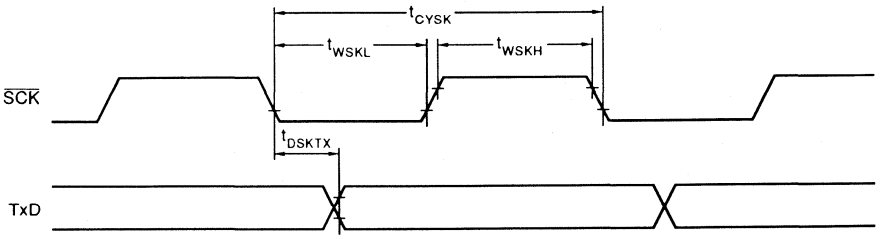


Write operation

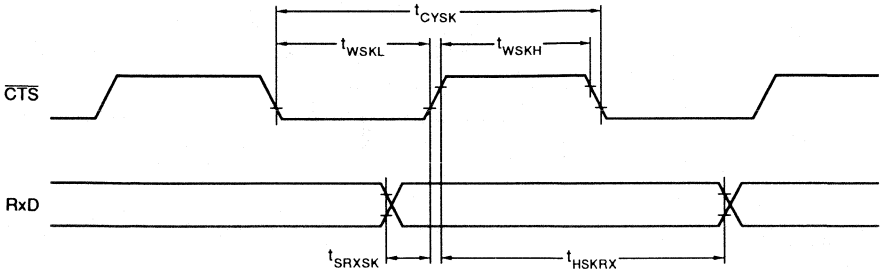


Serial Operation Timing

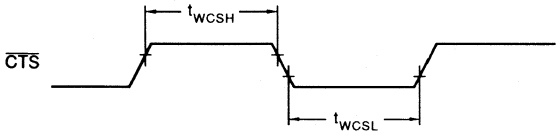
Send operation in the I/O interface mode:



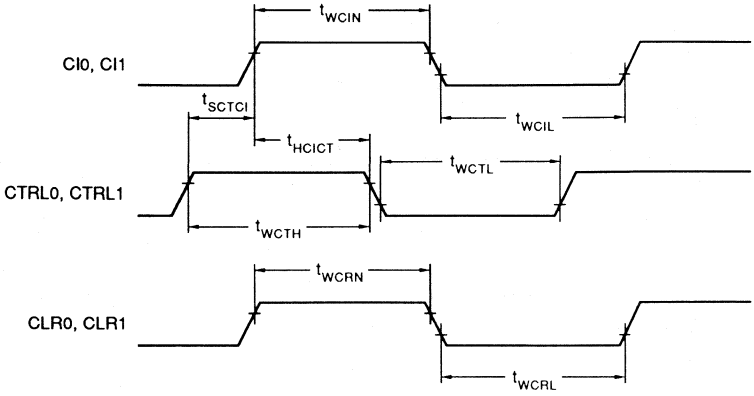
Receive operation in the I/O interface mode:



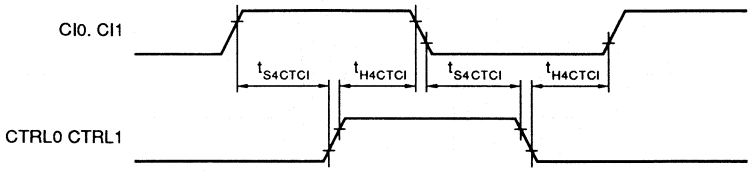
Send enable input timing (asynchronous mode):



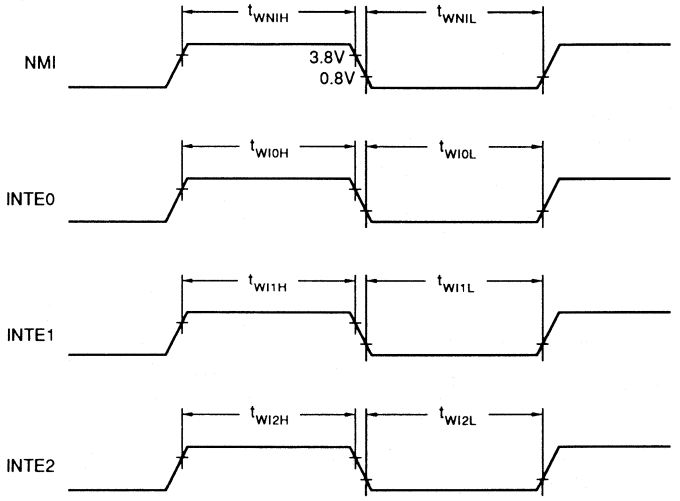
Up/Down Counter Input Timing



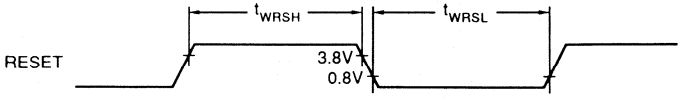
Up/Down Counter in Mode 4 (78310A/312A only)



Interrupt Input Timing

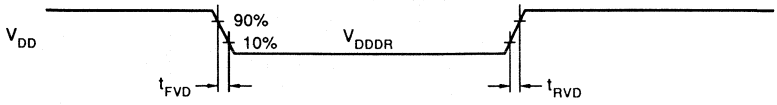


Reset Input Timing

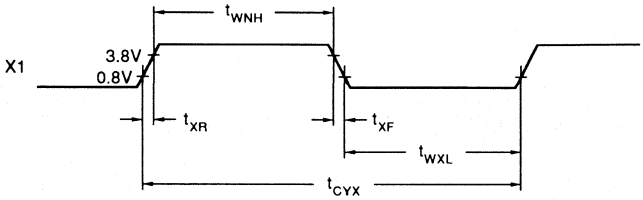


Rise/Fall Time of V_{DD} (only for 78310A/312A)

Data Retention Timing

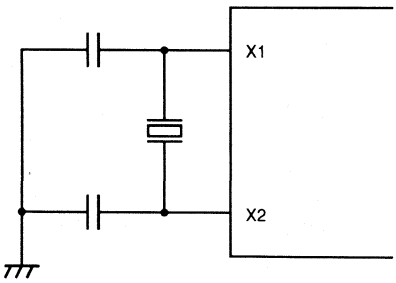


External Clock Timing

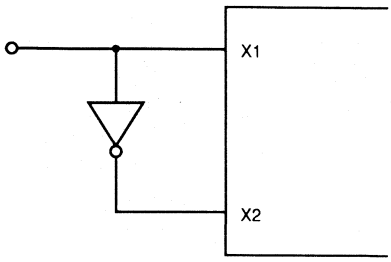


X1, X2 Input Connection

A) Crystal Connection

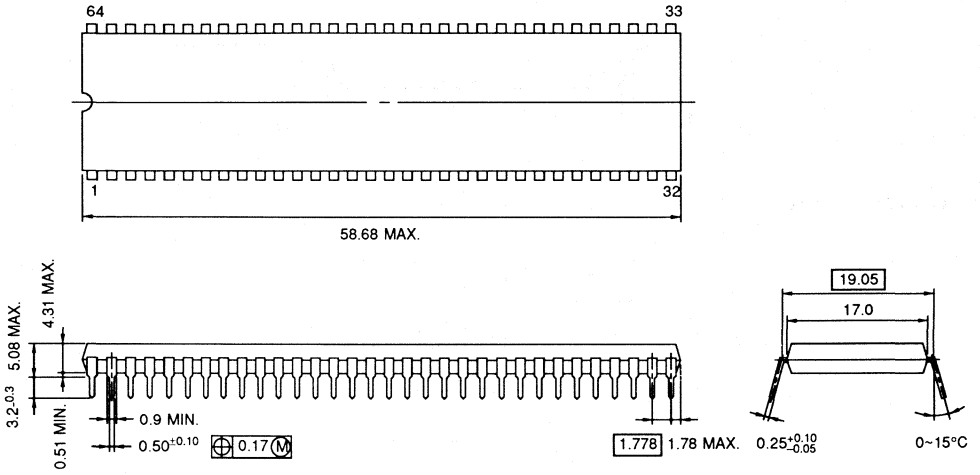


B) External Clock Supply



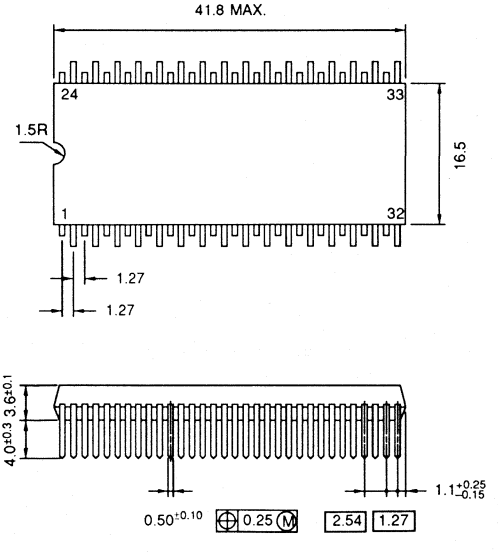
Package Dimensions (unit: mm)

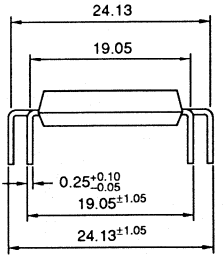
64-Pin SDIP



P64C-70-750A.C

64-Pin QUIP

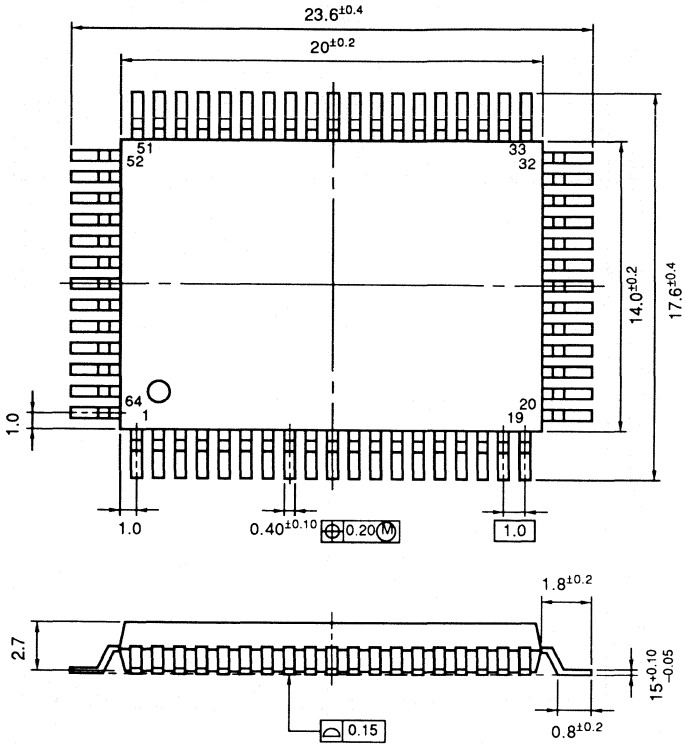




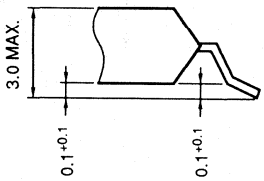
P64GQ-100-36

Package Dimensions (unit: mm)

64-Pin Flat Pack (QFP, 14 x 20)



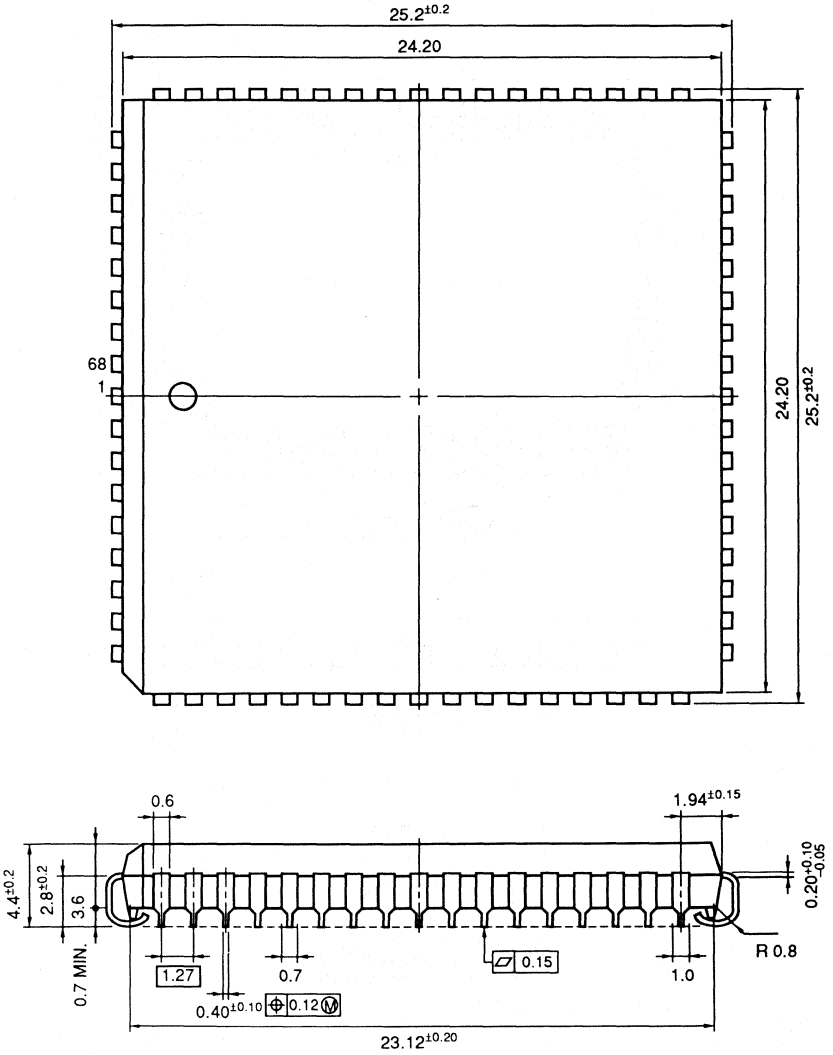
Detail of Pin Shape



P64GF-100-3B8, 3BE

Package Dimensions (unit: mm)

68-Pin PLCC



P68L-50A

Description

μPD78P312A is a 16-/8-bit single-chip microcomputer having the same functions as μPD78312A, except that the internal mask ROM of μPD78312A is replaced with one-time ROM or EPROM. Allowing data to be written only once, the one-time EPROM product is suited for small-scale production of various types of products, or early development of the application system. The EPROM version allows programs to be written more than once and is ideal for system evalution.

Features

- Compatible with μPDA78312A
  - Can be replaced with μPD78312A, which integrates mask ROM, when the application system is mass-produced
- Internal PROM: 8,192 x 8 bits
  - Data can be written only once (one-time PROM product without window)
  - Erasable by ultraviolet ray. Electrically rewritten (EPROM product with window)
- PROM programming characteristics:
  Compatible with μPD27C256A
  Can be written with general-purpose PROM writer

Ordering Information

Part Number	Package Type	ROM
μPD78P312ADW	64-Pin SDIP	8-K UVPROM
μPD78P312AR	64-Pin QUIP ceramic with window	
μPD78P312ACW	64-Pin SDIP	8-K OTPROM
μPD78P312AGQ-36	64-Pin QUIP	
μPD78P312AGF	64-Pin QFP	
μPD78P312AL	68-Pin PLCC	

SDIP = Shrink dual-in-line package
QUIP = Quad-in-line package/Bent Leads
QFP = Quad-Flat Pack (SMD)
PLCC = Plastic Leaded chip carrier

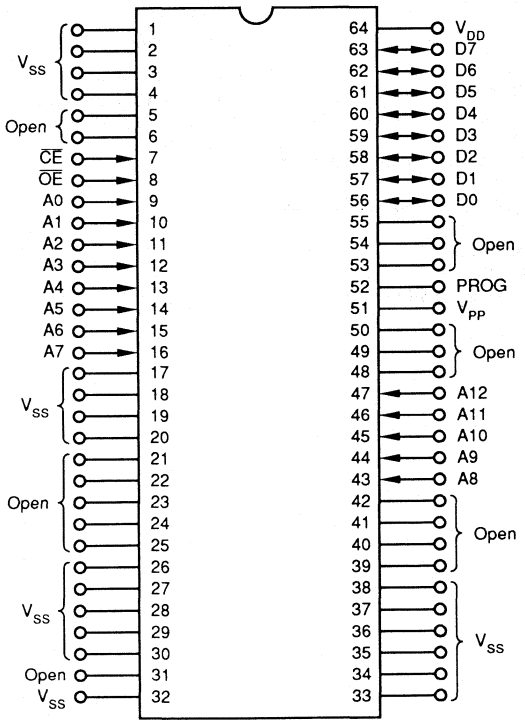
2

Pin Configuration (top view)

For the pin configurations in normal mode and detailed description of all pin functions please refer to μPD78310A/312A data sheet. Below all pin functions and pin configurations for the programming mode are given.

EPROM programming mode

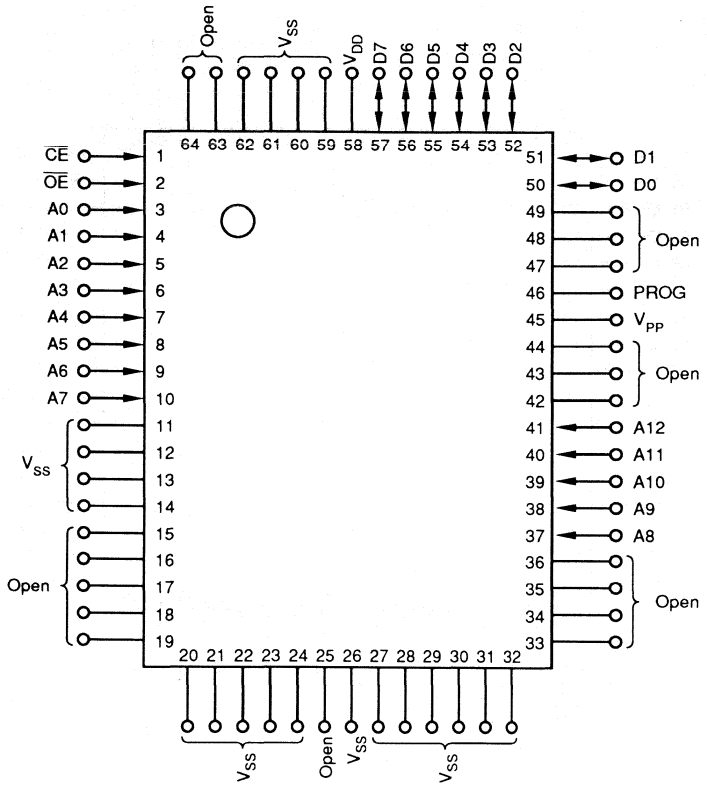
(a) 64-pin plastic shrink DIP/QUIP
64-pin shrink DIP/QUIP ceramic window



Note: 1. V_{SS} : Ground this pin.
2. Open : Do not connect this pin.

A0-A12	:	Address Bus	$\overline{CE}$	:	Chip Enable
D0-D7	:	Data Bus	$\overline{OE}$	:	Output Enable
PROG	:	Program	V_{PP}	:	Program Power Supply

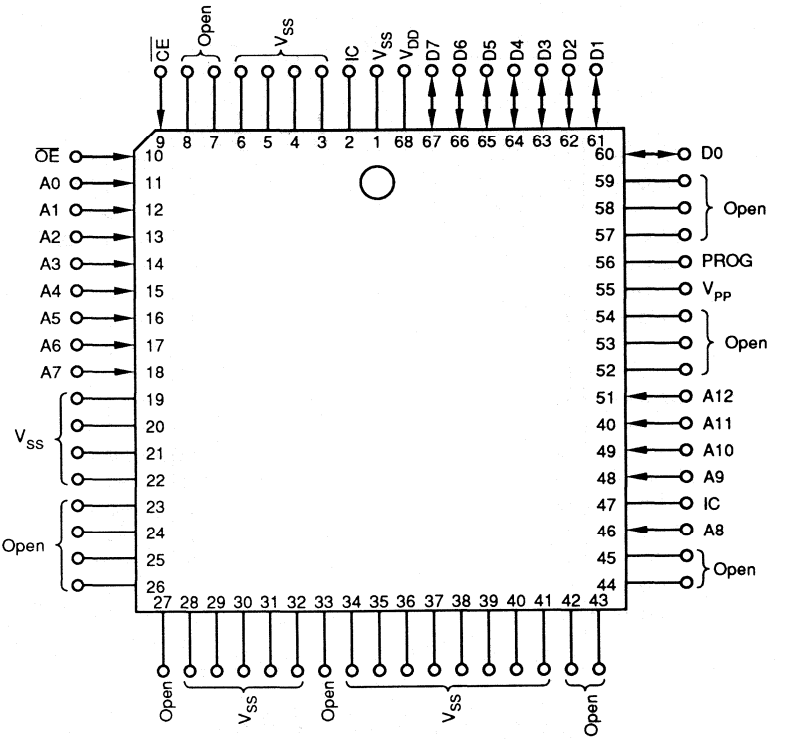
(b) 64-pin plastic QFP (bent leads)



Note: 1. V_{SS} : Ground this pin.
2. Open : Do not connect this pin.

2

(c) 68-pin PLCC



Note: 1. V_{SS} : Ground this pin.
2. Open : Do not connect this pin.

Pins used in EPROM programming mode

Pin name	Input/Output	Shared pin (Note)	Function
A0-A7	Input	P10-P17	Address input pins
A8-A12		P50-P54/A8-A12	
D0-D7	Input/Output	P40-P47/AD0-AD7	Data input/output pins
$\overline{CE}$	Input	P06	Chip-enable input pin/program pulse input pin
$\overline{OE}$	Input	P07	Output-enable input pin
PROG		$\overline{RESET}$	EPROM programming mode set pin
V_{PP}		–	Program write/verify high voltage application pin
V_{DD}		–	Positive power supply pin
V_{SS}		–	GND

2

Recommended Conditions for Unused Pins

Pin	Recommended connection
P00-P07 P10-P17	Input mode: Connect to V_{DD} through a pull-up resistor Output mode: Open
P20-P23	Connect to V_{SS}
P30-P33	Connect to either V_{SS} or V_{DD}
P24-P27 P34-P37 P40-P47 P50-P57	Input mode: Connect to V_{DD} through a pull-up resistor Output mode: Open
$\overline{WR}$ $\overline{RD}$ ALE $\overline{RFSH}$	Open
AN0-AN3 AV_{REF} AV_{SS}	Connect to either V_{SS} or V_{DD} (Note)

Note: When not using the A/D converter, AV_{REF} and AV_{SS} should be set to the same level.

Comparison of Family Products

The μPD78P312A is a version of the μPD78312A in which the internal mask ROM is replaced with an one-time PROM or EPROM. The μPD78P312A is an upgraded version of the μPD78312. A comparison of the three products, μPD78P312A,μPD78312A, and μPD78310A is shown in the table below. These products are identical with respect to function, except the few diferences listed below.
Refer to the documents provided for the μPD78312A and μPD78310A for details concerning the internal hardware such as CPÜ functions.

Comparison of μPD78P312A, μPD78312A, and μPD78310A

Item		μPD78P312A	μPD78312A	μPD78310A
Program memory		• PROM • 8.192 x 8 bits	• Mask ROM • 8.192 x 8 bits	• Not internally provided
Pin function	PROM programming mode	Provided	None	
	Ports 4, 5	Provided	Provided	None (These ports always serve as the address bus, data bus)
	$\overline{EA}$	None	Provided	Provided (However, must be operated with this pin set to low)
External memory access		External memory can be expanded in steps by 256 bytes, 4K bytes, 16K bytes, or 56K bytes, using the memory expansion mode register (MN).		Always accesses 64K bytes of the externalmemory (regardless of the setting in the memory expansion mode register (MN).
Package	Without window	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QUIP • 64-pin plastic QFP (14 x 20) • 68-pin PLCC		
	With window	• 64-pin ceramic shrink DIP with window (750 mil) • 64-pin ceramic QUIP with window	None	

Difference Between μPD78P312A and μPD78P312

Item	μPD78P312A	μPD78P312
Mode 4 in count unit (4 x multiplication mode)	Provided	Not provided
Count start triggered by external pulse of interval timer	Provided	Not provided
16 bit data transfer instruction used between memory and a pair register • MOVW rpl, !addr 16 instruction • MOVW !addr 16, rpl instruction	Provided	Not provided

PROM Programming

The ROM contained in μPD78P312A is an electrically erasable PROM with 8,192 x 8 bit configuration. The pins listed in the table below are used to program the PROM.
When used in the normal operation mode, 5V ±10% is applied to the V_{DD} and V_{PP} pins. A voltage higher than V_{DD} should not be applied to other pins.
The programming characteristics of the μPD78P312A are identical to those of the μPD27C256A.

Pin Name	Function
V_{PP}	High voltage input (write/verify mode), high level input (read mode)
PROG	High voltage input (write/verify mode, read mode)
A0-A7	Address input (lower 8 bits)
A8-A12	Address input (upper 8 bits)
D0-D7	Data input (write mode), data output (verify mode)
$\overline{CE}$	Program pulse input
$\overline{OE}$	Output enable input
V_{DD}	Power supply pin

Note:
1. Attach a light baffle film to μPD78P312A with an erase window to protect the EPROM from being erased accidentally.
2. The one-time PROM product, μPD78P312A, cannot be erased by ultraviolet rays, because it is not provided with a window.

PROM programming Mode

When +6V is applied to the V_{DD} pin and +12.5V is applied to the PROG pin and V_{PP} pin, the μPD78P312A enters the program write/verify mode. Operation in thismode is dtermined according to the setting of $\overline{CE}$ and $\overline{OE}$ pins as indicated in the table below. Additionally, when set to the read mode, the μPD78P312A can read the contents of PROM.

Operation mode specification					Operation mode	
V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	PROG		
+12.5V	+6V	L	H	+12.5V	Write mode	
		H	L		Verify mode	
		H	H		Program inhibit mode	
$V_{PP} = V_{DD} = +5V$		L/H	L		Read mode	Data is output from the D0-D7 pins
			H			D0-D7 are high impedance

Remarks: H indicates high level; L indicates low level.

Notes: When +12.5V is applied to V_{PP} and +6V is applied to V_{DD}, both $\overline{CE}$ and $\overline{OE}$ must not be set to low level (L) simultaneously.

Recommended Conditions for Unused Pins

The table below describes how to set unused pins when programming the PROM.

Recommended Conditions for Unused Pins

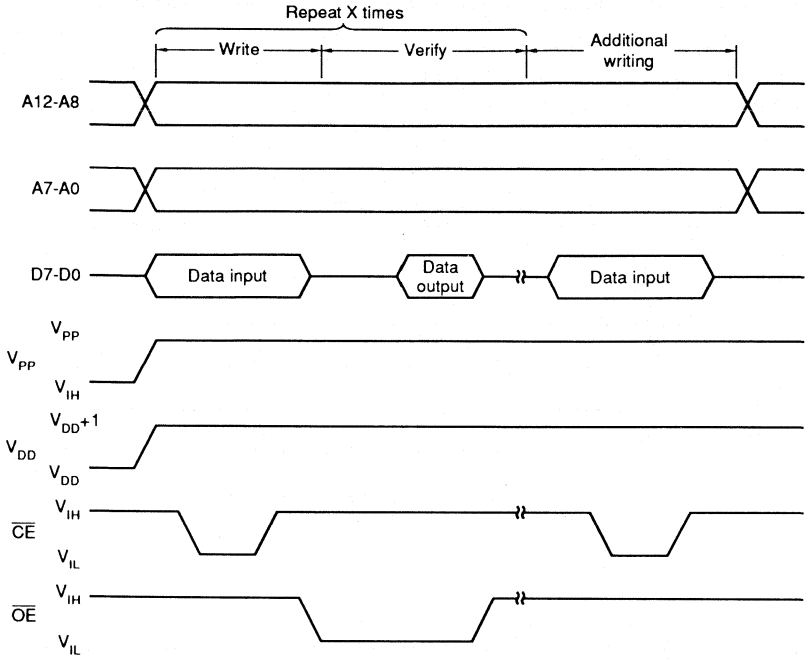
Pin	Recommended Connection
P00-P03	Connect to V_{SS}
P04, P05	Open
P20-P23	Connect to V_{SS}
P25-P27 $\overline{RFSH}$	Open
P30-P33 X1	Connect to V_{SS}
X2	Open
AN0-AN3 AV_{REF}, AV_{SS}	Connect to V_{SS}
P34-P37 P55-P57 $\overline{RD}$, $\overline{WR}$ ALE	Open

Prom Write Procedure

Data can be written to the PROM using the following procedure. High speed data write operation is possible.

(1) Set the pins not used programming as indicated in previous Table, and supply +6V to the V_{DD} pin and +12.5V to the V_{PP} pin.
(2) Provide the initial address.
(3) Provide write data.
(4) Provide a 1ms program pulse (active low) to the $\overline{CE}$ pin.
(5) Verify mode. If the data has been written, proceed to (7), if not, repeat steps (3) to (5). If the data cannot be correctly written in 25 attempts, go to step (6).
(6) Classify the PROM as defective and cease write operation.
(7) Provide write data and supply (for additional writing) program pulses for 3ms times the number of repeats performed between steps (3) and (5).
(8) Increment the address.
(9) Repeat steps (3) to (8) until the end address is reached.

PROM Write/Verify Timing



2

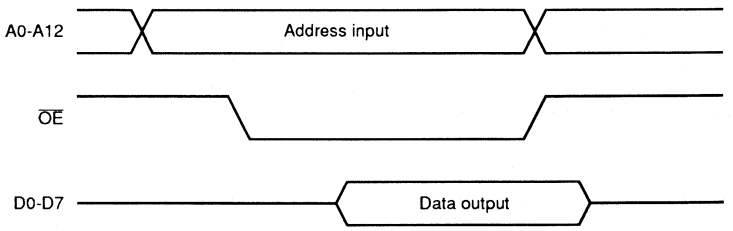
PROM Read Procedure

The contents of the PROM can be read out to the external data bus (D0-D7) using the following procedure.

(1) Set the unused pins as indicated in previous Table.
(2) Supply +5V to the V_{DD} pin, and +12.5V to the PROG pin.
(3) Input the address of the data to be read to the A0 to A12 pins.
(4) Read mode.
(5) Data is output to the D0 to D7 pins.

The figure below shows the timing for this sequence from steps (2) to (5).

PROM Read Timing



Erasing Procedure (EPROM product only)

Data on the μPD78P312ADW/R EPROM can be erased by exposing the EPROM to light with a wavelength shorter than 400nm. Therefore, if the EPROM is exposed to direct sunlight or the light of a fluorescent lamp for a long time, the data on the EPROM may be erased. To protect the data, mask the EPROM window with a light baffle film, which is attached as an accessory. Usually, cast a 254nm ultraviolet ray onto the window of the EPROM to erase the memory contents. To completely erase the EPROM contents, a minimum of 15W.s/cm^2 (strength of the ultraviolet light x erase time) of exposure is necessary. This means that, when a 12,000μW/cm^2 ultraviolet lamp is used, about 15 to 20 minutes are required to completely erase the EPROM contents. The time required to erase the EPROM contents, however, may be lengthened if the life of the ultraviolet lamp used is ending, or if the window of the EPROM is soiled. The distance between the ultraviolet lamp and the window should be 2.5cm or shorter.

Absolute Maximum Ratings
Ta = 25°C

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5~+7.0	V
	AV_{REF}		-0.5~V_{DD}+0.3	V
	AV_{SS}		-0.5~+0.5	V
	V_{PP}		-0.5~+13.5	V
Input Voltage	V_{I1}	Other than $\overline{RESET}$ Pin	-0.5~V_{DD}+0.5	V
	V_{I2}	$\overline{RESET}$	-0.5~+13.5	V
Output Voltage	V_O		-0.5~V_{DD}+0.5	V
Output Current Low	I_{OL}	at 1 Pin	4.0	mA
		All Output Pins Total	60	mA
Output Current High	I_{OH}	at 1 Pin	- 1	mA
		All Output Pins Total	-15	mA
Operating Temperature	T_{opt}		-10~+70	°C
Storage Temperature	T_{stg}		-65~150	°C

Operating Conditions

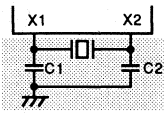
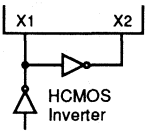
Parameter / Osc. Freq.	Condition	Ta	V_{DD}
4MHz≤f_{XX}≤12MHz		-10~+70°C	+5.0V±10%

Capacitance (Ta=25°C,V_{DD}=V_{SS}=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f=1MHz pins not used for measurement are at 0V.			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	C_{IO}				20	pF

Oscillator characteristics

(Ta = -10 to +70°C, $V_{DD} = AV_{DD} = +5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0V$, $4.0V \le AV_{REF} \le V_{DD}$)

Oscillator	Recommended circuit	Item	Min.	Max.	Unit
Ceramic resonator or crystal resonator (Note)		Oscillator frequency (f_{XX})	4	12	MHz
External clock		X1 input frequency (f_X)	4	12	MHz
		X1 input rise, fall time (t_{XR}, t_{XF})	0	30	ns
		X1 input high/low level widths (t_{WXH}, t_{WXL})	30	130	ns

Notes 1: Oscillator circuit must be located as close as possible to the X1 and X2 pins.
2: To prevent noise from affecting operation, avoid locating other signal lines within the shaded area.

Note: When using a crystal resonator, the following external capacitor is recommended.
C1 = C2 = 15pF

DC Characteristics

Ta=-10°C to +70°C, $V_{DD}=5.0V\pm10\%$, $V_{ss}=0V$

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except X2, X1, $\overline{RESET}$, P20/NMI	2.2		V_{DD}	V
	V_{IH2}	X2, X1, $\overline{RESET}$, P20/NMI	3.8		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL}=2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH}=-1mA	V_{DD}-1			V
Input Current	I_I	$\overline{RESET}$, P20/NMI, $0.45V<V_I<V_{CC}$			±10	μA
Input Leakage Current	I_{LI}				±10	μA
Output Leakage Current	I_{LO}				±10	μA
AV_{REF} Current	AI_{REF}	f_{CLK}=6MHz		1.5	5	mA
V_{DD} Supply Current	I_{DD1}	Operation Mode, f_{CLK}=6MHz		30	60	mA
	I_{DD2}	Halt Mode, f_{CLK}=6MHz		5	15	mA
Data Retention Current	I_{DDDR}	STOP mode, V_{DDDR}=2.5V		3	15	μA
		STOP mode, V_{DDDR}=5.0±10%		10	50	μA
Data Retention Voltage	V_{DDDR}	Stop Mode	2.5			V

AC Characteristics

Read/Write Operation Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{SS}=0V

Parameter	Symbol	Test Conditions	Min.	Max.	Units
Internal System Clock *1	t_{CYK}		166		ns
Address Setup to ALE ↓	t_{SAL}		150		ns
Address Hold from ALE ↓	t_{HLA}		30		ns
Address to $\overline{RD}$ ↓ delay time	t_{DAR}		230		ns
$\overline{RD}$ ↓ to Address floating	t_{FRA}			0	ns
Address to Data output	t_{DAID}			410	ns
ALE ↓ to Data Input	t_{DLID}			230	ns
$\overline{RD}$ ↓ to Data Input	t_{DRID}			180	ns
ALE ↓ to$\overline{RD}$ ↓ Delay Time	t_{DLR}		60		ns
Data Hold Time from $\overline{RD}$ ↑	t_{HRID}		0		ns
$\overline{RD}$ ↑ to Address active	t_{DRA}		50		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{DRL}		100		ns
$\overline{RD}$ Width Low	t_{WRL}		200		ns
ALE Width High	t_{WLH}		120		ns
Address to $\overline{WR}$ ↓ Delay	t_{DAW}		300		ns
ALE ↓ to Data Output	t_{DLOD}			190	ns
$\overline{WR}$ ↓ to Data Output	t_{DWOD}			100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time*2	t_{DLW}		30		ns
		in Refresh Mode	110		ns
Data Setup Time to $\overline{WR}$ ↑	t_{SODWR}		150		ns
Data Setup Time to $\overline{WR}$ ↓ *3	t_{SODWF}	in Refresh Mode	30		ns
Data Hold Time from $\overline{WR}$ ↑	t_{HWOD}		20		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{DWL}		110		ns
$\overline{WR}$ Width Low	t_{WWL}		200		ns

Notes:

*1: The internal system clock (f_{CLK}) is the oscillation clock (f_{XX}) divided by 2 or 8, depending on the STBC register specification. The value in this table is indicated as f_{XX} = 12MHz and $f_{CLK} = f_{XX}/2$.

*2: During pulse refresh operation, the falling edge of the WR signal is delayed by a half clock. Therefore, the value in the lower row is used as the value of t_{DLW}.

*3: When accessing a pseudo-static RAM (μPD4168 etc.) from which the data is clocked in at the falling edge of the WR signal, the data set up time is not t_{SODWR}, but t_{SODWF}.

Serial Operation

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{SS}=0V

Parameter	Symbol	Test Conditions			Min.	Max.	Units
$\overline{SCK}$ Cycle Time	t_{CYSK}	Output	$\overline{SCK}$	*1	1.33		μs
			$\overline{CTS}$	*2	1.33		μs
		Input	$\overline{CTS}$	*3	1		μs
$\overline{SCK}$ Width Low	t_{WSKL}	Output	$\overline{SCK}$	*1	580		ns
			$\overline{CTS}$	*2	580		ns
		Input	$\overline{CTS}$	*3	420		ns
$\overline{SCK}$ Width High	t_{WSKH}	Output	$\overline{SCK}$	*1	580		ns
			$\overline{CTS}$	*2	580		ns
		Input	$\overline{CTS}$	*3	420		ns
$\overline{CTS}$ Width High/Low	t_{WCSH} t_{WCSL}			*4	3		t_{CLK}
RxD Setup Time to $\overline{CTS}$ ↑	t_{SRXSK}				80		ns
RxD Hold Time from $\overline{CTS}$ ↑	t_{HSKRX}				80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{DSKTX}					210	ns

Notes:
*1: I/O interface mode transmission, data transfer speed 750 kbps
*2: I/O interface mode reception, data transfer speed 750 kbps
*3: I/O interface mode reception, data transfer speed 1 Mbps
*4: Asynchronous mode

A/D Converter Characteristics

Ta=-10°C to +70°C, V_{SS}=AV_{SS}=0V, 4.0V≤V_{AREF}≤V_{DD}, V_{DD}=+5V±10%

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Resolution			8			Bit
Full Scale Error		4.0≤AV_{REF}≤V_{DD}, 166ns≤t_{CYC}≤500ns			0.4	%
		166ns ≤ t_{CYK} ≤ 500ns			0.8	%
Quantization Error					±1/2	LSB
Conversion Time	t_{CONV}	166ns ≤ t_{CYK} ≤ 250ns	180			t_{CYK}
		250ns ≤ t_{CYK} ≤ 500ns	120			t_{CYK}
Sampling Time	t_{SAMP}	166ns ≤ t_{CYK} ≤ 250ns	36			t_{CYK}
		250ns ≤ t_{CYK} ≤ 500ns	24			t_{CYK}
Input Voltage	V_{IAN}		0		AV_{REF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
Analog Reference Voltage	AV_{REF}		4.0		V_{DD}	V
AV_{REF} Current	AI_{REF}	f_{CLK} = 6MHz		1.5	5.0	mA

Up/Down Counter Input

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions	Min.	Max.	Units
CI0, CI1 Hjgh/Low Time	t_{WCIH}, t_{WCIL}		3		t_{CYK}
CTRL0, CTRL1 High/Low Time	t_{WCTH}, t_{WCTL}		3		t_{CYK}
CTRL0, CTRL1 Setup Time against CI ↑	t_{SCTCI}	in Mode 3, CI programmed on rising edge	2		t_{CYK}
CTRL0, CTRL1 Hold Time against CI ↑	t_{HCICT}	in Mode 3, CI programmed on rising edge	5		t_{CYK}
CLR0, CLR1 High/Low Time	t_{WCRH}, t_{WCRL}		3		t_{CYK}
CI0/CI1 Setup Time against CTRL	t_{S4CICT}	in Mode 4	6		t_{CYK}
CI0/CI1 Hold Time from CTRL	t_{H4CTCI}	in Mode 4	6		t_{CYK}
CI0/CI1, CTRL0/CTRL1 Cycle Time	t_{CYC4}	in Mode 4	4		μs

Other Operation

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter		Symbol	Test Conditions	Min.	Max.	Units
NMI	Input High/Low	t_{WNIH}, t_{WNIL}		10		μs
INTE0	Input High/Low	t_{WI0H}, t_{WI0L}		3		t_{CYK}
INTE1	Input High/Low	t_{WI1H}, t_{WI1L}		3		t_{CYK}
INTE2	Input High/Low	t_{WI2H}, t_{WI2L}		3		t_{CYK}
$\overline{RESET}$	Input High/Low	t_{WRSH}, t_{WRSL}		10		μs
V_{DD}	Rising/Falling Time	t_{RVD}, t_{FVD}		200		μs

External clock timing

Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter		Symbol	Test Conditions	Min.	Max.	Units
X1	Input High Width	t_{WXH}		30	130	ns
X1	Input Low Width	t_{WXL}		30	130	ns
X1	Rise Time	t_{XR}		0	30	ns
X1	Fall Time	t_{XF}		0	30	ns
X1	Cycle Time	t_{CYX}		83	250	ns

2

Definition of bus timing depending on t_{CYK}:

Item	Calculation formula	Min./Max.	Units
t_{SAL}	1.5T – 100	Min.	ns
t_{DAR}	2T – 100	Min.	ns
t_{DAID}	(3.5 + n)T – 170	Max.	ns
t_{DLID}	(2 + n)T – 100	Max.	ns
t_{DRID}	(1.5 + n)T – 70	Max.	ns
t_{DLR}	0.5T – 20	Min.	ns
t_{DRL}	T – 50	Min.	ns
t_{DRA}	0.5T – 30	Min.	ns
t_{WRL}	(1.5 + n)T – 50	Min.	ns
t_{WLH}	T – 40	Min.	ns
t_{DAW}	2T – 100	Min.	ns
t_{DLOD}	0.5T + 110	Max.	ns
t_{DLW}	0.5T – 20 (Normal operation)	Min.	ns
	T – 50 (Refresh mode)	Min.	ns
t_{SODWR}	(1.5 + n)T – 100	Min.	ns
t_{SODWF}	0.5T – 50	Min.	ns
t_{DWL}	T – 50	Min.	ns
t_{WWL}	(1.5 + n)T – 50	Min.	ns

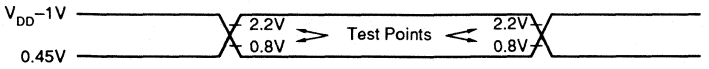
Remarks:

1. n is the number of WAIT states inserted by the specification in the MM register.

2. $T = t_{CYK} = 1/f_{CLK}$ (f_{CLK} is the internal system clock frequency.)

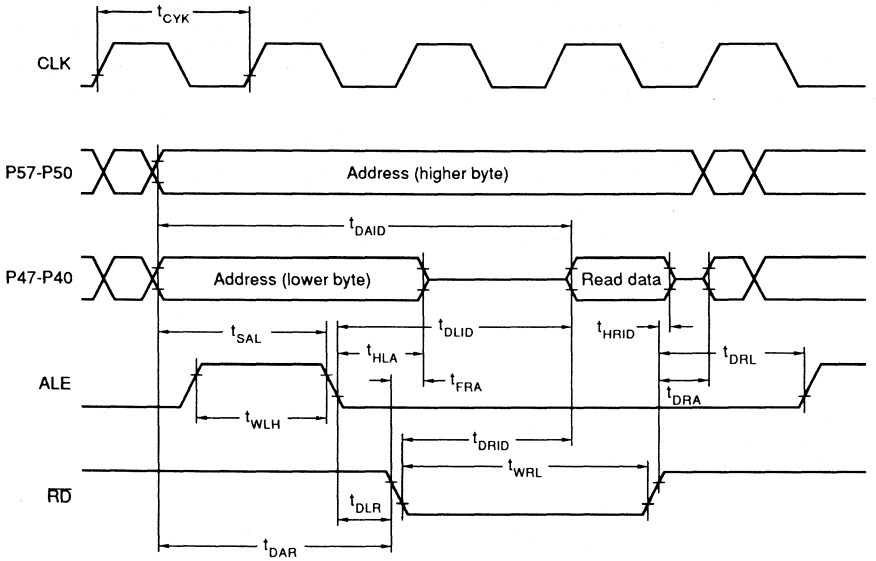
3. Items not shown in this table do not depend on the frequency of the internal system clock (f_{CLK}).

AC timing test points



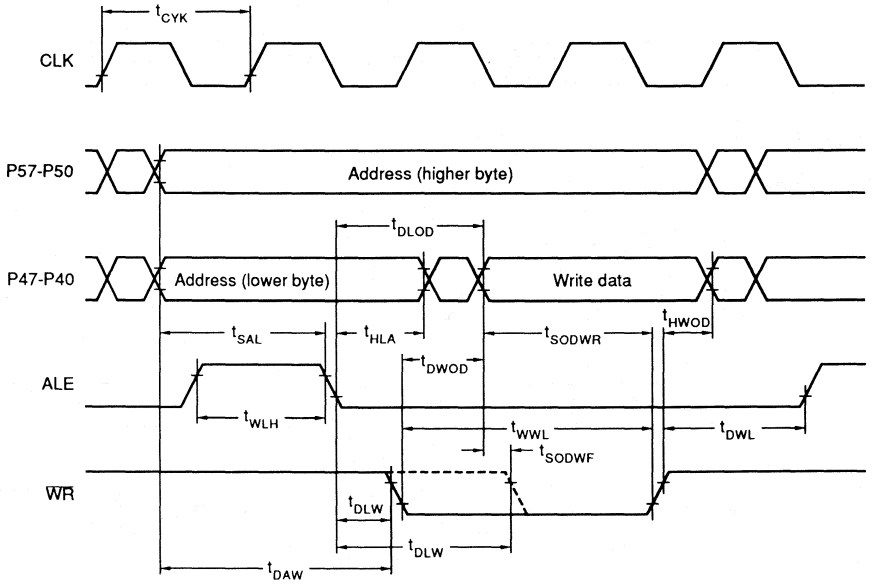
Timing Waveform

Read operation:



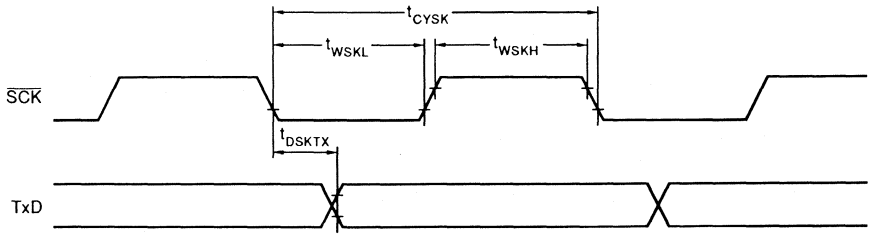
2

Write operation

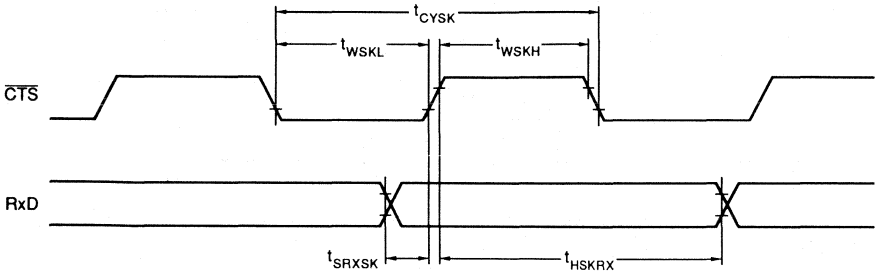


Serial Operation Timing

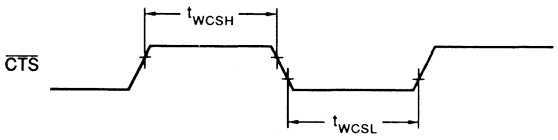
Transmission in I/O interface mode:



Receive in I/O interface mode:

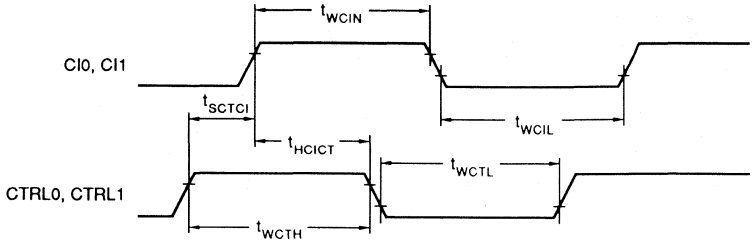


Transmit enable input timing (asynchronous mode):

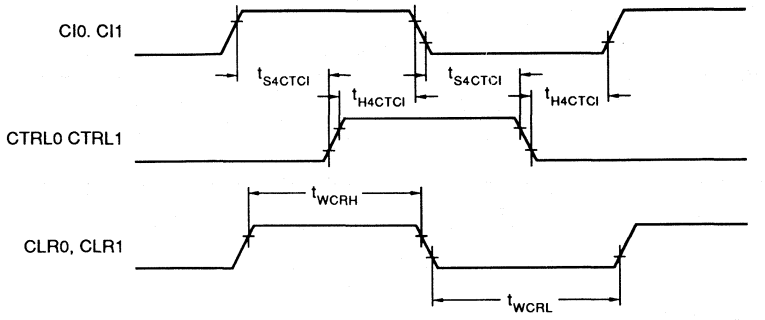


Count Unit Input Timing

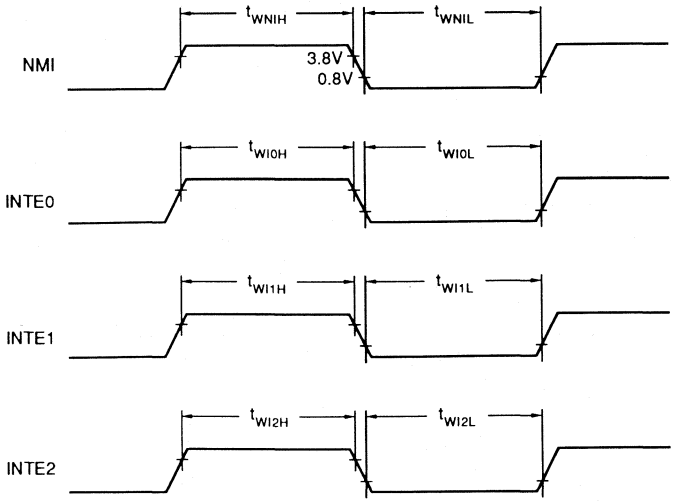
Mode 3 operation



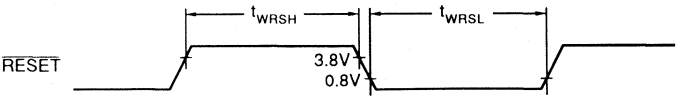
Mode 4 operation



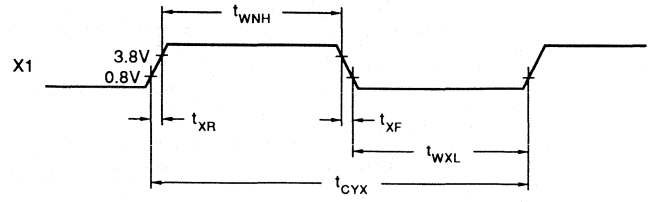
Interrupt Input Timing



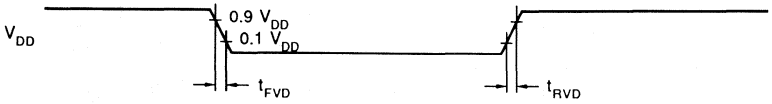
Reset Input Timing



External Clock Timing



Data Retention Timing



2

DC Programming Characteristics (Ta = 25 ±5°C, V_{IP} = 12.0 ± 0.5V, V_{SS} = 0V)

Parameter	Symbol	Symbol (Note)	Test Conditions	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}	V_{IH}		2.2		V_{DDP}+0.3	V
Input Low Voltage	V_{IL}	V_{IL}		–0.3		0.8	V
Input Leakage Current	V_{LIP}	V_{LI}	$0 \le V_I \le V_{DDP}$			10	μA
Output High Voltage	V_{OH}	V_{OH}	I_{OH} = –1mA	V_{DD}–1			V
Output Low Voltage	V_{OL}	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output Leakage Current	I_{LO}		$0 \le V_O \le V_{DDP}$, OE = V_{IH}			10	μA
PROG Pin High-Voltage Input Current	I_{IP}					±10	μA
V_{DDP} Supply Voltage	V_{DDP}	V_{DD}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	$V_{DD} = V_{DDP}$			V
V_{DDP} Supply Current	I_{DD}	I_{DD}	Program memory write mode		10	30	mA
			Program memory read mode CE = V_{IL}, V_I = V_{IH}		10	30	mA
V_{PP} Supply Current	I_{PP}	I_{PP}	Program memory write mode CE = V_{IL}, V_I = V_{IH}		10	30	mA
			Program memory read mode		1	100	μA

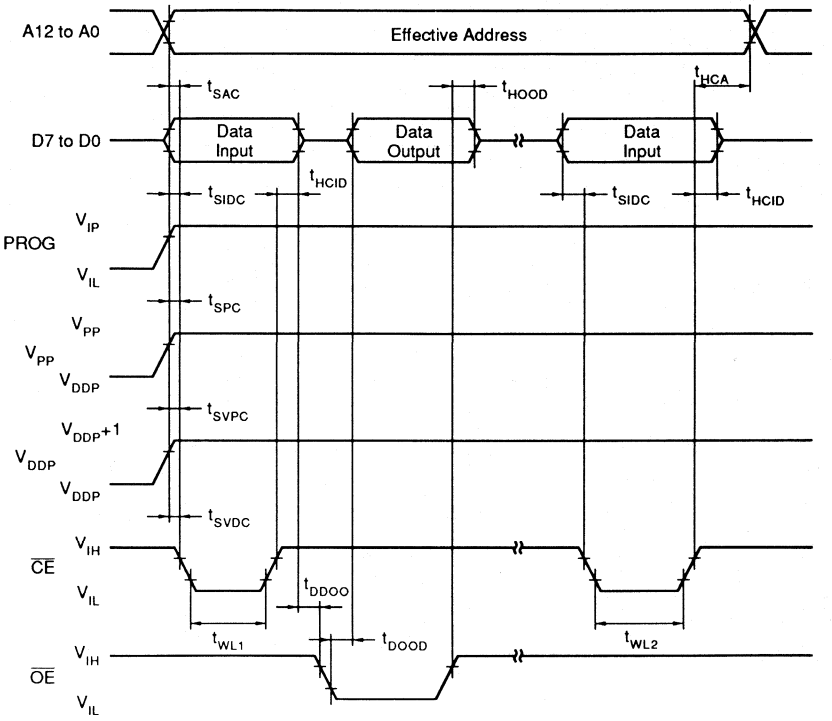
Note: Symbols of corresponding μPD27C256A

AC Programming Characteristics (Ta = 25 ±5°C, V_{IP} = 12.0 ± 0.5V, V_{SS} = 0V)

Parameter	Symbol	Symbol (Note)	Test Conditions	Min.	Typ.	Max.	Units
Address Setup Time (for $\overline{CE}$ ↓)	t_{SAC}	t_{AS}		2			μs
Data → $\overline{OE}$ ↓ Delay Time	t_{DDOO}	t_{OES}		2			μs
Input Data Setup Time (for $\overline{CE}$ ↓)	t_{SIDC}	t_{DS}		2			μs
Address Hold Time (for $\overline{CE}$ ↑)	t_{HCA}	t_{AH}		2			μs
Input Data Hold Time (for $\overline{CE}$ ↑)	t_{HCID}	t_{DH}		2			μs
Output Data Hold Time (for $\overline{CE}$ ↑)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} Setup Time (for $\overline{CE}$ ↓)	t_{SVPC}	t_{VPS}		2			μs
V_{DDP} Setup Time (for $\overline{CE}$ ↓)	t_{SVDC}	t_{VDS}		2			μs
Initial Program Pulse Width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Additional Program Pulse Width	t_{WL2}	t_{OPW}		2.85		78.75	ms
PROG High-Voltage Input Setup Time (for $\overline{CE}$ ↓)	t_{SPC}			2			μs
Address → Data Output Time	t_{DAOD}	t_{ACC}	$\overline{OE}$ = V_{IL}			2	μs
$\overline{OE}$ ↓ → Data Output Time	t_{DOOD}	t_{OE}				1	μs
Data Hold Time (for $\overline{OE}$ ↑)	t_{HCOD}	t_{DF}		0		130	ns
Data Hold Time (for address)	t_{HAOD}	t_{OH}	$\overline{OE}$ = V_{IL}	0			ns

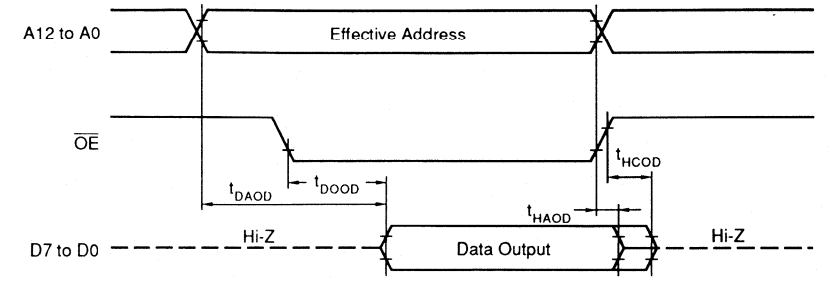
Note: Symbols of corresponding μPD27C256A

EPROM Write Mode Timings



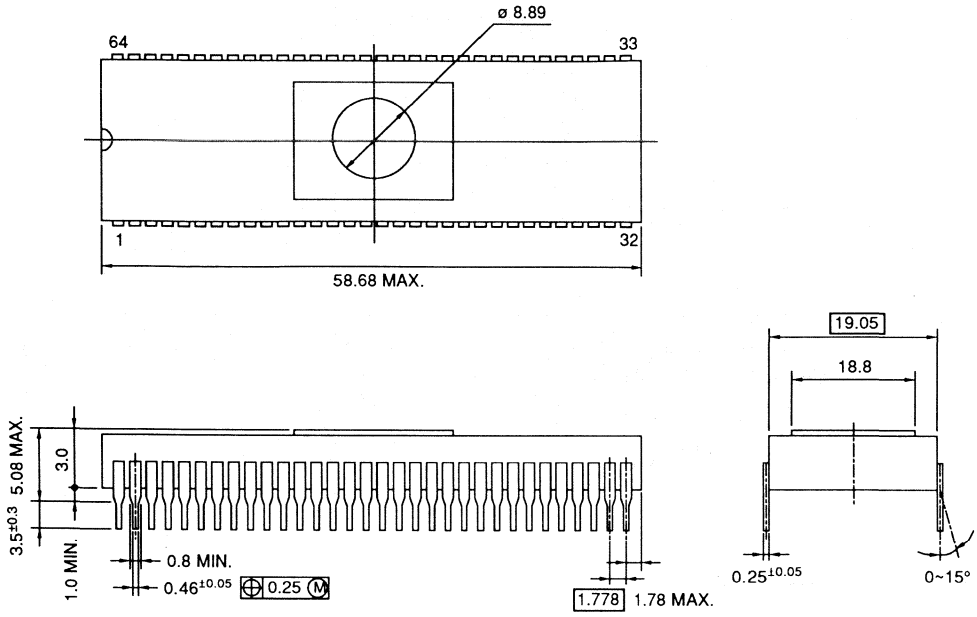
Note 1: Apply V_{DDP} before V_{PP} and cut it off after V_{PP}.
2: Set V_{PP} to +13V or less including an overshoot.

EPROM Read Mode Timing

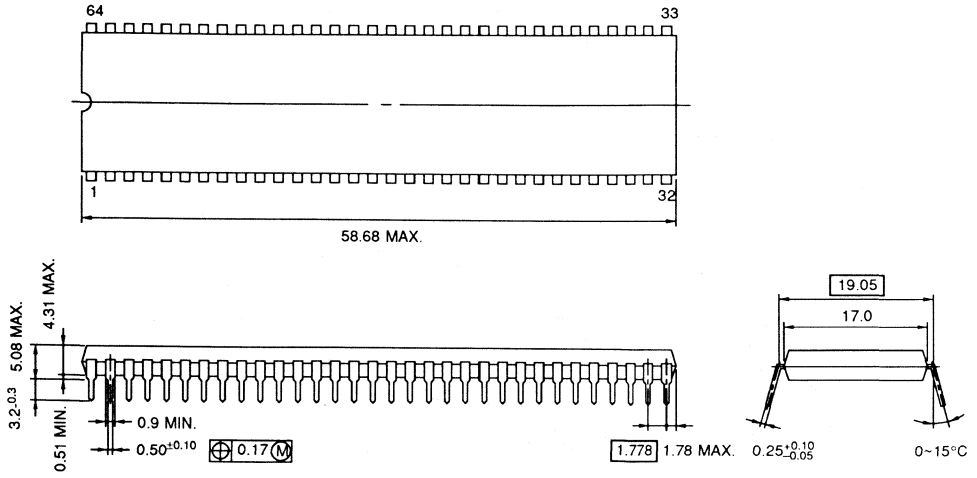


Package Dimensions (unit: mm)

64-Pin SDIP Ceramic

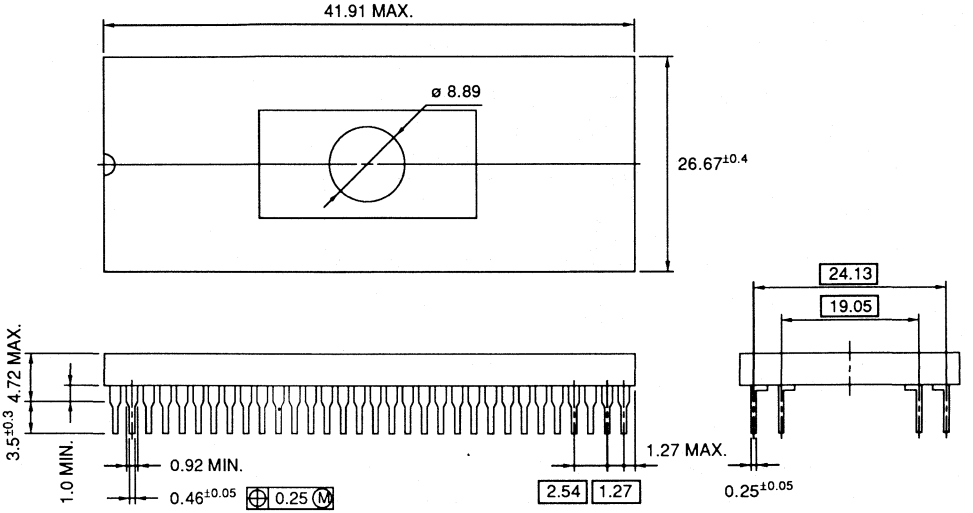


64-Pin SDIP Plastic (750 mil)



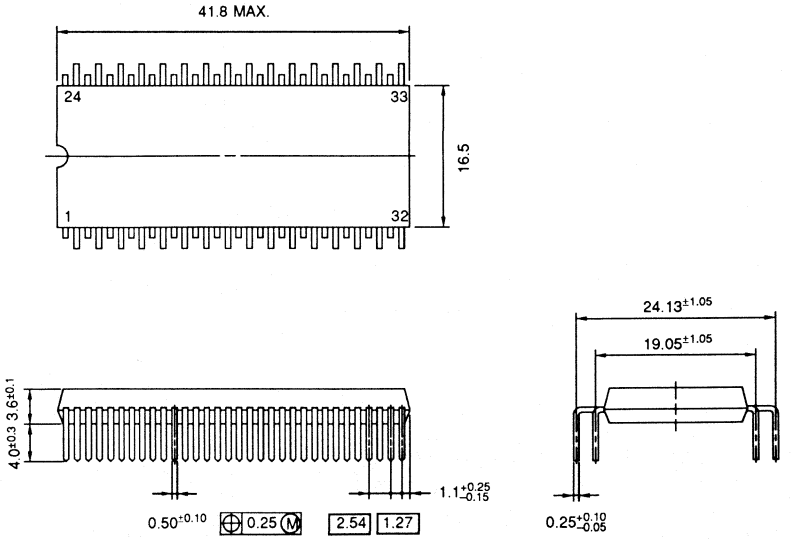
P64C-70-750A.C

64-Pin QUIP Ceramic



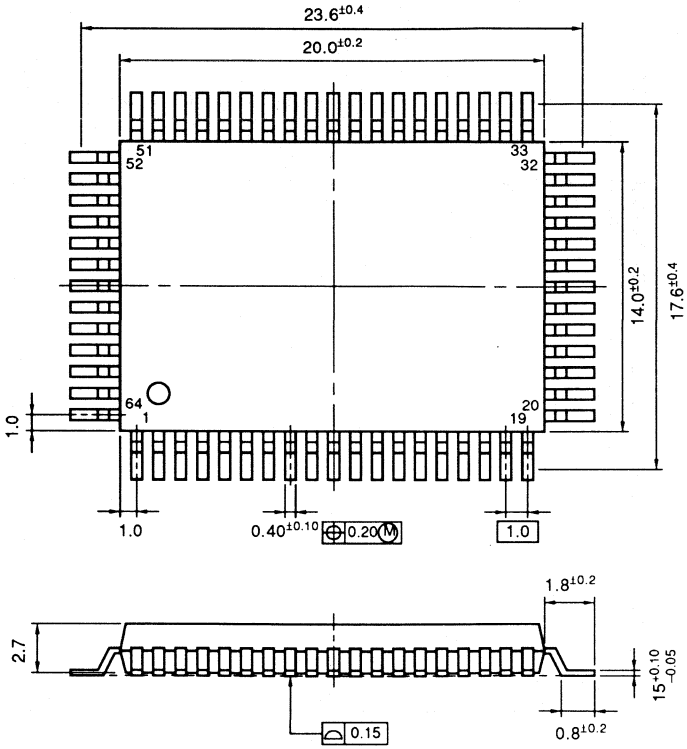
P64EW–100–A

64-Pin QUIP Plastic (Units: mm)

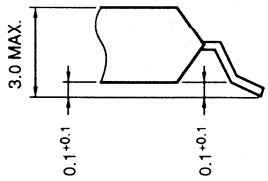


P64GQ–100–36

64-Pin Plastic QFP (14 x 20) (Units: mm)

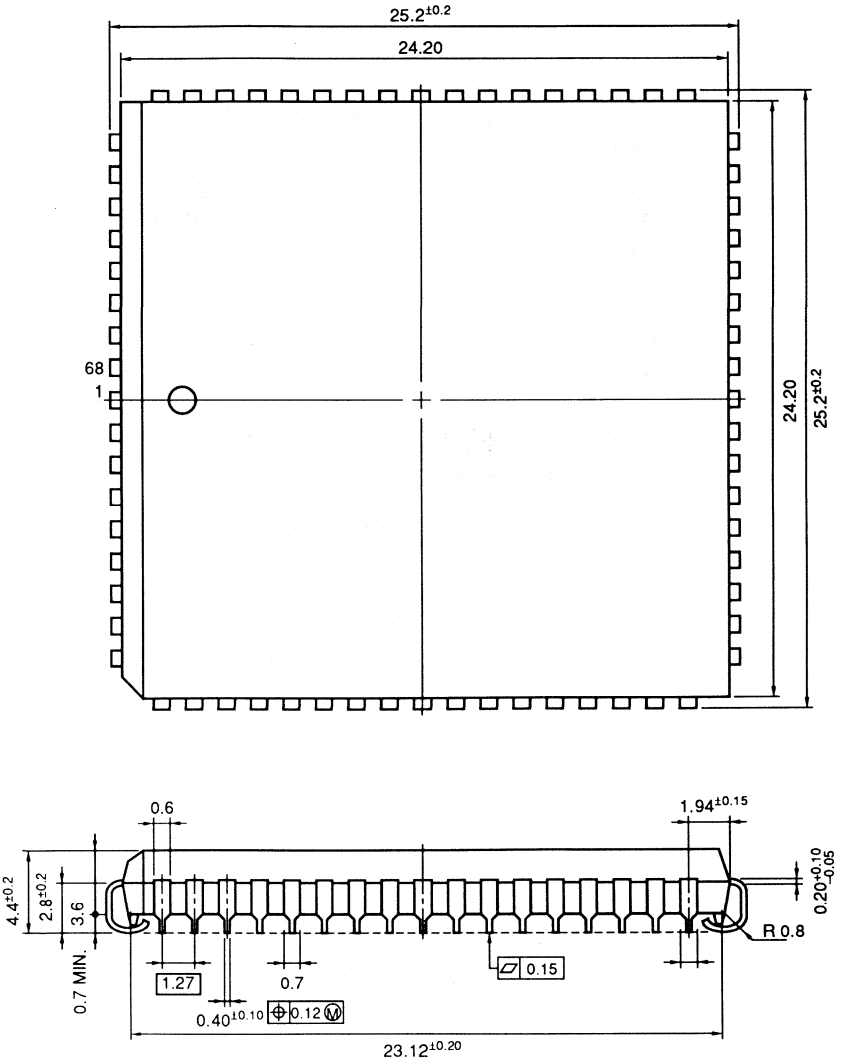


Detail of Pin Shape



P64GF-100-3B8, 3BE-1

68-Pin PLCC (□ 950) (Units: mm)



P68L–50A1

Description

The μPD78322/μPD78320 are single-chip microcomputers designed for process control. It features a 16-bit CPU, an 8-bit external bus, and a powerful set of on-chip peripherals including counters and timers, an A/D converter, two serial ports, and a maximum of 55 input/output lines. An advanced interrupt handling facility includes a three level program-controlled hardware priority interrupt controller and three separate methods of handling interrupt requests. It is manufactured of 1.2μ CMOS process, operates from a single 5 volt power supply, and has a maximum oscillator frequency of 16 MHz. The μPD78322 has 16K bytes of on-chip mask-programmed ROM, and the μPD78320 is a ROM-less version. Both chips have 640 bytes of on-chip RAM and are supplied in 68-pin PLCC and 74-pin QFP packages.

The μPD78322 includes an interface for a special dedicated memory chip, the μPD71P301. The μPD71P301 includes memory, interface circuitry, and an instruction pre-fetch pointer. This makes it possible to fetch instructions from external memory at the same high speed at which they can be fetched-from on-chip ROM.

The primary applications of the μPD78322 include automotive engine control, anti-lock braking control, and control of computer disks and tapes. Its speed and powerful on-chip peripherals, however, make it suitable for all of the more demanding types of process control.

Features

- Single-chip microcomputer:
  - 16-bit ALU.
  - 16K bytes of ROM (μPD78322).
- Powerful instruction set:
  - 16-bit unsigned multiply & divide.
  - 1-bit & 8-bit logic instructions.
  - String instructions.
- Minimum instruction time: 250 nsec. @ 16 MHz input.
- 3-byte instruction pre-fetch queue.
- Memory expansion:
  - 64K bytes address space.
  - High speed fetch from external memory.
- Large I/O capacity:
  - Up to 55 I/O port lines.
- Special interface for Turbo Access Manager (μPD71P301).
- Memory mapped on-chip peripherals (special function registers).
- Multi-purpose pulse input/output unit:
  - 16/18-bit free-running timer.
  - 16-bit timer/event counter.
  - Six 16-bit compare registers.
  - Four 18-bit capture registers.
  - Two 18-bit capture/compare registers.
  - Six external interrupt/capture lines.
  - One external event counter/interrupt line.
  - Six timer-controlled output lines
- 10-bit, 8-channel Analog to Digital Converter:
  - On-chip sample & hold amplifier.
- Two channel serial communication interface:
  - Asynchronous serial interface. (UART)
  - Serial Bus Interface.
  - Dedicated Baud rate generator.
- Programmable priority interrupt controller (3 levels).
- Threemethods of interrupt service:
  - Vectored interrupts.
  - Context switching:
    Includes hardware save of all general registers.
  - Macro Service:
    Choice of eight different functions.
- Watchdog Timer with dedicated output.
- Standby functions: STOP & HALT
- Single 5 V power supply.
- 68-pin PLCC package.
- 74-pin QFP

Ordering Information

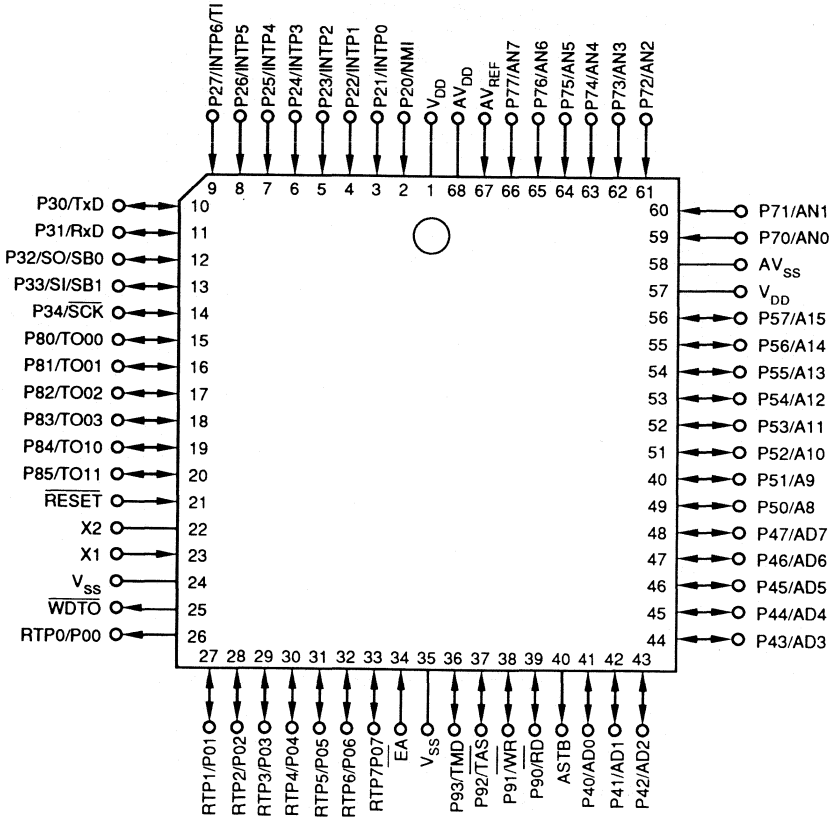
Part Number	Package Type	ROM
μPD78320L μPD78320GJ	68-Pin PLCC 74-Pin QFP	ROMless
μPD78322L-xxx μPD78322GJ-xxx	68-Pin PLCC 74-Pin QFP	16-K ROM
μPD78P322L μPD78P322GJ	68-Pin PLCC 74-Pin QFP	16-K OTPROM
μPD78P322KC μPD78P322KD	68-Pin LCC 74-Pin LCC ceramic with window	16-K UVPROM

Function Table

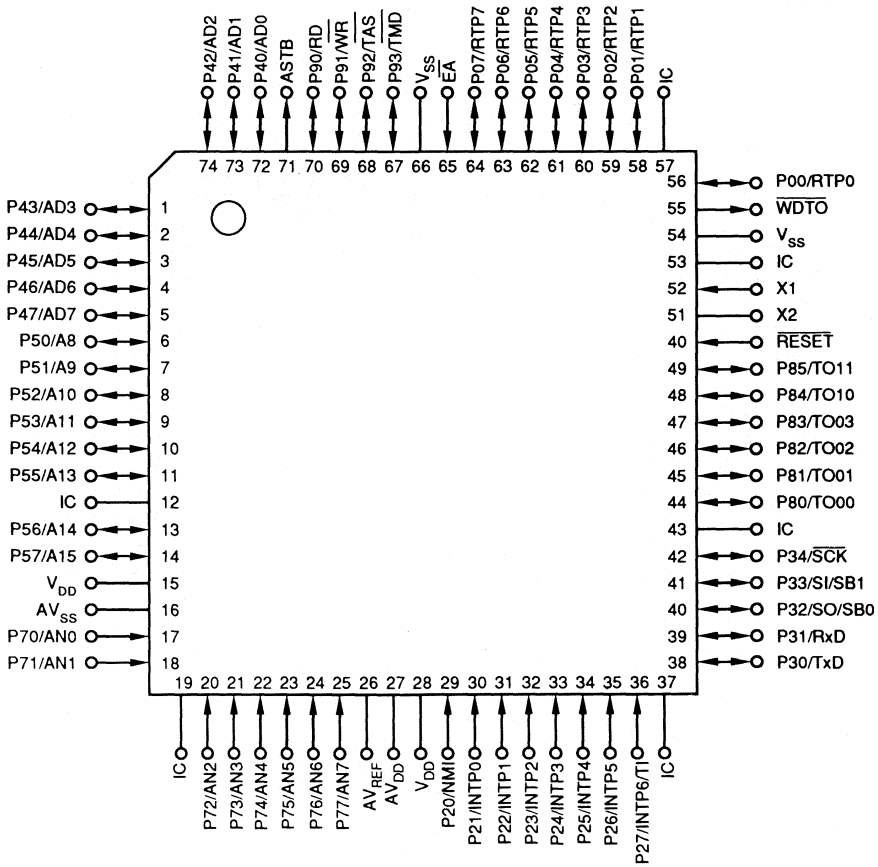
Function	Description
No. of basic instructions	109
Minimum instruction execution time	0.25 μs (external clock operating at 16 MHz)
On-chip memories	• ROM: 16384 x 8 bits (μPD78322 only) • RAM: 640 x 8 bits
Memory space	64K bytes
General-purpose register	8 bits x 16 x 8 banks (memory mapping)
I/O line	• Input ports : 16 • Input/output ports : 39 (μPD78322) 21 (μPD78320) • Analog inputs : 8
Realtime pulse unit	• 18/16-bit free running timer : 1 • 16-bit timer/event counter : 1 • 16-bit compare registers : 6 • 18-bit capture registers : 4 • 18-bit capture/compare registers : 2 • Realtime output ports : 8
Serial communication interface	Serial interface with a dedicated baud rate generator • UART : 1 channel • SBI (NEC serial bus interface : 1 channel
A/D converter	10-bit resolution (8 analog inputs)
Interrupt	• 21 sources (external: 8, internal: 13) • 3 processing modes (Vectored interrupt, context switching function and macro service function)
Standby	STOP mode/HALT mode
Instruction set	16-bit transfer/operation instructions, and multiply/divide instructions (16 x 16, 32 + 16), bit manipulation instruction, string instruction, etc.
Others	• On-chip watchdog timer • Directly connectable with turbo access manager μPD71P301
Package	68-pin PLCC (Plastic Leaded Chip Carrier) 74-pin plastic QFP

Pin Configuration

1. 68-pin PLCC



2. 74-Pin Plastic QFP (20 x 20 mm)

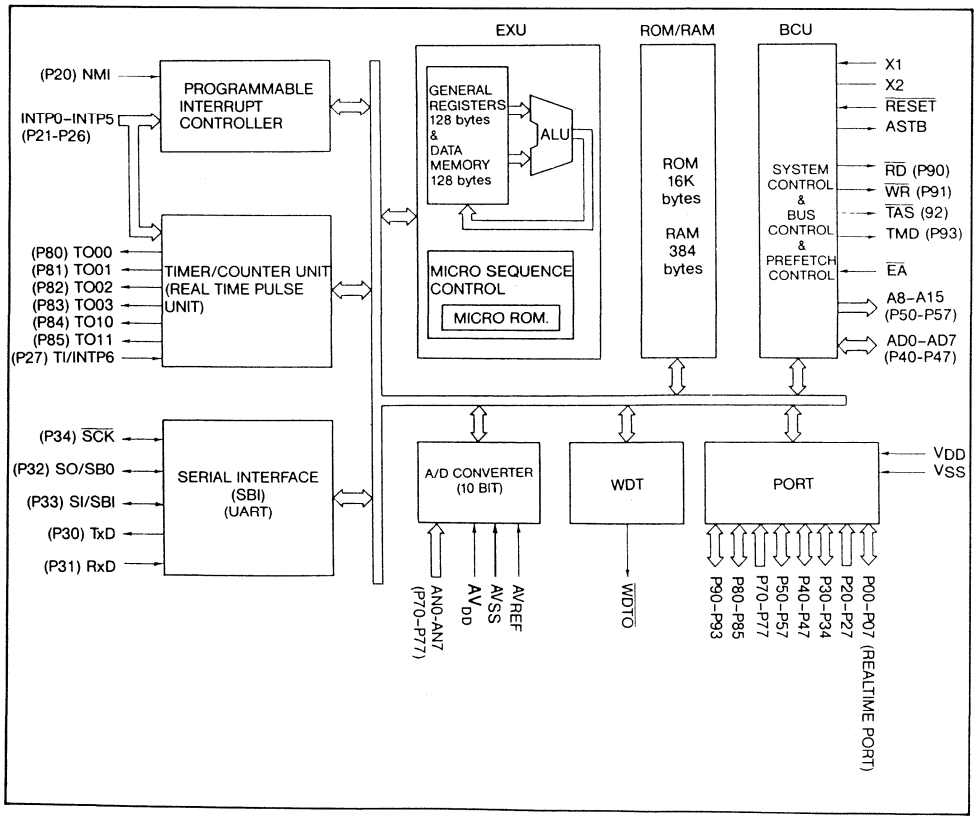


Pin Identification

P00 to P07	:	Port 0
P20 to P27	:	Port 2
P30 to P34	:	Port 3
P40 to P47	:	Port 4
P50 to P57	:	Port 5
P70 to P77	:	Port 7
P80 to P85	:	Port 8
P90 to P93	:	Port 9
NMI	:	Nonmaskable Interrupt
INTP0 to INTP6	:	Interrupt from Peripherals 0 to 6
RTP0 to RTP7	:	Real-time Port 0 to 7
TI	:	Timer Input
TxD	:	Transmit Data
RxD	:	Receive Data
SB0/SO	:	Serial Bus/Serial Output
SB1/SI	:	Serial Bus/Serial Input
$\overline{SCK}$	:	Serial Clock
TO00 to TO11	:	Timer Output 00 to 11
RESET	:	Reset
X1, X2	:	Crystal 1, 2
$\overline{WDTO}$	:	Watchdog Timer Output
$\overline{EA}$	:	External Access
TMD	:	Turbo Mode
$\overline{TAS}$	:	Turbo Access Strobe
$\overline{WR}$	:	Write
$\overline{RD}$	:	Read
ASTB	:	Address Strobe
AD0 to AD7	:	Address 0 to 7/Data 0 to 7
A8 to A15	:	Address 8 to 15
AN0 to AN7	:	Analog Input 0 to 7
AV_{REF}	:	Analog Reference Voltage
AV_{SS}	:	Analog V_{SS}
AV_{DD}	:	Analog V_{DD}

2

Block Diagram



Pin Functions

Ports

Pin Name	Input/ Output	Dual Function Pin	Function
P00 to P07	Input/ Output	RTP0 to RTP7	Port 0 8-bit input/output port Input/output specifiable for each bit Also serves as a realtime output port.
P20	Input	NMI	Port 2
P21		INTP0	Dedicated 8-bit input port
P22		INTP1	
P23		INTP2	
P24		INTP3	
P25		INTP4	
P26		INTP5	
P27		INTP6/TI	
P30	Input/ Output	TxD	Port 3
P31		RxD	5-bit input/output port
P32		SO/SB0	Input/output specifiable for each bit
P33		SI/SB1	
P34		$\overline{SCK}$	
P40 to P47	Input/ Output	AD0 to AD7	Port 4 8-bit input/output port Input/output specifiable for 8-bit unit
P50 to P57	Input/ Output	A8 to A15	Port 5 8-bit input/output port Input/output specifiable for each bit
P70 to P77	Input	AN0 to AN7	Port 7 Dedicated 8-bit input port
P80	Input/ Output	TO00	Port 8
P81		TO01	6-bit input/output port
P82		TO02	Input/output specifiable for each bit
P83		TO03	
P84		TO10	
P85		TO11	
P90	Input/ Output	$\overline{RD}$	Port 9
P91		$\overline{WR}$	4-bit input/output port
P92		$\overline{TAS}$	Input/output specifiable for each bit
P93		TMD	

Other than Ports

Pin Name	Input/ Output	Dual Function Pin	Function
RTP0 to RTP7	Output	P00 to P07	Realtime output port which generates pulses in synchronization with the trigger signal transmitted from the realtime pulse unit (RPU).
NMI	Input	P20	Nonmaskable interrupt request input which can specify an effective edge at the rising or falling edge using mode register.
INTP0	Input	P21	External interrupt request input which can specify an effective edge using mode register
INTP1		P22	
INTP2		P23	
INTP3		P24	
INTP4		P25	
INTP5		P26	
INTP6		P27/TI	
TI	Input	P27/INTP6	External count clock input to timer 1 (TM1)
RxD	Input	P30	Serial data input to the asynchronous serial interface (UART)
TxD	Output	P31	Serial data output from the asynchronous serial interface (UART)
SO	Output	P32/SB0	Serial data output from the clock synchronous serial interface in the 3-wire mode
SI	Input	P33/SB1	Serial data input to the clock synchronous serial interface in the 3-wire mode
SB0	Input/ Output	P32/SO	Serial data input/output to/from the clock synchronous serial interface in the SBI mode
SB1		P33/SI	
$\overline{SCK}$	Input/ Output	P34	Serial clock input/output to/from the clock synchronous serial interface
AD0 to AD7	Input Output	P40 to P47	Multiplexed address/data bus for external memory expansion
A8 to A15	Output	P50 to P57	Address bus for external memory expansion
TO00	Output	P80	Pulse output from the realtime pulse unit
TO01		P81	
TO02		P82	
TO03		P83	
TO10		P84	
TO11		P85	
$\overline{RD}$	Output	P90	Strobe signal output for external memory read operations
$\overline{WR}$		P91	Strobe signal output for external memory write operations
$\overline{TAS}$		P92	Control signal output for accessing the turbo access manager μPD71P301
TMD		P93	
$\overline{WDTO}$	Output	—	Signal output for indicating that the watchdog timer has generated a nonmaskable interrupt

(to be continued)

(cont'd)

Pin Name	Input/ Output	Dual Function Pin	Function
ASTB	Output	—	Timing signal output for externally latching the address information output to port 4 for external memory access
$\overline{EA}$	Input	—	Normally $\overline{EA}$ pin is connected to V_{DD} for the μPD78322. When $\overline{EA}$ pin is connected to V_{SS}, the ROM-less mode is set and the external memory is accessed. Fix $\overline{EA}$ pin to "0" (low-level) for the μPD78320. The EA pin level cannot be changed during operation.
AN0 to AN7	Input	—	Analog input to the A/D converter
AV_{REF}	Input	—	A/D converter reference voltage input
AV_{DD}	—	—	A/D converter analog power supply
AV_{SS}	—	—	A/D converter GND
$\overline{RESET}$	—	—	System reset input
X1	Input	—	System clock oscillation crystal input pin. Input is applied to the X1 pin when clocks are supplied externally.
X2	—	—	
V_{DD}	—	—	Positive power supply pin
V_{SS}	—	—	GND pin

I/O Circuits

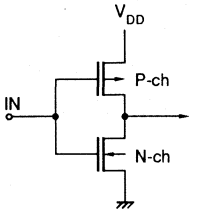
The type of I/O circuits of each pin are given in following table. The different types of I/O circuits are shown afterwards.

Input/Output Circuit types of each pin

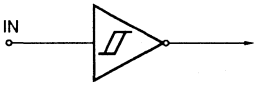
Pin	Input/Output Circuit Types
P00 to P07	5
P20/NMI	2
P21 to P26/INTP0 to INTP5	
P27/INTP6/TI	
P30/TxD	5
P31/RxD	
P32/SO/SB0	8
P33/SI/SB1	
P34/$\overline{SCK}$	
P40 to P47/AD0 to AD7	5
P50 to P57/A8 to A15	
P70 to P77/AN0 to AN7	9
P80 to P83/TO00 to TO03	5
P84 to P85/TO10 to TO11	
P90/$\overline{RD}$	
P91/$\overline{WR}$	
P92/$\overline{TAS}$	
P93/TMD	
$\overline{WDTO}$	3
$\overline{ASTB}$	4
$\overline{EA}$	1
$\overline{RESET}$	2

Pin I/O Circuits

Type 1

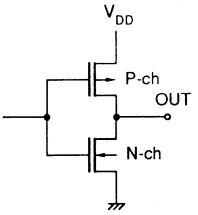


Type 2

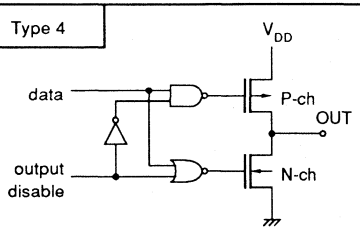


Schmitt-trigger input having hysteresis characteristics

Type 3



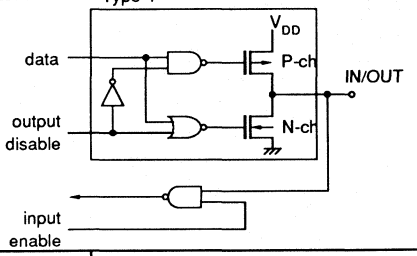
Type 4



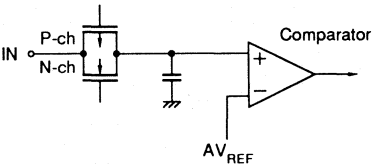
Push-pull output which can become output high-impedance (with both P-ch and N-ch set to off).

Type 5

Type 4



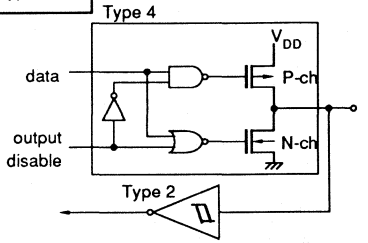
Type 7



(Threshold Voltage)

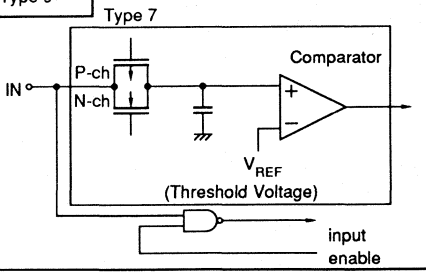
Type 8

Type 4



Type 9

Type 7



(Threshold Voltage)

Absolute Maximum Ratings
Ta = 25°C

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5 to +7.0	V
	AV_{DD}		-0.5 to V_{DD} +0.5	V
	AV_{SS}		-0.5 to +0.5	V
Input Voltage	V_I		-0.5 to V_{DD}+0.5	V
Output Voltage	V_O		-0.5 to V_{DD}+0.5	V
Output Current Low	I_{OL}	at 1 Pin	4.0	mA
		All Output Pin Total	90	mA
Output Current High	I_{OH}	at 1 Pin	- 1.0	mA
		All Output Pin Total	-20	mA
Reference Voltage	AV_{REF}	f_{XX}≤16MHz	-0.5 to AV_{DD} ±0.3	V
Operating Temperature	t_{opt}		-10 to +70	°C
Storage Temperature	t_{stg}		-65 to +150	°C

Recommended Operating Conditions

OSC Frequency	Ta	V_{DD}
8 MHz < f_{XX} ≤ 16 MHz	-10 C to +70 C	+5.0V+10%

Capacitance (Ta=25°C,V_{DD}=V_{ss}=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f_C = 1MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins			20	pF
I/O Capacitance	C_{IO}	Returned to 0V			20	pF

2

DC Characteristics

Ta = -10°C to +70°C, V_{DD}=5.0V±10%, V_{SS}=0V

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL}			0		0.8	V
Input High Voltage	V_{IH1}	*1		2.2			V
	V_{IH2}	*2		$0.8V_{DD}$			
Output Low Voltage	V_{OL}	I_{OL}=2.0mA				0.45	V
Output High Voltage	V_{OH}	I_{OH}=-400μA		V_{DD}-1.0			V
Input Leakage Current	I_{LI}	$0V \le V_I \le V_{DD}$				±10	μA
Output Leakage Current	I_{LO}	$0V \le V_O \le V_{DD}$				±10	μA
V_{DD} supply current	I_{DD1}	Operation Mode			40	65	mA
	I_{DD2}	Halt Mode			20	35	mA
Data Retention Voltage	V_{DDDR}	STOP Mode		2.5			V
Data Retention Current	I_{DDDR}	STOP Mode	V_{DDDR}=2.5V		2	10	μA
			V_{DDR}=5.0±10%		10	50	μA

Notes:

*1. All except $\overline{\text{RESET}}$, X1, X2, P20/NMI, P21/INTE0, P22/INTE1,P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{\text{SCK}}$

*2. $\overline{\text{RESET}}$, X1, X2, P20/NMI, P21/INTE0, P22/INTE1, P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{\text{SCK}}$

AC Characteristics

Read/Write Operation Ta = -10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Normal memory read/write operation (with general-purpose memory /turbo access manager connected).

Parameter	Symbol	Test Conditions	Min.	Max.	Units
System Clock Cycle Time	t_{CYK}		125	250	ns
Address Setup Time to ASTB↓	t_{SAST}		32		ns
Address Hold from ASTB↓	t_{HSTA}		32		ns
Address to $\overline{RD}$↓ Delay Time	t_{DAR}		85		ns
Address Float Time from $\overline{RD}$↓	t_{FRA}			0	ns
Address to Data Input	t_{DAID}			222	ns
$\overline{RD}$↓ to Data Input	t_{DRID1}			112	ns
ASTB↓ to $\overline{RD}$↓ Delay Time	t_{DSTR}		42		ns
Data Hold Time from $\overline{RD}$↑	t_{HRID}		0		ns
$\overline{RD}$↑ to Adress Delay Time	t_{DRA}		37		ns
$\overline{RD}$ Width Low	t_{WRL}		157		ns
ASTB Width High	t_{WSTH}		37		ns
Adress to $\overline{WR}$↓ Delay Time	t_{DAW}		85		ns
ASTB↓ to Data Output	t_{DSTOD}			102	ns
$\overline{WR}$↓ to Data Output	t_{DWOD}			40	ns
ASTB↓ to $\overline{WR}$↓ Delay Time	t_{DSTW}		42		ns
Data Setup to $\overline{WR}$↑	t_{SODW}		147		ns
Data Hold Time from $\overline{WR}$↑	t_{HWOD}		32		ns
$\overline{WR}$↑ to ASTB↑ Delay Time	t_{DWST}		42		ns
$\overline{WR}$ Width Low	t_{WWL}		157		ns

Branch Operation

Continuous instruction code fetch operation (with general-purpose memory/turbo access manager connected).

Parameter	Symbol	Test Conditions	Min.	Max.	Units
$\overline{TAS}$ Width Low	t_{WTAL}		37		ns
$\overline{TAS}$ Width High	t_{WTAH}		42		ns
$\overline{TAS}$ ↑ to Data Input	t_{DTAID}			55	ns
TMD ↑ to $\overline{TAS}$ ↑	t_{DTMRTA}		157		ns
RD ↓ to Data Input	t_{DRID2}			65	ns
$\overline{TAS}$ Setup to ASTB ↓	t_{STAST}		32		ns
TMD Setup to ASTB ↓	t_{STMST}		42		ns
TMD ↓ to $\overline{TAS}$ ↑	t_{DTMFTA}		95		ns
ASTB ↓ to TMD ↓ Delay Time	t_{DSTTM}		85		ns
Data Hold Time from $\overline{TAS}$ ↑	t_{HTMID}		0		ns

Serial Operation

Ta = -10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions		Min.	Max.	Units
$\overline{SCK}$ Cycle Time	t_{CYSK}	$\overline{SCK}$ Output	Note	1		μs
		$\overline{SCK}$ Input	External clock	1		μs
$\overline{SCK}$ Width Low	t_{WSKL}	$\overline{SCK}$ Output	Note	420		ns
		$\overline{SCK}$ Input	External clock	420		ns
$\overline{SCK}$ Width High	t_{WSKH}	$\overline{SCK}$ Output	Note	420		ns
		$\overline{SCK}$ Input	External clock	420		ns
SI Setup Time to $\overline{SCK}$ ↑	t_{SRXSK}			80		ns
SI Hold Time to $\overline{SCK}$ ↑	t_{HSKRX}			80		ns
SO Delay Time from $\overline{SCK}$ ↓	t_{DSKTX}				210	ns

Note: Internally divided by 8

A/D Converter Characteristics

Ta = -10°C to +70°C, V_{SS}=AV_{SS}=0V, 3.4V≤AV_{REF}≤AV_{DD}, V_{DD}=+5V±10%, V_{DD} - 0.5V ≤ AV_{DD} ≤ V_{DD}

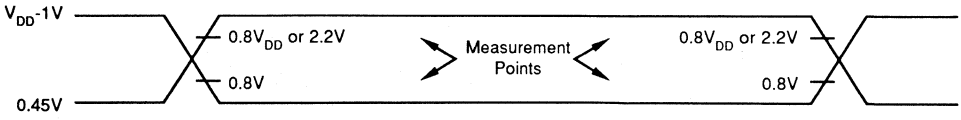
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Resolution			10			Bits
Relative Accuracy					±0.2%	FSR
Quatization Error					±1/2	LSB
Conversion Time	t_{CONV}		144			t_{CYK}
Sampling Time	t_{SAMP}		24			t_{CYK}
Zero Offset Error				±1.5		LSB
Gain Error				±1.5		LSB
Linearity Error				±1.5		LSB
Analog Input Voltage	V_{IAN}		0		VA_{REF}	V
VA_{REF} Current	AI_{REF}			1.0	3.0	mA
AV_{DD} supply Current	AI_{DD}			2.0	6.0	mA

Bus Timing Depending on Tcyk

Symbol	Calculation Expression	Min./Max.	Unit
t_{SAST}	0.5 T - 30	Min.	ns
t_{HSTA}	0.5 T - 30	Min.	ns
t_{DAR}	T - 40	Min.	ns
t_{DAID}	(2.5 + n) T - 90	Max.	ns
t_{DRID1}	(1.5 + n) T - 75	Max.	ns
t_{DSTR}	0.5 T - 20	Min.	ns
t_{DRA}	0.5 T - 25	Min.	ns
t_{WRL}	(1.5 + n) T - 30	Min.	ns
t_{WSTH}	0.5 T - 25	Min.	ns
t_{DAW}	T - 40	Min.	ns
t_{DSTOD}	0.5 T + 40	Max.	ns
t_{DSTW}	0.5 T - 20	Min.	ns
t_{SODW}	1.5 T - 40	Min.	ns
t_{HWOD}	0.5 T - 30	Min.	ns
t_{DWAST}	0.5 T - 20	Min.	ns
t_{WWL}	(1.5 + n) T - 30	Min.	ns
t_{WTAL}	0.5 T - 25	Min.	ns
t_{WTAH}	0.5 T - 20	Min.	ns
t_{DTAID}	T - 45	Min.	ns
t_{DTMRTA}	1.5 T - 30	Min.	ns
t_{DRID2}	T - 60	Max.	ns
t_{STAST}	0.5 T - 30	Min.	ns
t_{STMST}	0.5 T - 20	Min.	ns
t_{DTMFTA}	T - 30	Min.	ns
t_{DSTTM}	T - 40	Min.	ns

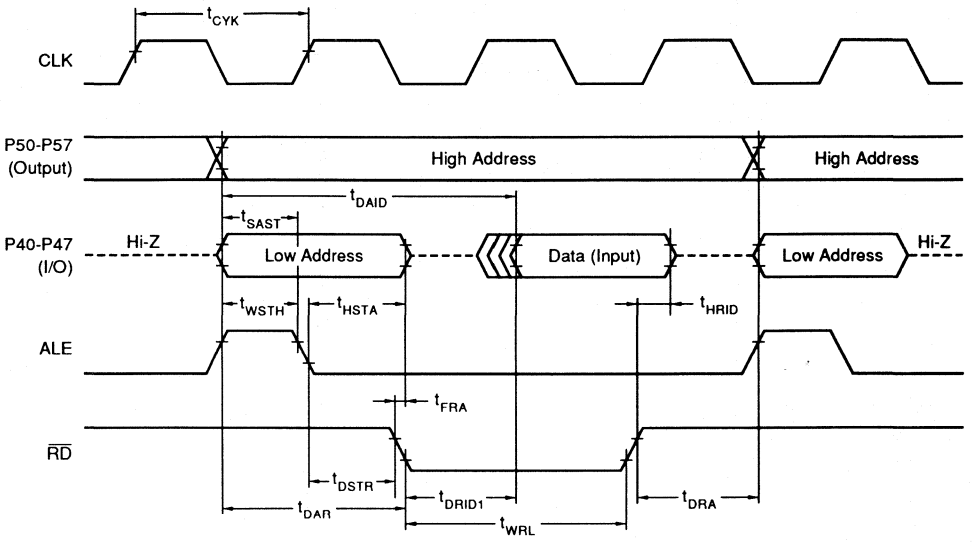
Note: $t = T_{CYK} = 1/f_{CLK}$ (f_{CLK}: Internal System Clock)
n = number of wait cycles defined by user software
The parameters not included in the above list are not dependent on t_{CYK}.

AC Timing Measurement Points

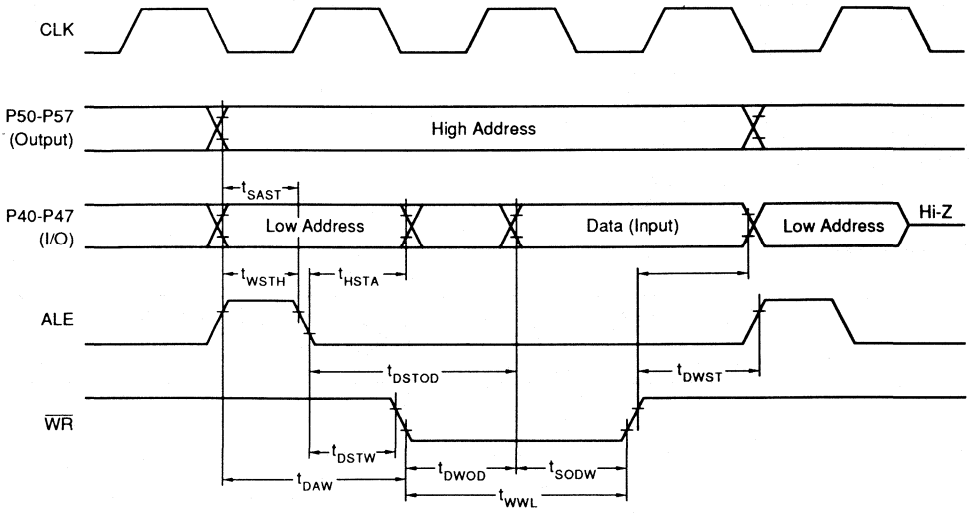


Timing Diagrams

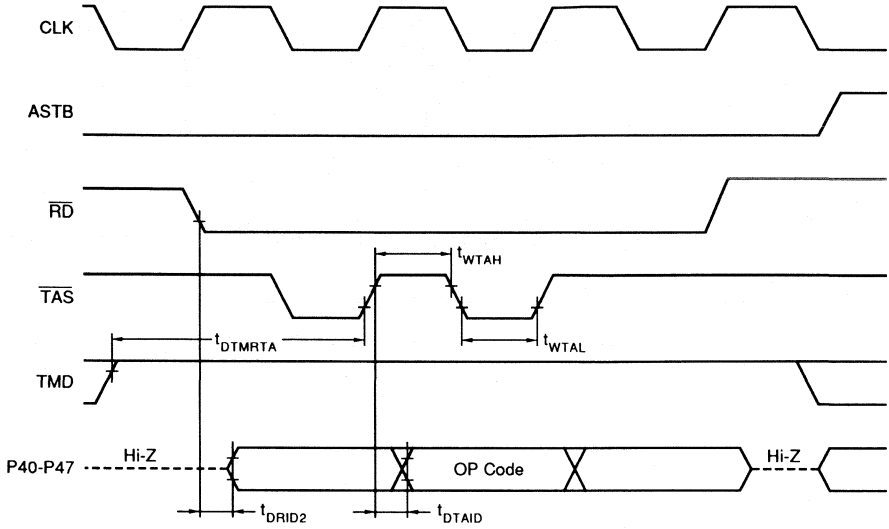
Read Operation



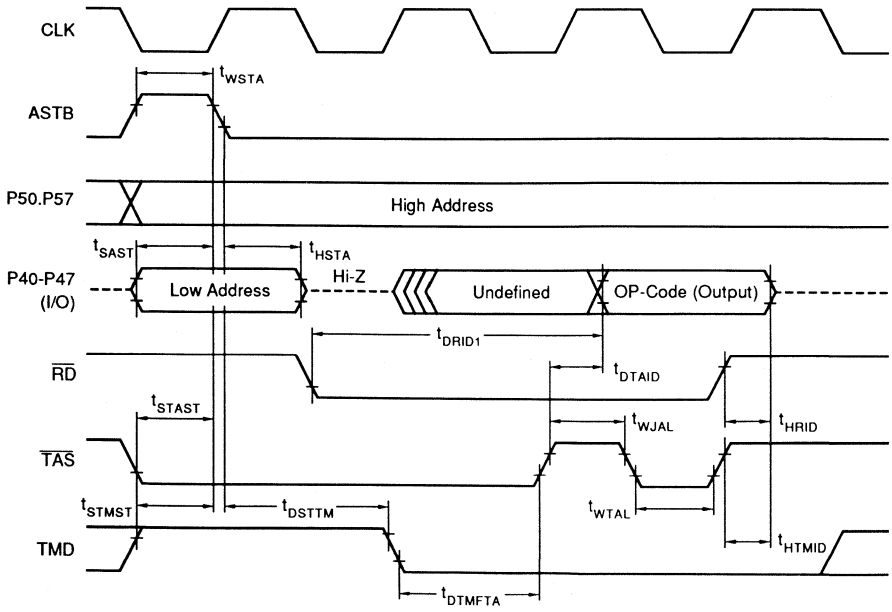
Write Operation



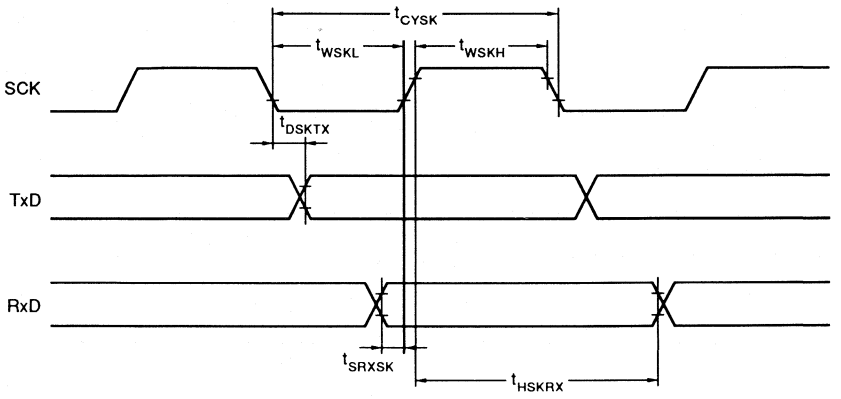
Turbo Fetch Operation



Branch Operation



Serial Operation



Extended Temperature Range

Absolute Maximum Ratings
Ta = 25°C

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5 to +7.0	V
	AV_{DD}		-0.5 to V_{DD} +0.5	V
	AV_{SS}		-0.5 to +0.5	V
Input Voltage	V_I		-0.5 to V_{DD}+0.5	V
Output Voltage	V_O		-0.5 to V_{DD}+0.5	V
Output Current Low	I_{OL}	at 1 Pin	4.0	mA
		All Output Pin Total	90	mA
Output Current High	I_{OH}	at 1 Pin	- 1.0	mA
		All Output Pin Total	-20	mA
Reference Voltage	AV_{REF}	f_{XX}≤16MHz	-0.5 to AV_{DD} ±0.3	V
Operating Temperature	t_{opt}		-40 to +85	°C
Storage Temperature	t_{stg}		-65 to +150	°C

Recommended Operating Conditions

OSC Frequency	Ta	V_{DD}
8 MHz < f_{XX} ≤ 16 MHz	-40 C to +85 C	+5.0V±10%

Capacitance (Ta=25°C,V_{DD}=V_{ss}=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f_C = 1MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins			20	pF
I/O Capacitance	C_{IO}	Returned to 0V			20	pF

DC Characteristics

Ta = -40°C to +85°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL}			0		0.8	V
Input High Voltage	V_{IH1}	*1		2.2			V
	V_{IH2}	*2		$0.8V_{DD}$			
Output Low Voltage	V_{OL}	I_{OL}=2.0mA				0.45	V
Output High Voltage	V_{OH}	I_{OH}=-400μA		V_{DD}-1.0			V
Input Leakage Current	I_{LI}	0V≤V_I≤V_{DD}				±10	μA
Output Leakage Current	I_{LO}	0V≤V_O≤V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operation Mode			40	65	mA
	I_{DD2}	Halt Mode			25	40	mA
Data Retention Voltage	V_{DDDR}	STOP Mode		2.5			V
Data Retention Current	I_{DDDR}	STOP Mode	V_{DDDR}=2.5V		4	100	μA
			V_{DDR}=5.0±10%		20	300	μA

Notes:

*1. All except $\overline{\text{RESET}}$, X1, X2, P20/NMI, P21/INTE0, P22/INTE1,P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{\text{SCK}}$

*2. $\overline{\text{RESET}}$, X!, X2, P20/NMI, P21/INTE0, P22/INTE1, P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{\text{SCK}}$

AC Characteristics

Read/Write Operation Ta = -40°C to +85°C, V_{DD}=5.0V±10%, V_{ss}=0V

Normal memory read/write operation (with general-purpose memory /turbo access manager connected).

Parameter	Symbol	Test Conditions	Min.	Max.	Units
System Clock Cycle Time	t_{CYK}		125	250	ns
Address Setup Time to ASTB↓	t_{SAST}		32		ns
Address Hold from ASTB↓	t_{HSTA}		32		ns
Address to $\overline{RD}$↓ Delay Time	t_{DAR}		85		ns
Address Float Time from $\overline{RD}$↓	t_{FRA}			0	ns
Address to Data Input	t_{DAID}			222	ns
$\overline{RD}$↓ to Data Input	t_{DRID1}			112	ns
ASTB↓ to $\overline{RD}$↓ Delay Time	t_{DSTR}		42		ns
Data Hold Time from $\overline{RD}$↑	t_{HRID}		0		ns
$\overline{RD}$↑ to Adress Delay Time	t_{DRA}		37		ns
$\overline{RD}$ Width Low	t_{WRL}		157		ns
ASTB Width High	t_{WSTH}		37		ns
Adress to $\overline{WR}$↓ Delay Time	t_{DAW}		85		ns
ASTB↓ to Data Output	t_{DSTOD}			102	ns
$\overline{WR}$↓ to Data Output	t_{DWOD}			40	ns
ASTB↓ to $\overline{WR}$↓ Delay Time	t_{DSTW}		42		ns
Data Setup to $\overline{WR}$↑	t_{SODW}		147		ns
Data Hold Time from $\overline{WR}$↑	t_{HWOD}		32		ns
$\overline{WR}$↑ to ASTB↑ Delay Time	t_{DWST}		42		ns
$\overline{WR}$ Width Low	t_{WWL}		157		ns

Branch Operation

Continuous instruction code fetch operation (with general-purpose memory/turbo access manager connected).

Parameter	Symbol	Test Conditions	Min.	Max.	Units
$\overline{TAS}$ Width Low	t_{WTAL}		37		ns
$\overline{TAS}$ Width High	t_{WTAH}		42		ns
$\overline{TAS}$ to Data Input	t_{DTAID}			55	ns
TMD to $\overline{TAS}$	t_{DTMRTA}		157		ns
RD to Data Input	t_{DRID2}			58	ns
$\overline{TAS}$ Setup to ASTB	t_{STAST}		32		ns
TMD Setup to ASTB	t_{STMST}		32		ns
TMD to $\overline{TAS}$	t_{DTMFTA}		92		ns
ASTB to TMD Delay Time	t_{DSTTM}		85		ns
Data Hold Time from $\overline{TAS}$	t_{HTMID}		0		ns

Serial Operation

Ta = -40°C to +85°C, V_{DD}=5.0V±10%, V_{SS}=0V

Parameter	Symbol	Test Conditions		Min.	Max.	Units
$\overline{SCK}$ Cycle Time	t_{CYSK}	$\overline{SCK}$ Output	Note	1		μs
		$\overline{SCK}$ Input	External clock	1		μs
$\overline{SCK}$ Width Low	t_{WSKL}	$\overline{SCK}$ Output	Note	420		ns
		$\overline{SCK}$ Input	External clock	420		ns
$\overline{SCK}$ Width High	t_{WSKH}	$\overline{SCK}$ Output	Note	420		ns
		$\overline{SCK}$ Input	External clock	420		ns
SI Setup Time to $\overline{SCK}$ ↑	t_{SRXSK}			80		ns
SI Hold Time to $\overline{SCK}$ ↑	t_{HSKRX}			80		ns
SO Delay Time from $\overline{SCK}$ ↓	t_{DSKTX}				210	ns

Note: Internally divided by 8

A/D Converter Characteristics

Ta = -40°C to +85°C, V_{SS}=AV_{SS}=0V, 3.4V≤AV_{REF}≤AV_{DD}, V_{DD}=+5V±10%, V_{DD} - 0.5V ≤ AV_{DD} ≤ V_{DD}

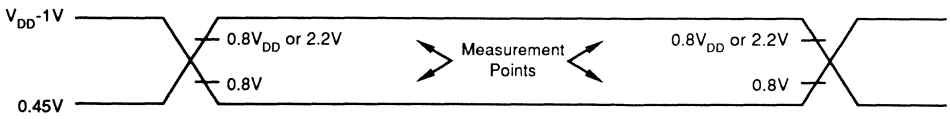
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Resolution			10			Bits
Absolute Accuracy					±0.2%	FSR
Quatization Error					±1/2	LSB
Conversion Time	t_{CONV}		144			t_{CYK}
Sampling Time	t_{SAMP}		24			t_{CYK}
Zero Offset Error				±1.5		LSB
Gain Error				±1.5		LSB
Linearity Error				±1.5		LSB
Analog Input Voltage	V_{IAN}		0		VA_{REF}	V
VA_{REF} Current	AI_{REF}			1.0	3.0	mA
AV_{DD} supply Current	AI_{DD}			2.0	6.0	mA

Bus Timing Depending on Tcyk

Symbol	Calculation Expression	Min./Max.	Unit
t_{SAST}	0.5 T - 30	Min.	ns
t_{HSTA}	0.5 T - 30	Min.	ns
t_{DAR}	T - 40	Min.	ns
t_{DAID}	(2.5 + n) T - 90	Max.	ns
t_{DRID1}	(1.5 + n) T - 75	Max.	ns
t_{DSTR}	0.5 T - 20	Min.	ns
t_{DRA}	0.5 T - 25	Min.	ns
t_{WRL}	(1.5 + n) T - 30	Min.	ns
t_{WSTH}	0.5 T - 25	Min.	ns
t_{DAW}	T - 40	Min.	ns
t_{DSTOD}	0.5 T + 40	Max.	ns
t_{DSTW}	0.5 T - 20	Min.	ns
t_{SODW}	1.5 T - 40	Min.	ns
t_{HWOD}	0.5 T - 30	Min.	ns
t_{DWAST}	0.5 T - 20	Min.	ns
t_{WWL}	(1.5 + n) T - 30	Min.	ns
t_{WTAL}	0.5 T - 25	Min.	ns
t_{WTAH}	0.5 T - 20	Min.	ns
t_{DTAID}	T - 48	Min.	ns
t_{DTMRTA}	1.5 T - 30	Min.	ns
t_{DRID2}	T - 66	Max.	ns
t_{STAST}	0.5 T - 30	Min.	ns
t_{STMST}	0.5 T - 30	Min.	ns
t_{DTMFTA}	T - 33	Min.	ns
t_{DSTTM}	T - 40	Min.	ns

Note: $t = T_{CYK} = 1/f_{CLK}$ (f_{CLK}: Internal System Clock)
n = number of wait cycles defined by user software
The parameters not included in the above list are not dependent on t_{CYK}.

AC Timing Measurement Points



Absolute Maximum Ratings
Ta = 25°C

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5 to +7.0	V
	AV_{DD}		-0.5 to V_{DD} +0.5	V
	AV_{SS}		-0.5 to +0.5	V
Input Voltage	V_I		-0.5 to V_{DD}+0.5	V
Output Voltage	V_O		-0.5 to V_{DD}+0.5	V
Output Current Low	I_{OL}	at 1 Pin	4.0	mA
		All Output Pin Total	90	mA
Output Current High	I_{OH}	at 1 Pin	- 1.0	mA
		All Output Pin Total	-20	mA
Reference Voltage	AV_{REF}	f_{XX}≤12MHz	-0.5 to AV_{DD} ±0.3	V
Operating Temperature	t_{opt}		-40 to +110	°C
Storage Temperature	t_{stg}		-65 to +150	°C

Recommended Operating Conditions

OSC Frequency	Ta	V_{DD}
8 MHz < f_{XX} ≤ 12 MHz	-40 C to +110°C	+5.0V±10%

Capacitance (Ta=25°C,V_{DD}=V_{ss}=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f_C = 1MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins			20	pF
I/O Capacitance	C_{IO}	Returned to 0V			20	pF

DC Characteristics

Ta = -40°C to +110°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL}			0		0.8	V
Input High Voltage	V_{IH1}	*1		2.0			V
	V_{IH2}	*2		$0.8V_{DD}$			
Output Low Voltage	V_{OL}	I_{OL}=2.0mA				0.45	V
Output High Voltage	V_{OH}	I_{OH}=-400μA		V_{DD}-1.0			V
Input Leakage Current	I_{LI}	$0V \le V_I \le V_{DD}$				±10	μA
Output Leakage Current	I_{LO}	$0V \le V_O \le V_{DD}$				±10	μA
V_{DD} supply current	I_{DD1}	Operation Mode			35	60	mA
	I_{DD2}	Halt Mode			25	40	mA
Data Retention Voltage	V_{DDDR}	STOP Mode		2.5			V
Data Retention Current	I_{DDDR}	STOP Mode	V_{DDDR}=2.5V		4	100	μA
			V_{DDR}=5.0±10%		10	300	μA

Notes:

*1. All except $\overline{RESET}$, X1, X2, P20/NMI, P21/INTE0, P22/INTE1,P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{SCK}$

*2. $\overline{RESET}$, X!, X2, P20/NMI, P21/INTE0, P22/INTE1, P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{SCK}$

AC Characteristics

Read/Write Operation Ta = -40°C to +110°C, V_{DD}=5.0V±10%, V_{ss}=0V

Normal memory read/write operation (with general-purpose memory /turbo access manager connected).

Parameter	Symbol	Test Conditions	Min.	Max.	Units
System Clock Cycle Time	t_{CYK}		166	250	ns
Address Setup Time to ASTB↓	t_{SAST}		43		ns
Address Hold from ASTB↓	t_{HSTA}		43		ns
Address to $\overline{RD}$↓ Delay Time	t_{DAR}		116		ns
Address Float Time from $\overline{RD}$↓	t_{FRA}			0	ns
Address to Data Input	t_{DAID}			315	ns
$\overline{RD}$↓ to Data Input	t_{DRID1}			164	ns
ASTB↓ to $\overline{RD}$↓ Delay Time	t_{DSTR}		53		ns
Data Hold Time from $\overline{RD}$↑	t_{HRID}		0		ns
$\overline{RD}$↑ to Adress Delay Time	t_{DRA}		48		ns
$\overline{RD}$ Width Low	t_{WRL}		209		ns
ASTB Width High	t_{WSTH}		48		ns
Adress to $\overline{WR}$↓ Delay Time	t_{DAW}		116		ns
ASTB↓ to Data Output	t_{DSTOD}			133	ns
$\overline{WR}$↓ to Data Output	t_{DWOD}			40	ns
ASTB↓ to $\overline{WR}$↓ Delay Time	t_{DSTW}		53		ns
Data Setup to $\overline{WR}$↑	t_{SODW}		209		ns
Data Hold Time from $\overline{WR}$↑	t_{HWOD}		43		ns
$\overline{WR}$↑ to ASTB↑ Delay Time	t_{DWST}		53		ns
$\overline{WR}$ Width Low	t_{WWL}		209		ns

Branch Operation

Continuous instruction code fetch operation (with general-purpose memory/turbo access manager connected).

Parameter	Symbol	Test Conditions	Min.	Max.	Units
$\overline{TAS}$ Width Low	t_{WTAL}		48		ns
$\overline{TAS}$ Width High	t_{WTAH}		53		ns
$\overline{TAS}$ to Data Input	t_{DTAID}			55	ns
TMD to $\overline{TAS}$	t_{DTMRTA}		209		ns
RD to Data Input	t_{DRID2}			55	ns
$\overline{TAS}$ Setup to ASTB	t_{STAST}		43		ns
TMD Setup to ASTB	t_{STMST}		43		ns
TMD to $\overline{TAS}$	t_{DTMFTA}		90		ns
ASTB to TMD Delay Time	t_{DSTTM}		116		ns
Data Hold Time from $\overline{TAS}$	t_{HTMID}		0		ns

Serial Operation

Ta = -40°C to +110°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions		Min.	Max.	Units
$\overline{SCK}$ Cycle Time	t_{CYSK}	$\overline{SCK}$ Output	Note	1.3		μs
		$\overline{SCK}$ Input	External clock	1.3		μs
$\overline{SCK}$ Width Low	t_{WSKL}	$\overline{SCK}$ Output	Note	580		ns
		$\overline{SCK}$ Input	External clock	580		ns
$\overline{SCK}$ Width High	t_{WSKH}	$\overline{SCK}$ Output	Note	580		ns
		$\overline{SCK}$ Input	External clock	580		ns
SI Setup Time to $\overline{SCK}$ ↑	t_{SRXSK}			80		ns
SI Hold Time to $\overline{SCK}$ ↑	t_{HSKRX}			80		ns
SO Delay Time from $\overline{SCK}$ ↓	t_{DSKTX}				210	ns

Note: Internally divided by 8

2

A/D Converter Characteristics

Ta = -10°C to +70°C, V_{SS}=AV_{SS}=0V, 3.4V≤AV_{REF}≤AV_{DD}, V_{DD}=+5V±10%, V_{DD} - 0.5V ≤ AV_{DD} ≤ V_{DD}

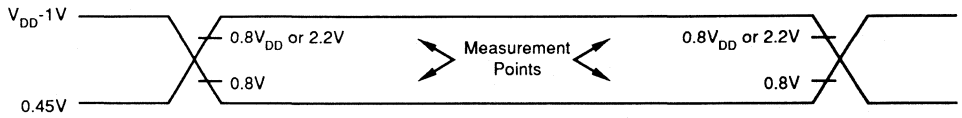
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Resolution			10			Bits
Absolute Accuracy		-40°C≤Ta≤85°C			±0.2%	FSR
		85°C≤Ta≤110°C			±0.4%	FSR
Quatization Error					±1/2	LSB
Conversion Time	t_{CONV}	t_{cyk}≥166ns	144			t_{CYK}
Sampling Time	t_{SAMP}	t_{cyk}≥166ns	24			t_{CYK}
Zero Offset Error				±1.5		LSB
Gain Error				±1.5		LSB
Linearity Error				±2.0		LSB
Analog Input Voltage	V_{IAN}		0		VA_{REF}	V
VA_{REF} Current	AI_{REF}			1.0	3.0	mA
AV_{DD} supply Current	AI_{DD}			2.0	6.0	mA

Bus Timing Depending on Tcyk

Symbol	Calculation Expression	Min./Max.	Unit
t_{SAST}	0.5 T - 40	Min.	ns
t_{HSTA}	0.5 T - 40	Min.	ns
t_{DAR}	T - 50	Min.	ns
t_{DAID}	(2.5 + n) T - 100	Max.	ns
t_{DRID1}	(1.5 + n) T - 85	Max.	ns
t_{DSTR}	0.5 T - 30	Min.	ns
t_{DRA}	0.5 T - 35	Min.	ns
t_{WRL}	(1.5 + n) T - 40	Min.	ns
t_{WSTH}	0.5 T - 35	Min.	ns
t_{DAW}	T - 50	Min.	ns
t_{DSTOD}	0.5 T + 50	Max.	ns
t_{DSTW}	0.5 T - 30	Min.	ns
t_{SODW}	1.5 T - 50	Min.	ns
t_{HWOD}	0.5 T - 40	Min.	ns
t_{DWAST}	0.5 T - 30	Min.	ns
t_{WWL}	(1.5 + n) T - 40	Min.	ns
t_{WTAL}	0.5 T - 35	Min.	ns
t_{WTAH}	0.5 T - 30	Min.	ns
t_{DTAID}	T - 50	Min.	ns
t_{DTMRTA}	1.5 T - 40	Min.	ns
t_{DRID2}	T - 70	Max.	ns
t_{STAST}	0.5 T - 40	Min.	ns
t_{STMST}	0.5 T - 40	Min.	ns
t_{DTMFTA}	T - 35	Min.	ns
t_{DSTTM}	T - 45	Min.	ns

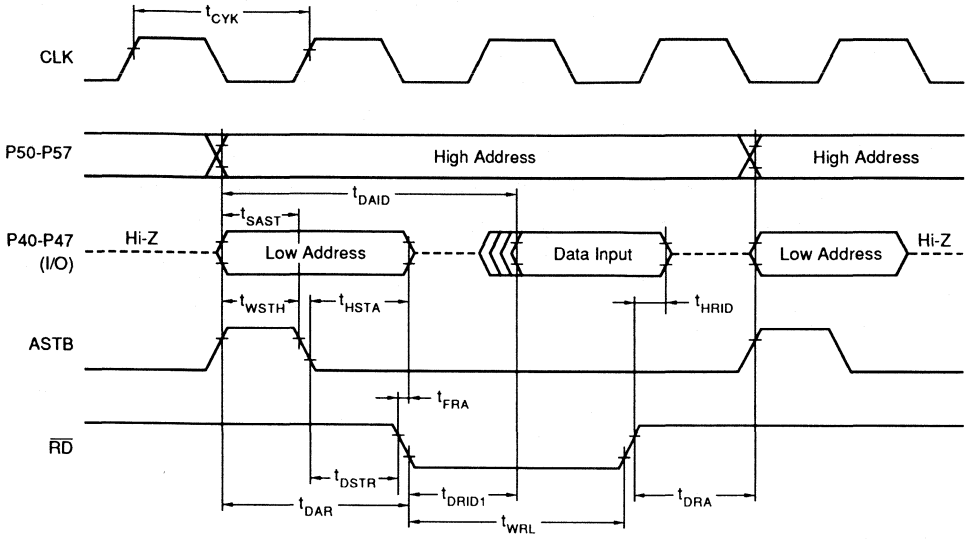
Note: t = T_{CYK} = $1/f_{CLK}$ (f_{CLK}: Internal System Clock)
n = number of wait cycles defined by user software
The parameters not included in the above list are not dependent on t_{CYK}.

AC Timing Measurement Points

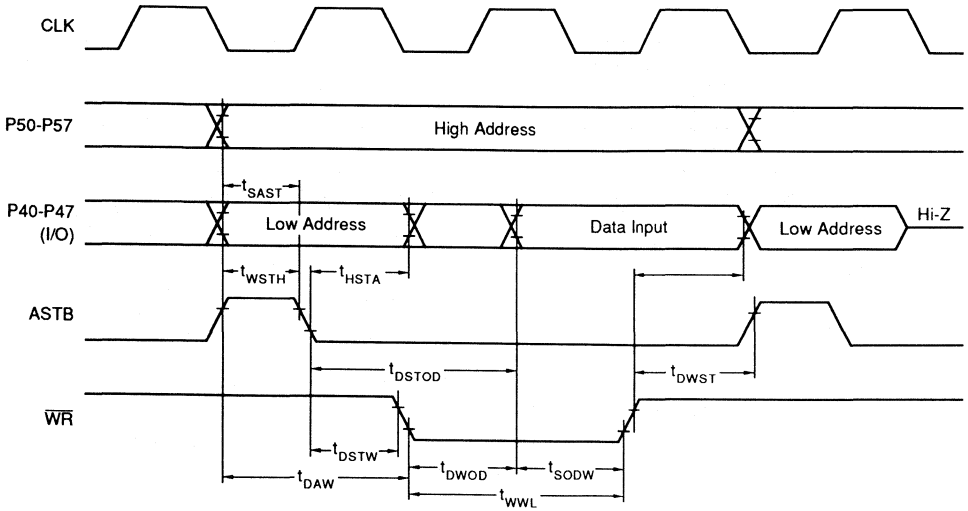


Timing Diagrams

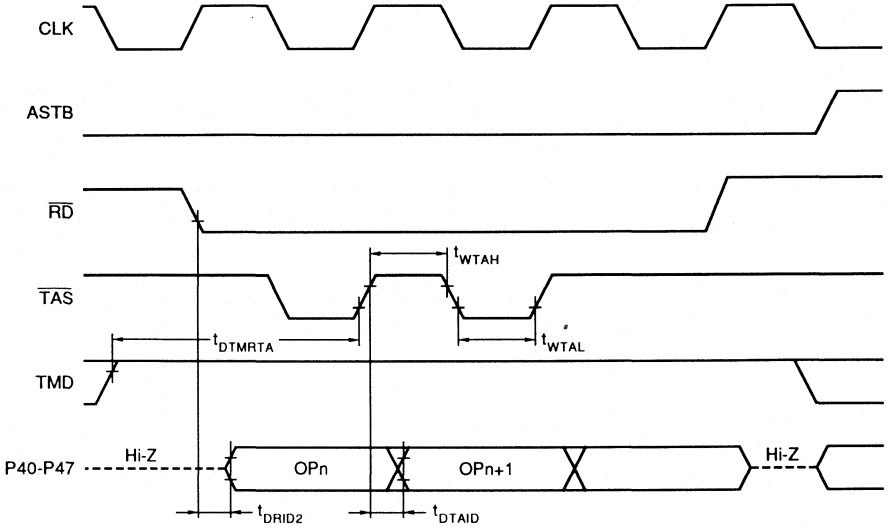
Read Operation



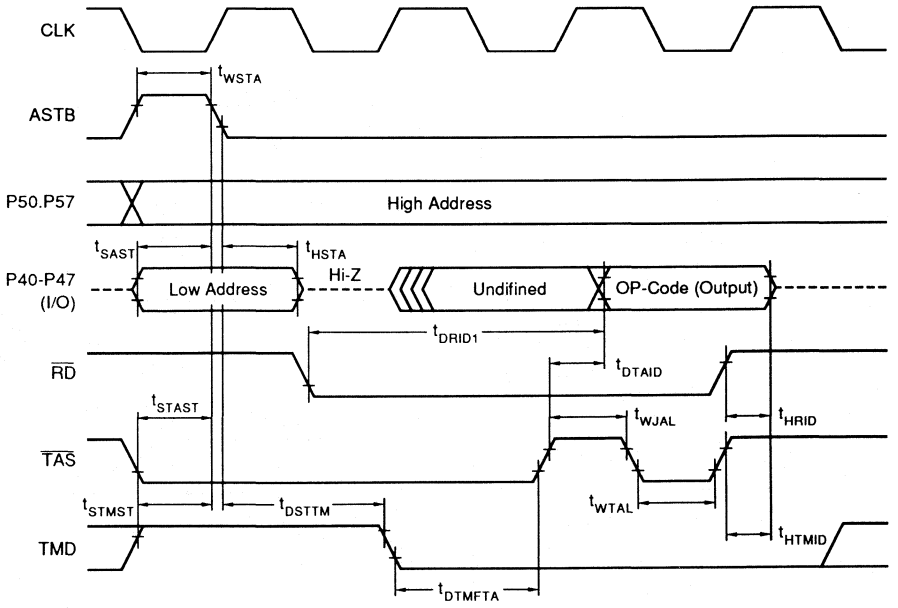
Write Operation



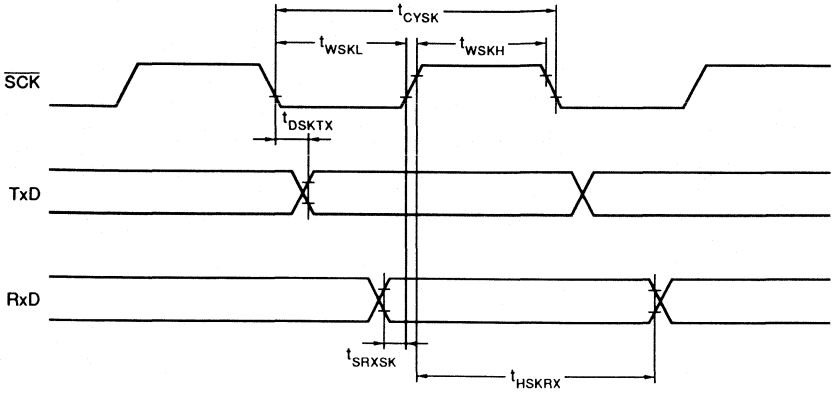
Turbo Fetch Operation



Branch Operation



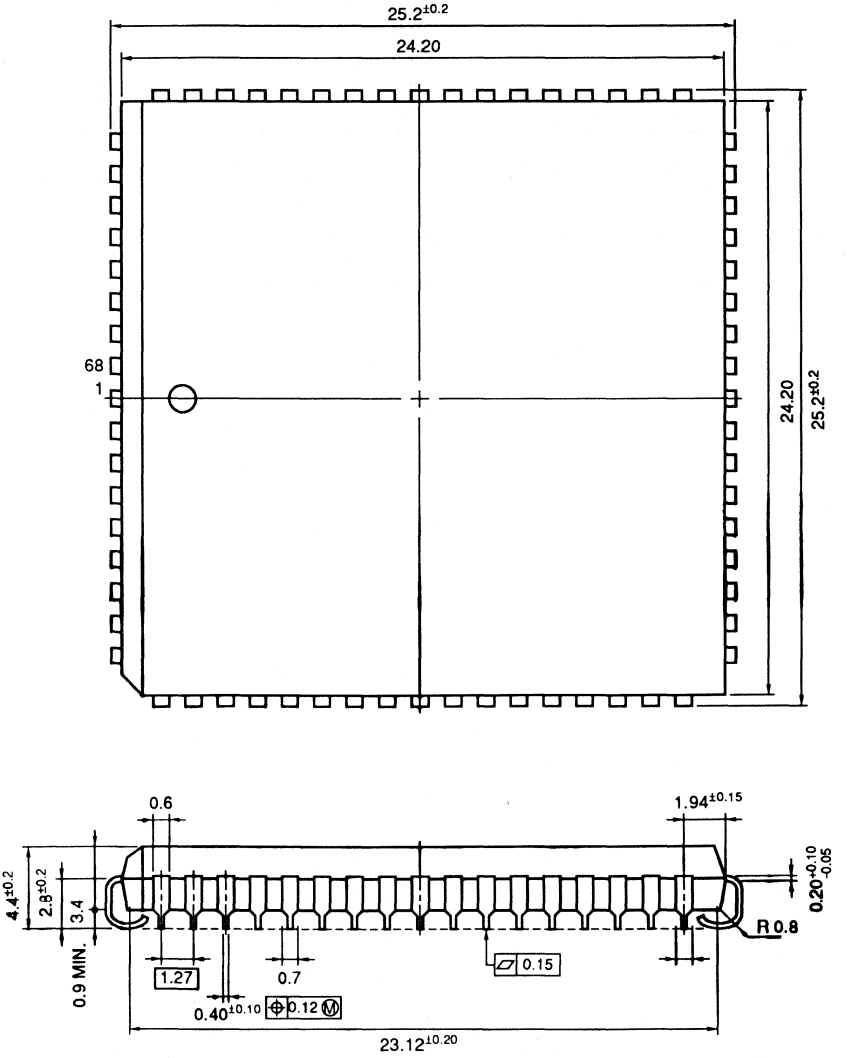
Serial Operation



2

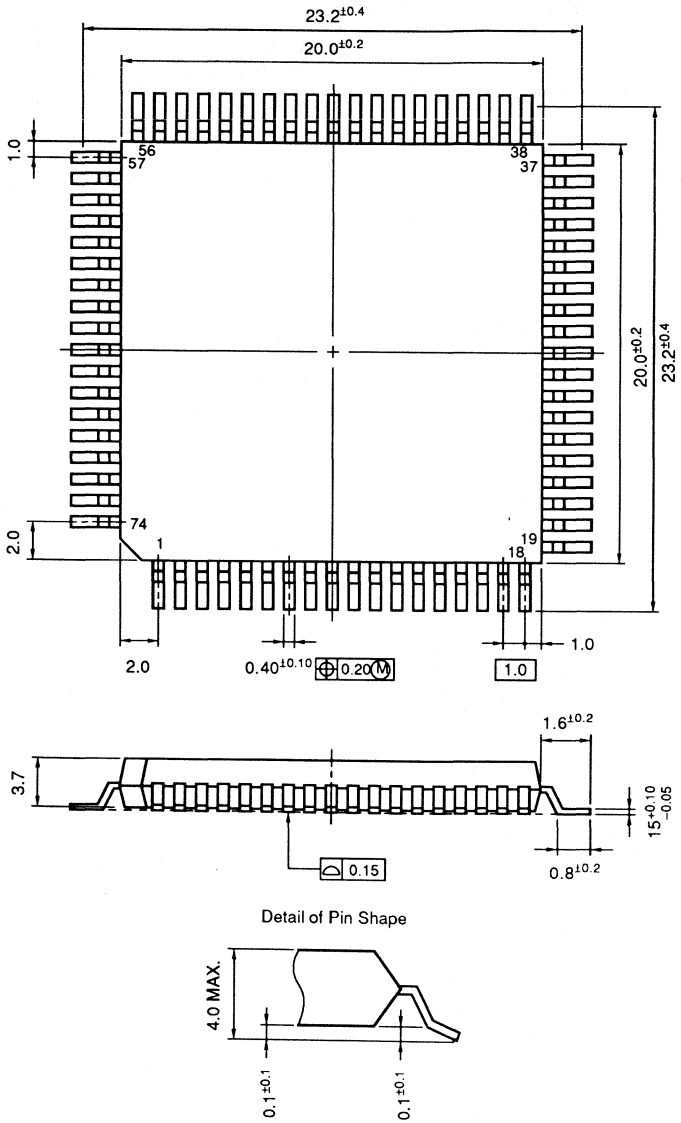
Package Dimensions (unit: mm)

68-Pin PLCC



P68L-50A1

74-Pin Plastic QFP



S74GJ-100-5BJ-1

Recommended Soldering Conditions

The table below shows the soldering conditions for this product based on the package.

Recommended Soldering Conditions

Product	Package	Recommended Condition
μPD78320GJ-3	74-pin plastic Quad Flat Pack [QFP]	Pin heated only
μPD78322GJ-xxx		
μPD78320L	68-pin PLCC	VP15-00 Pin heated only
μPD322L-xxx		

Soldering Conditions

Recommended Condition	Soldering	Soldering condition
VP15-00	VPS	Package peak temperature: 215°C; Time > 40sec (200°C <) one cycle
Heat applied to the pins only	Heat applied to the pins only	Pin temperature: > 300°C; Time: > 10sec

Description

The μPD78P322 is a product provided by replacing μPD78322 internal mask ROM with one-time PROM or EPROM. The one-time PROM product is programmable only once and is useful for short-run and multiple device production and early startup of set. The EPROM product is reprogrammable and appropriate for system evalution.
To read this doument, read also the μPD78322 documents.

Features

- μPD78320/322 compatible
- On-chip EPROM of 16k bytes:
  - μPD78322L/GJ: One-time progammable version.
  - μPD78322KC/KD: Reprogrammable version in ceramic package with window.

Ordering Information

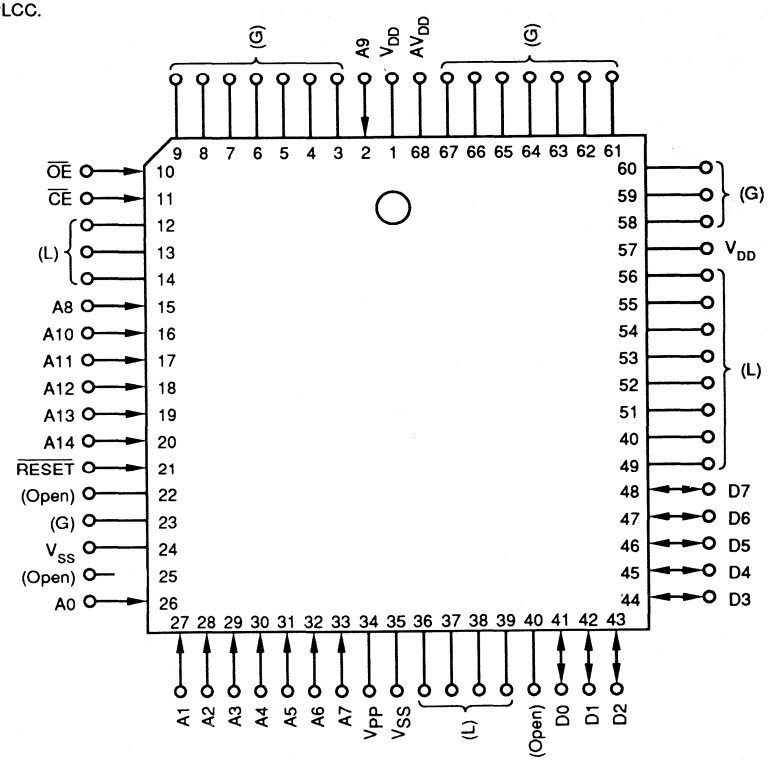
Part Number	Package Type	ROM
μPD78P322L μPD78P322GJ	68-Pin PLCC 74-Pin QFP	16-K OTPROM
μPD78P322KC μPD78P322KD	68-Pin LCC 74-Pin LCC ceramic with window	16-K UVPROM

2

Pin Configuration (top view)

For pin configuration in Normal Mode operation corresponding pin function tables, please refer to μPD78320/322 data sheet. Pin configuration in PROM programming mode ($\overline{RESET}$ = high and AV_{DD} = 0V).

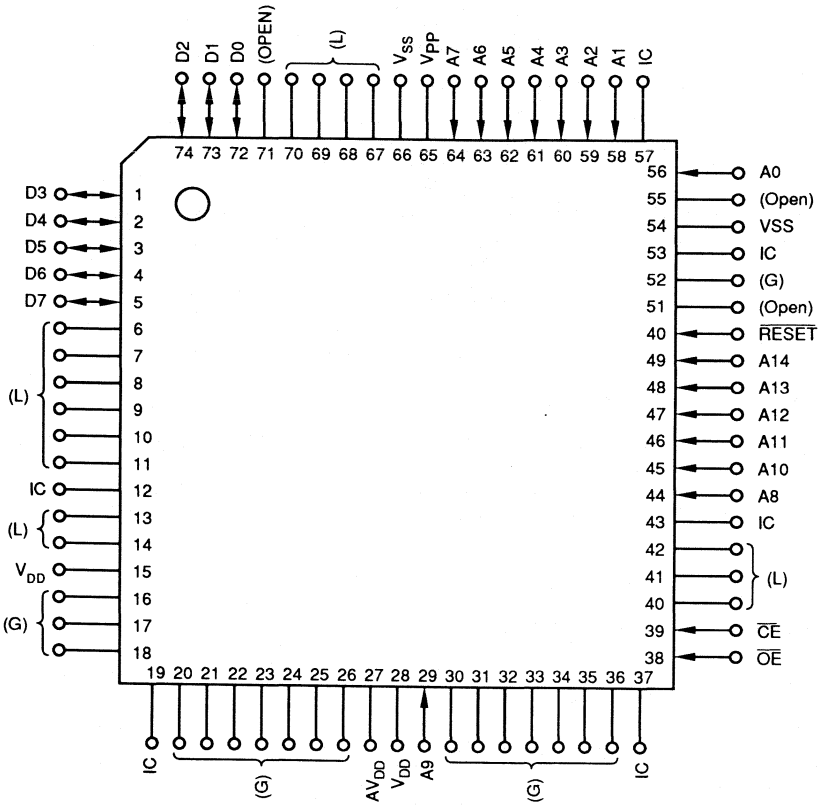
a) 68-pin ceramic leaded chip carrier and
68-pin PLCC.



Cautions: The recommended conditions for the unused pins in the PROM programming mode are indicated in parentheses.
L: Connect each pin to V_{SS} with a resistor.
G: Connect the pin to V_{SS}.
Open: Leave the pin unconnected.

A0-A14	:	Address 0-14	$\overline{RESET}$	:	} Programming Mode Set
D0-D7	:	Data 0-7	AV_{DD}	:	
$\overline{CE}$	:	Chip Enable	V_{PP}	:	Programming Power Supply
$\overline{OE}$	:	Output Enable			

b) 74-pin ceramic leaded chip carrier with window and
74-pin plastic quad-flat package.



Cautions: The recommended conditions for the unused pins in the PROM programming mode are indicated in parentheses.
L: Connect each pin to V_{SS} with a resistor.
G: Connect the pin to V_{SS}.
Open: Leave the pin unconnected.

Remarks: IC is internally connected. Do not connect the pin to the external.

A0-A14	:	Address 0-14	$\overline{RESET}$	:	} Programming Mode Set
D0-D7	:	Data 0-7	AV_{DD}	:	
$\overline{CE}$	:	Chip Enable	V_{PP}	:	Programming Power Supply
$\overline{OE}$	:	Output Enable			

Pin Functions in PROM Programming Mode ($\overline{RESET}$ = H, AV_{DD} = 0V)

Pin Name	I/O	Function
AV_{DD}	I	PROM programming mode setting
$\overline{RESET}$		
A0-A14	I	Address bus
D0-D7	I/O	Data bus
$\overline{CE}$	I	PROM enable input
$\overline{OE}$	I	Read strobe to PROM
V_{PP}	—	Write power supply
V_{DD}		Positive power supply
V_{SS}		GND

Differences Between μPD78P322 and μPD78322

The μPD78P322 is a product provided by replacing μPD78322 internal mask ROM with reprogrammable EPROM.

In functions other than the PROM specifications such as write/verify, the μPD78P322 is the same as the μPD78322 except for the EA pin function. The μPD78P322 does not have the EA pin. The Table below lists the differences between the μPD78P322 and μPD78322.

For details on the CPU function and on-chip hardware, refer to the μPD78322 User's Manual, etc.

Differences between μPD78P322 and μPD78322

Item \ Product Name	μPD78P322	μPD78322
Internal Program Memory	EPROM	Mask ROM
EPROM programming pin	Contained	Not contained
$\overline{EA}$ Pin	Not contained	Contained
Package	68-pin plastic leaded chip carrier 74-pin plastic quad-flat package	
	68-pin ceramic leaded chip carrier with a window (Note) 74-pin ceramic leaded chip carrier with a window (Note)	—

Note: Reprogrammable

PROM Programming

The μPD78P322 internal program memory is 16384 x 8-bit electrically programmable PROM. To program PROM, set the PROM programming mode by using the RESET and AV_{DD} pins.

The programming characteristics are compatible with the μPD27C256A programming characteristics.

Pin Function in Programming Mode

Function	Normal Operation Mode	Programming Mode
Address Input	P00-P07, P80, P20, P81-P85	A0-A14
Data Input	P40-P47	D0-D7
Chip Enable/Program Pulse	P31	$\overline{CE}$
Output Enable	P30	$\overline{OE}$
Program Voltage	VPP	
Mode Control	$\overline{RESET}$, AV_{DD}	

Operation Mode

When the $\overline{RESET}$ pin is set high and the AV_{DD} pin is set to 0V, the μPD78P322 enters the program write/verify mode. The Table below lists the PROM programming operation mode according to how the $\overline{CE}$ and $\overline{OE}$ pins are set.

By setting the μPD78P322 to the read mode, the PROM contents can be read.

Treat the unused pins exactly as indicated on Pin Configuration shown above.

PROM Programming Operation Mode

Mode	$\overline{RESET}$	AV_{DD}	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}	D0-D7
Program Write	H	0V	L	H	+12.5V	+6V	Data input
Program Verify			H	L			Data output
Program Inhibit			H	H			High impedance
Read			L	L	+5V	+5V	Data output
Output Disable			L	H			High Impedance
Standby			H	L/H			High Impedance

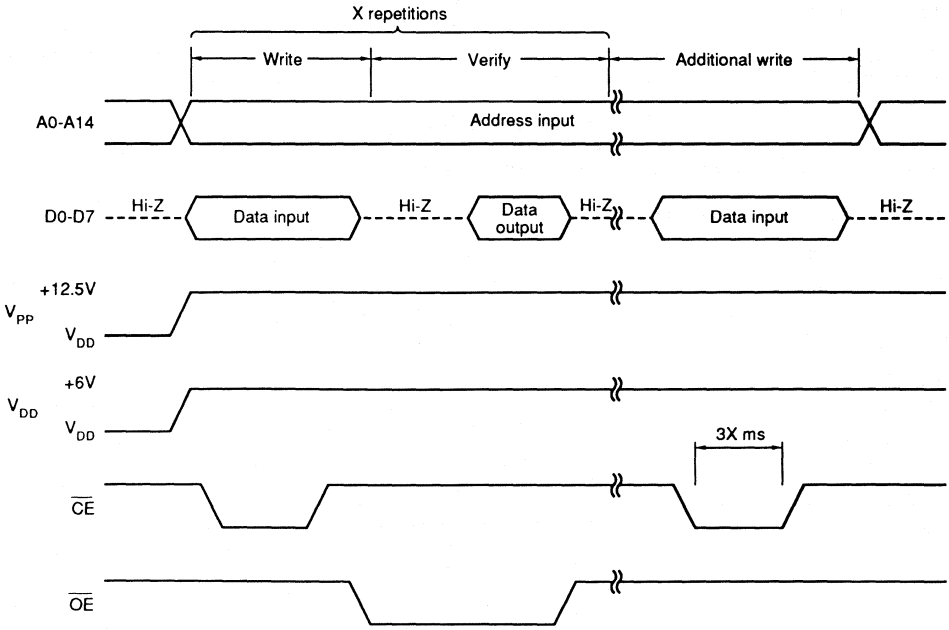
Caution: When V_{PP} is set to +12.5V and V_{DD} is set to +6V, setting both $\overline{CE}$ and $\overline{OE}$ low is inhibited.

PROM Write Procedure

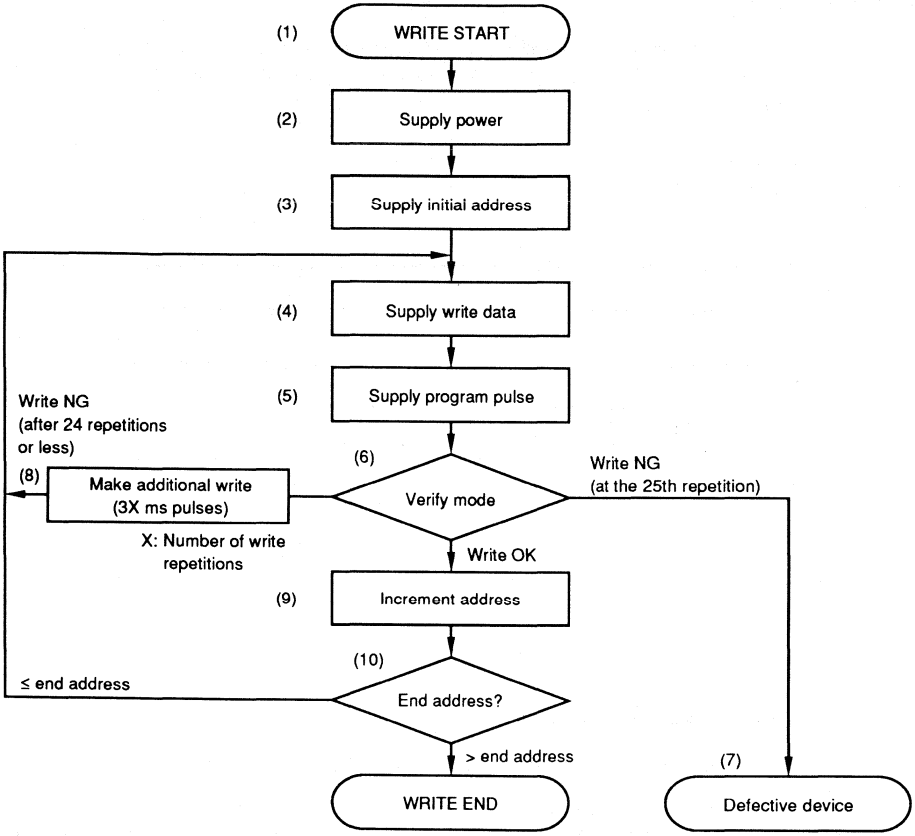
PROM can be written at the high speed according to the following procedure:

(1) Fix the $\overline{RESET}$ pin high and the AV_{DD} pin to 0V. Connect unused pins as indicated in Pin Configuration shown above.
(2) Supply +6V to the V_{DD} pin and +12.5V to the V_{PP} pin.
(3) Supply an initial address.
(4) Supply write data.
(5) Supply a 1-ms program pulse (active low) to the $\overline{CE}$ pin.
(6) Execute the verify mode. If the data is written normally, proceed to (9). If it is not written normally go to (8) and repeat steps (4) - (6).If the data is not written normally after 25 repetitions of the steps, proceed to (7).
(7) Assume the device to be defective. Stop write operation.
(8) Supply write data and X (number of (4) - (6) repetitions) x 3ms program pulses (additional write).
(9) Increment the address.
(10) Repeat (4) - (9) until the end address is reached.

Following Figure shows the PROM write/verify timing ((2) - (8) above).



Prom Write/Verify Timing

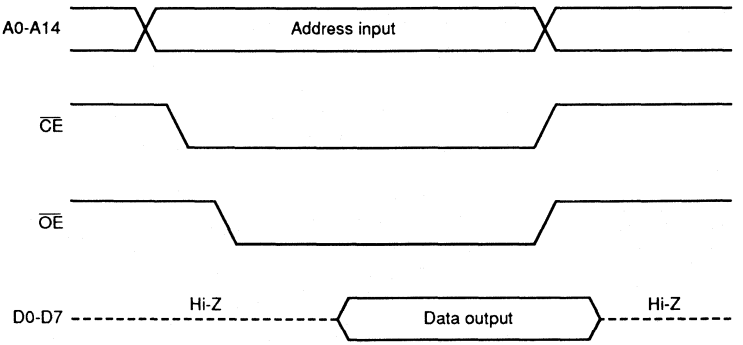


Write Flowchart

PROM Read Procedure

The PROM contents can be read into the external data bus (D0-D7) according to the following procedure:

(1) Fix the $\overline{RESET}$ pin high and the AV_{DD} pin to 0V. Treat unused pins exactly as indicated on Pin Configuration shown above.
(2) Supply +5V to the V_{DD} and V_{PP} pins.
(3) Input the address of the data to be read to the A0-A14 pins.
(4) Execute the read mode.
(5) The data is output to the D0-D7 pins.



PROM Read Timing

Erasion Characteristics (μPD78P322KC/KD Only)

The programmed data contents of the μPD78P322KC/KD can be erased (FFH) by applying light whose wave length is shorter than about 400 nm.

To erase the μPD78P322KC/KD program memory contents, normally apply ultraviolet rays having the 254-nm wave length. All the radiation amount required to completely erase the μPD78P322KC/KD is 15Ws/cm^2 (ultraviolet strength x erasion time) at the minimum. The erasion time is about 15-20 minutes when a 12000 μW/cm^2 ultraviolet lamp is used. However, the erasion time may be prolonged due to ultraviolet lamp performance deterioration, dirty package window, etc. For erasion, place the μPD78P322KC/KD at a position within 2.5 cm from an ultraviolet lamp. If a filter is attached to the ultraviolet lamp, remove the filter before erasion.

Window Seal (μPD78P322KC/KD Only)

To prevent erroneous erasion of the EPROM contents by light other than erasion lamp light or erroneous operation of the internal circuit other than EPROM because of light, put a protection seal on the window except when EPROM contents are erased.

Package Information

Package dimensions of 68-pin ceramic leaded chip carriers with a window (unit: mm)

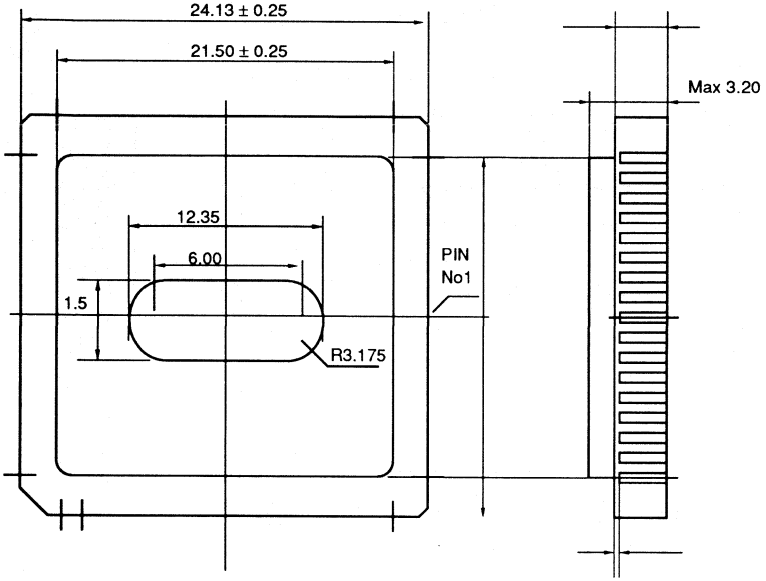
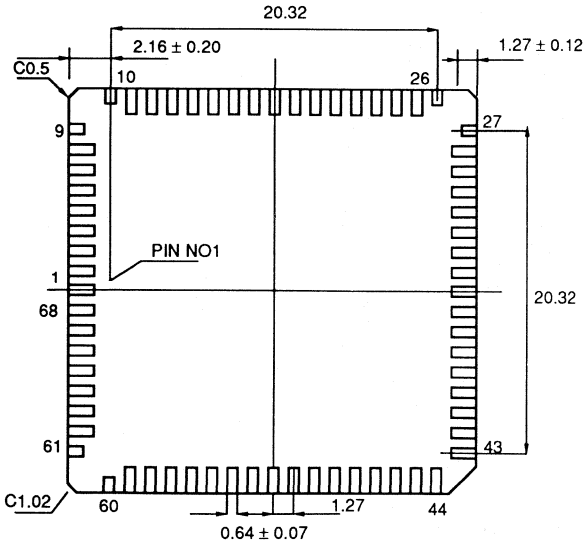


Figure 1
68-PIN-LCC PACKAGE (μPD78P322KC)



Package dimensions of 74-pin ceramic leaded chip carriers with a window (unit: mm)

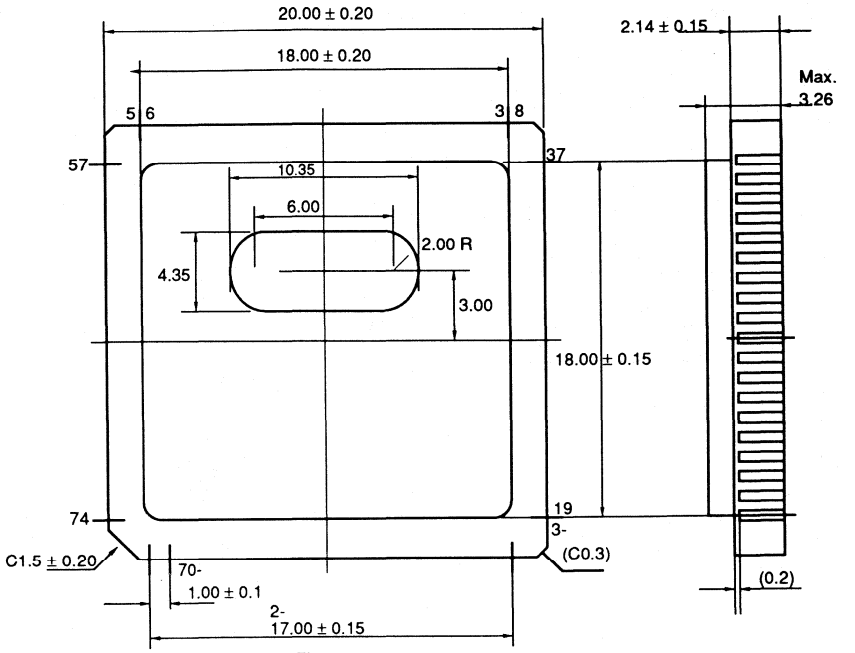
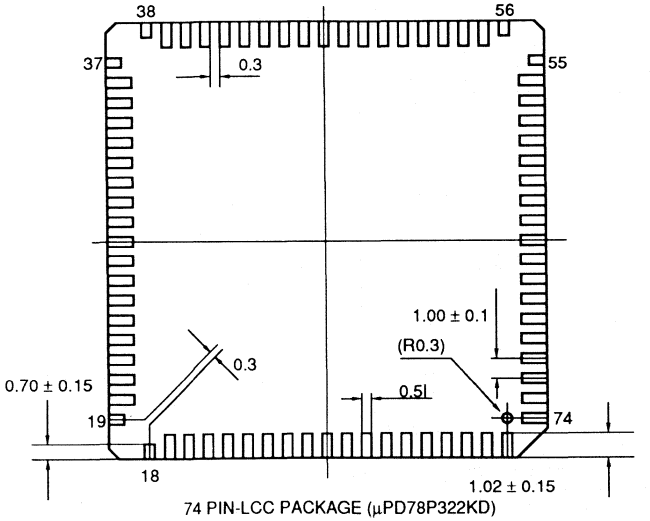
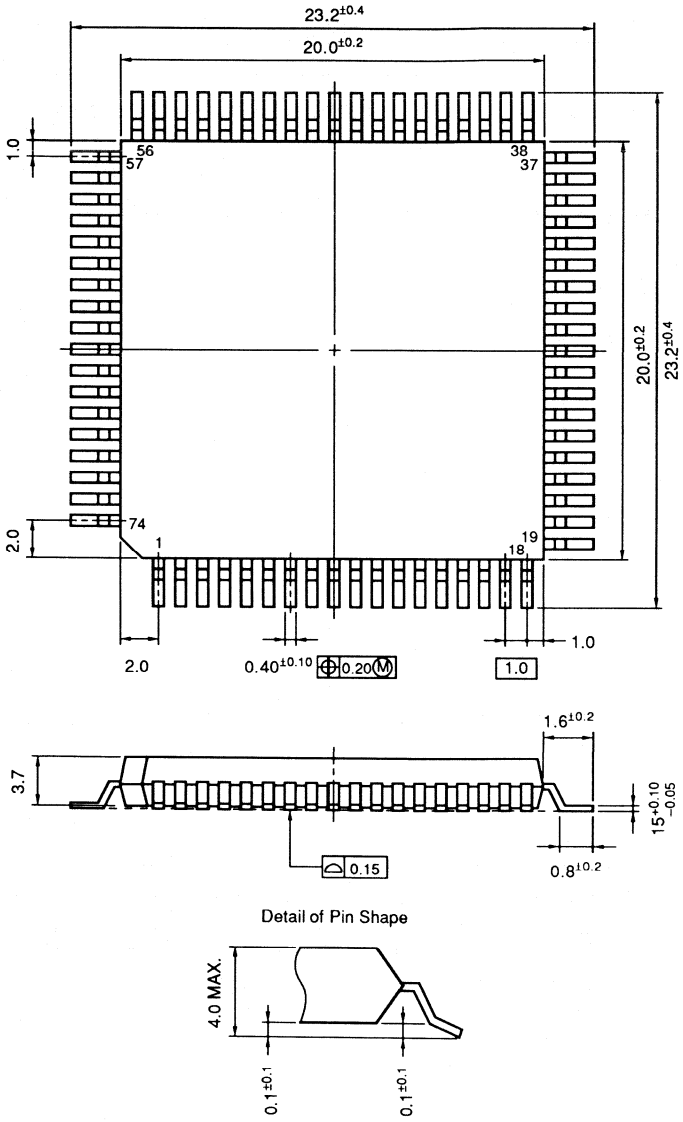


Figure 2



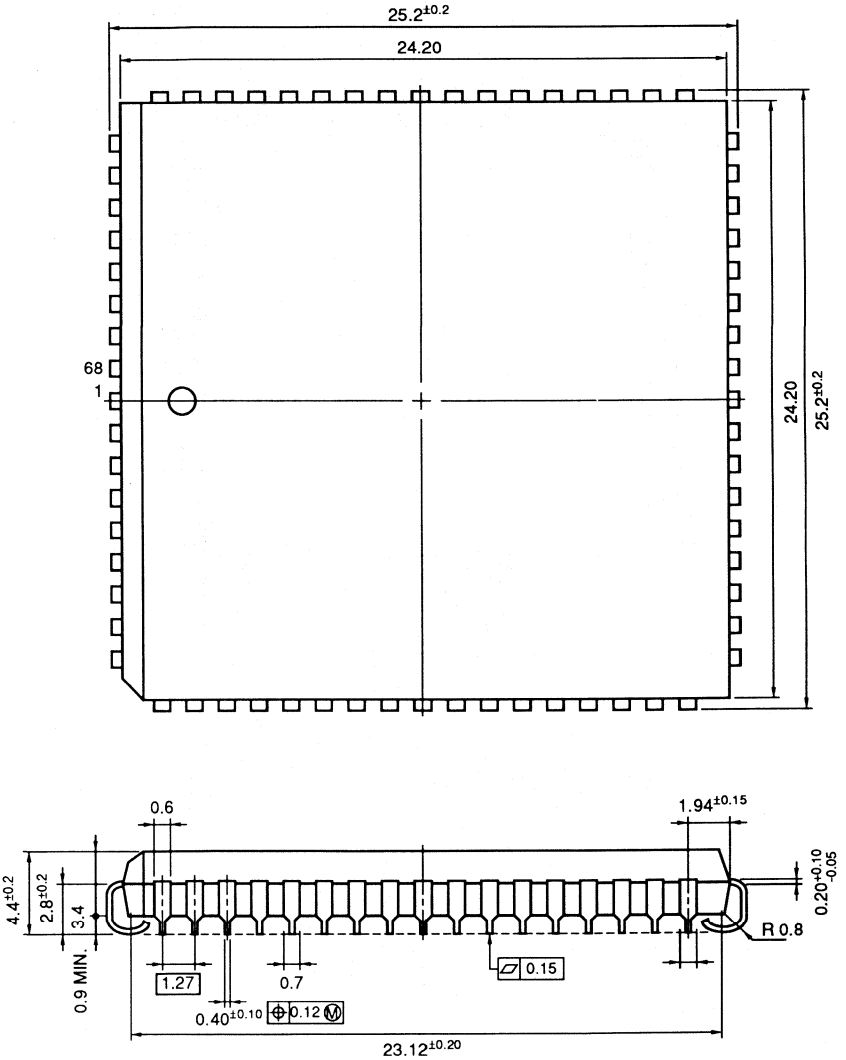
74 PIN-LCC PACKAGE (μPD78P322KD)

74-pin plastic quad-flat package (□ 20) dimension (unit: mm)



S74GJ-100-5BJ-1

68-pin plastic leaded chip carrier (□ 950) package dimensions (unit: mm)



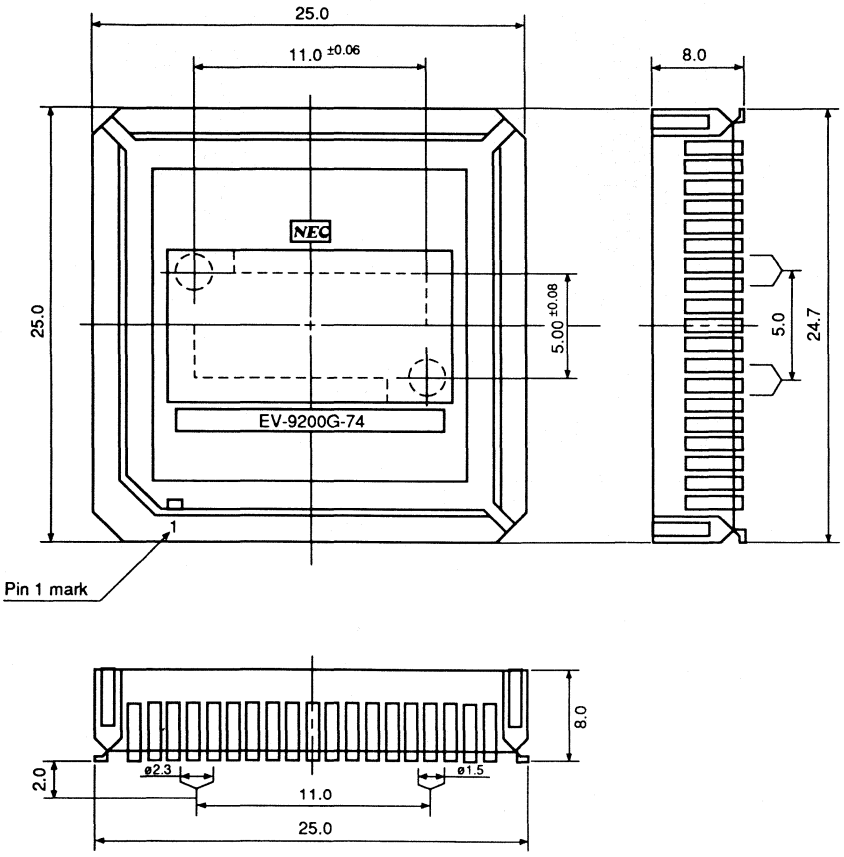
P68L-50A1-1

EV-9200G-74 Package Information and Pad Information

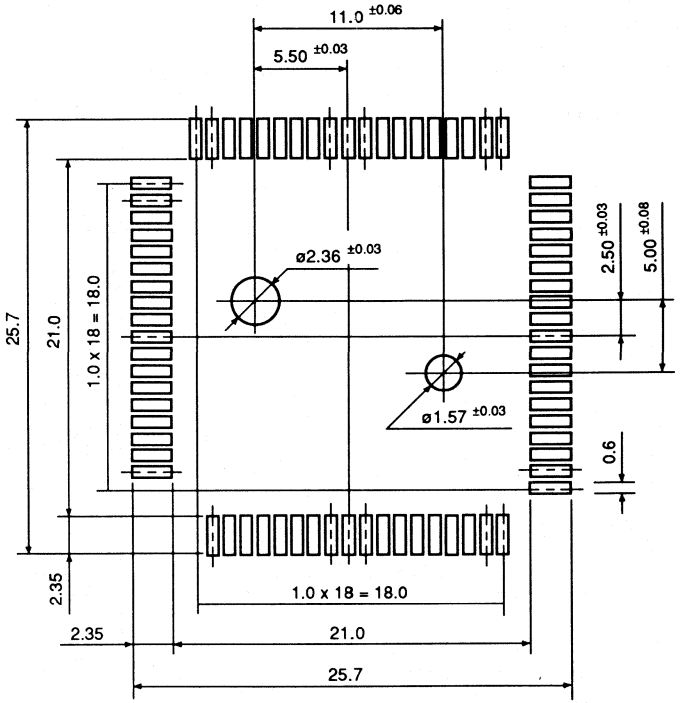
The μPD78P322KD can be installed on a printed circuit board in combination with socket EV-9200G-74 for leaded chip carrier having the same pin configuration as the quad-flat package (GJ) type.

The EV-9200G-74 package dimensions and pad drawing (for reference) are shown below:

(1) Package dimension (unit: mm)



(2) Pad drawing



Description

The μPD78327/μPD78328 are single-chip microcomputers designed for process and motor control. They feature a 16-bit CPU, an 8-bit external bus, and a powerful set of on-chip peripherals including counters, timers and a PWM output function plus 8-bit realtime output port, an A/D converter, two serial ports and a maximum of 52 input/output lines. An advanced interrupt handling facility includes a three level program-controlled hardware priority interrupt controller and three separate methods of handling interrupt requests including macro service and context switch. They are manufactured of 1.2μ CMOS process, operate from a single 5 volt power supply, and have a maximum oscillator frequency of 16 MHz. The μPD78328 has a 16k bytes of on-chip mask programmed ROM, and the μPD78327 is a ROM-less version. Both have 512 bytes of on-chip RAM and are supplied in two different packages, 64-pin SDIP and 64-pin plastic QFP.

The μPD78327/328 include an interface for a special dedicated memory chip, the μPD71P301 called Turbo Access Manager (TAM). The TAM includes memory, I/O interfaces, and an instruction pre-fetch pointer. This makes it possible to fetch instructions from external memory at the same high speed at which they can be fetched from on-chip ROM.

For development/evalution purpose, preproduction and small volume applications there is also an EPROM version μPD78P328 under development, as UVPROM type in ceramic and as OTP type in plastic packages.

The μPD78327/328 are most suitable for all kind of control applications and in particular for AC motor control in many different applications like HD drives, advanced Inverters etc.

Features

- High performance single-chip microcomputer:
  - 16-bit CPU.
  - 8-bit external bus.
  - 16K bytes onchip ROM (μPD78328).
  - 512 bytes onchip RAM.
- Powerful instruction set:
  - Software compatible to 78320/322.
  - 16-bit arithmetic/logical instructions.
  - Multiply/divide (16 x 16 bits, 32 + 16 bits).
  - Signed multiply instruction.
  - Bit manipulation instruction.
  - String instruction
- Minimum instruction time: 250nsec @16MHz
- 3-byte instruction pre-fetch queue
- Real-time pulse unit:
  - One of two timer output modes can be selected (6 set/reset output channels, 8 buffer output channels)
  - Six-phase PWM signals can be easily output
- 10-bit A/D converter with 8 channels
- One channel high speed 8-bit PWM signal output
- High performance interrupt control function
- Two channel serial communication interface
  - Asynchronous serial interface. (UART)
  - Serial Bus Interface
  - Dedicated Baud rate generator
- Three methods of interrupt service:
  - Vectored interrupts
  - Context switching
    Includes hardware save of all general registers
  - Macro Service
    Choice of eight different functions
- Watchdog timer
- Interface to Turbo Access Manager
- Standby function : STOP & HALT
- 64-pin SDIP/QFP packages

Ordering Information

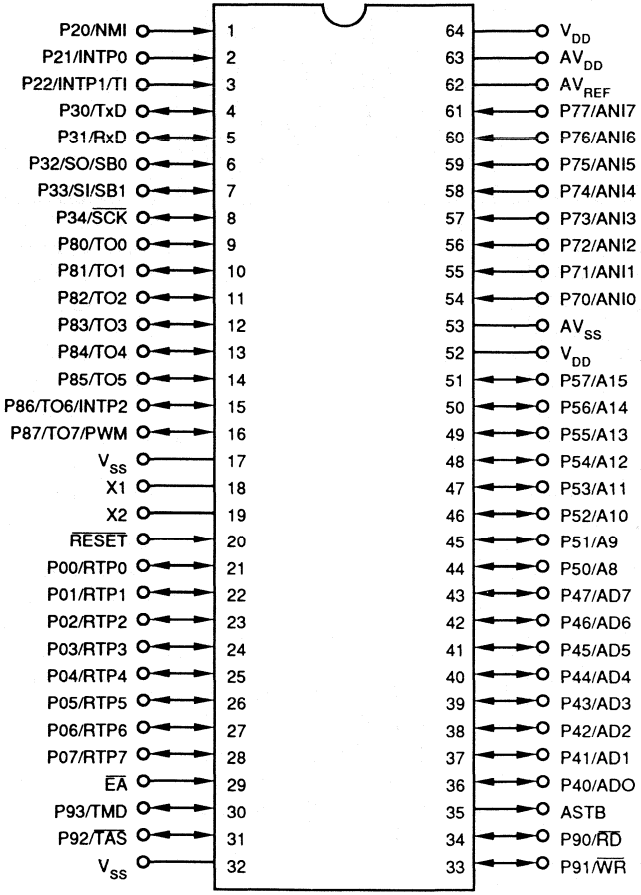
Part Number	Package Type	ROM
μPD78327CW	64-Pin SDIP	ROM less
μPD78327GF	64-Pin QFP	
μPD78328CW	64-Pin SDIP	16-K ROM
μPD78328GF	64-Pin QFP	
μPD78P328DW	64-Pin SDIP	16-K UVPROM
μPD78P328KB	64-Pin LCC ceramic with window	

Function Table

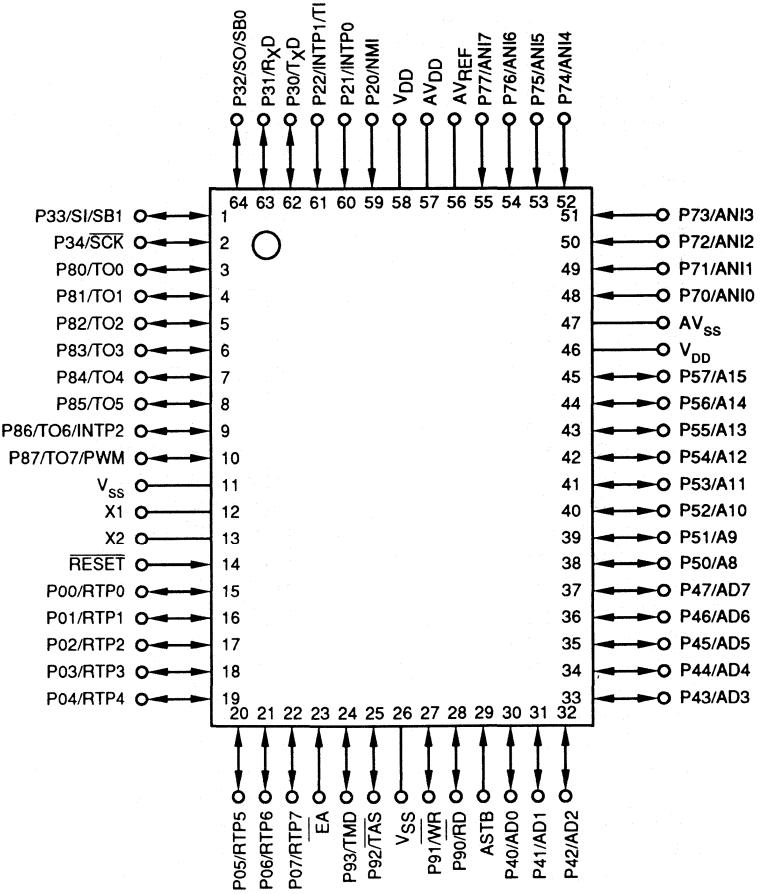
Number of basic instructions	109
Instruction cycle	0.25 μs (internal clock frequency: 8 MHz, external clock frequency: 16 MHz)
Built-in memory	• ROM: 16K bytes (μPD78328 only) • RAM: 512 bytes
Addressing space	64K bytes
General register	8 bits x 16 x 8 banks (memory mapping)
Real-time pulse unit	• 16-bit timer: 2 • 16-bit timer/event counter: 1 • 16-bit compare registers: 14 • 18-bit capture/compare registers: 1 • Two output modes can be selected. Mode 0 Set/reset output: 6 channels Toggle output: 1 channel Mode 1 Buffer output: 8 channels
PWM signal output function	8-bit resolution: 1 channel
A/D converter function	10-bit resolution: 8 channels
Interrupt function (External factors: 4) (Internal factors: 11)	• A 3-level priority can be specified by the software. • Three types of interrupt processing modes can be selected. (Vector interrupt function, context switching function, macro service function)
I/O line	Input ports: 11 Output ports: 41
Real-time output port function	4 bits x 2 channels or 8 bits x 1 channel
Serial interface with a dedicated baud rate generator	• UART: 1 channel • SBI (NEC serial bus interface): 1 channel
Package	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP
Others	• 78K/III architecture • Control signal output function for the turbo access manager • Standby function (STOP/HALT) • Watchdog timer function

Pin Configuration

1. 64-pin SDIP



2. 64-pin QFP and 64-pin LCC

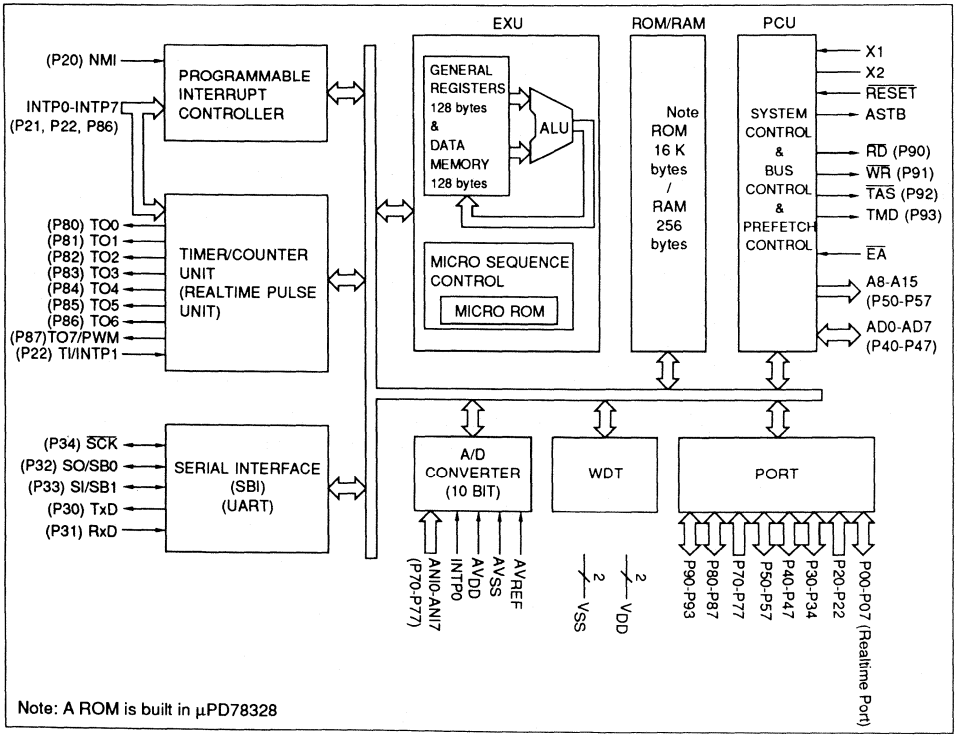


Pin Identification

P00 to P07	:	Port 0
P20 to P27	:	Port 2
P30 to P34	:	Port 3
P40 to P47	:	Port 4
P50 to P57	:	Port 5
P70 to P77	:	Port 7
P80 to P85	:	Port 8
P90 to P93	:	Port 9
NMI	:	Nonmaskable Interrupt
INTP0 to INTP2	:	Interrupt from Peripherals 0 to 2
RTP0 to RTP7	:	Real-time Ports 0 to 7
TI	:	Timer Input
TxD	:	Transmit Data
RxD	:	Receive Data
SB0/SO	:	Serial Bus/Serial Output
SB1/SI	:	Serial Bus/Serial Input
$\overline{SCK}$	:	Serial Clock
TO0 to TO7	:	Timer Outputs 0 to 7
RESET	:	Reset
X1, X2	:	Crystal 1 or 2
PWM	:	Pulse Wide Modulation Output
$\overline{EA}$	:	External Access
$\overline{TMD}$	:	Turbo Mode
$\overline{TAS}$	:	Turbo Access Strobe
$\overline{WR}$	:	Write
$\overline{RD}$	:	Read
ASTB	:	Address Strobe
AD0 to AD7	:	Address 0 to 7 or Data 0 to 7
A8 to A15	:	Address 8 to 15
ANI0 to ANI7	:	Analog Input 0 to 7
AV_{REF}	:	Analog Reference Voltage
AV_{SS}	:	Analog V_{SS}
AV_{DD}	:	Analog V_{DD}
V_{DD}	:	Power Supply
V_{SS}	:	Power Supply

2

Block Diagram



Note: A ROM is built in μPD78328

1. Pin Functions

1.1 Port Pins

Pin Name	Input/ Output	Dual Function Pin	Function
P00 to P07	Input/ Output	RTP0- RTP7	Port 0 4-bit or 8-bit input/output port Inputs and outputs can be specified bit by bit. These pins also function as a real-time output port.
P20 P21 P22	Input	NMI INTP0 INTP1/TI	Port 2 3-bit input (nondedicated) port
P30 P31 P32 P33 P34	Input/ Output	TxD RxD SO/SB0 SI/SB1 $\overline{SCK}$	Port 3 5-bit input/output port Inputs and outputs can be specified bit by bit.
P40 to P47	Input/ Output	AD0 to AD7	Port 4 8-bit input/output port Inputs and outputs can be specified in 8-bit units.
P50 to P57	Input/ Output	A8 to A15	Port 5 8-bit input/output port Inputs and outputs can be specified bit by bit.
P70 to P77	Input	ANI0 to ANI7	Port 7 8-bit input dedicated port
P80	Input/ Output	TO00	Port 8 8-bit input/output port Inputs and outputs can be specified bit by bit.
P81		TO01	
P82		TO02	
P83		TO03	
P84		TO04	
P85		TO05	
P86		TO06/INTP2	
P87		TO07/PWM	
P90	Input/ Output	$\overline{RD}$	Port 9 4-bit input/output port Inputs and outputs can be specified bit by bit.
P91		$\overline{WR}$	
P92		$\overline{TAS}$	
P93		TMD	

1.2 Non-port Pins

Pin Name	Input/ Output	Dual Function Pin	Function
RTP0 to RTP7	Output	P00 to P07	Synchronized with a trigger signal sent from the real-time pulse unit (RPU) and outputs a pulse in real-time.
NMI	Input	P20	Receives an input signal of a nonmaskable interrupt request. The mode register can specify the rising or falling edge as the effective edge with this request.
INTP0	Input	P21	Receive an input signal of an external interrupt request with which the mode register can specify the effective edge.
INTP1		P22/TI	
INTP2		P86/T06	
TI	Input	P22/INTP1	Receives an input of an external count clock signal to the timer 1 (TM1).
RxD	Input	P30	Receives an input signal of serial data of the asynchronous serial interface (UART).
TxD	Output	P31	Receives an output signal of serial data of the asynchronous serial interface (UART).
SO	Output	P32/SB0	Receives an output signal of serial data in the 3-wire mode of the clock synchronous serial interface.
SI	Input	P33/SB1	Receives an input signal of serial data in the 3-wire mode of the clock synchronous serial interface.
SB0	Input/ Output	P32/SO	Receive an input signal and an output signal of serial data in the SBI mode of the clock synchronous serial interface.
SB1		P33/SI	
$\overline{SCK}$	Input/ Output	P34	Receives an input and an output of a serial clock signal of the clock synchronous serial interface.
AD0 to AD7	Input Output	P40 to P47	Multiplexed address/data bus when an external memory is expanded.
A8 to A15	Output	P50 to P57	Address bus when an external memory is expanded
TO00	Output	P80	Receive a pulse output from the real-time pulse unit.
TO01		P81	
TO02		P82	
TO03		P83	
TO04		P84	
TO05		P85	
TO06		P86/INTP2	
TO07		P87/PWM	
PWM	Output	P87/TO7	Receives a PWM signal output from the real-time pulse unit.
$\overline{RD}$	Output	P90	Receives a strobe signal output for read operations of an external memory.
$\overline{WR}$		P91	Receives a strobe signal output for write operations of an external memory.
$\overline{TAS}$		P92	Receives a control signal output to access the turbo access manager μPD71P301.
TMD		P93	

(to be continued)

(cont'd)

Pin Name	Input/ Output	Dual Function Pin	Function
ASTB	Output	—	Receives a timing signal output to externally latch address information output to port 4 for accessing an external memory.
$\overline{EA}$	Input	—	For the μPD78328, normally the $\overline{EA}$ pin is connected to the V_{DD} pin. Connecting the $\overline{EA}$ pin to the V_{SS} pin enters the ROM-less mode, enabling access to an external memory. For the μPD78327, this pin must be fixed to 0 (low level). The level of the $\overline{EA}$ pin cannot be changed during operations.
ANI0 to ANI7	Input	P70-P77	Analog input to the A/D converter
AV_{REF}	Input	—	A/D converter reference voltage input.
AV_{DD}	—	—	Analog power supply of the A/D converter.
AV_{SS}	—	—	Ground of the A/D converter.
$\overline{RESET}$	—	—	System reset input
X1	Input	—	Crystal input pin for system clock oscillation. A clock signal provided externally is input to the X1 pin.
X2	—	—	
V_{DD}	—	—	Positive power supply pin
V_{SS}	—	—	Ground pin

1.3 Input/Output Circuit of Each Pin

The type of I/O circuit of each pin is shown in following table and afterwards the different types of I/O circuit are given.

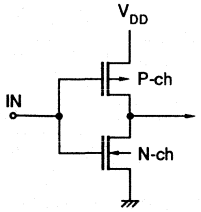
Input/Output Circuit of Each Pin

Terminal	I/O Circuit Type
P00-P07	5
P20/NMI	2
P21/INTP0	
P222/INTP1/TI	
P30/TxD	
P31/RxD	
P32/SO/SB0	8
P33/SI/SB1	
P34/$\overline{SCK}$	
P40-P47, AD0-AD7	
P50-P57, A8-A15	
P70-P77, ANI0-ANI7	9

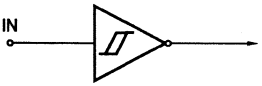
Terminal	I/O Circuit Type
P80-P85, TO0-TO5	5
P86/TO6/INTP2	6
P87/TO7/PWM	5
P90/$\overline{RD}$	
P91/$\overline{WR}$	
P92/$\overline{TAS}$	
P93/TMD	
ASTB	4
$\overline{EA}$	1
$\overline{RESET}$	2

Input/Output Circuits of Each Pin

Type 1

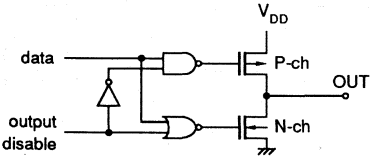


Type 2



Schmitt-trigger input with hysteresis characteristics

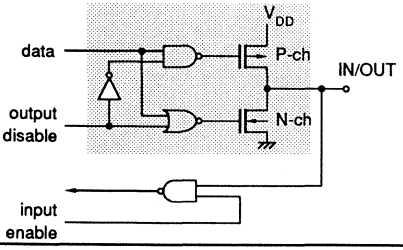
Type 4



Push-pull output which can output highimpedance (Both the positive and negative channels are off).

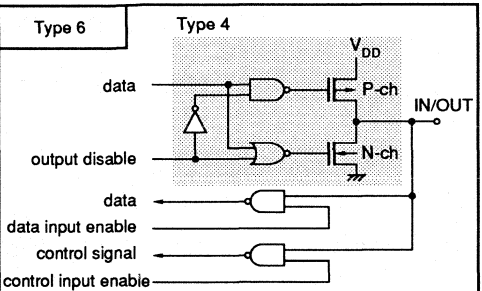
Type 5

Type 4

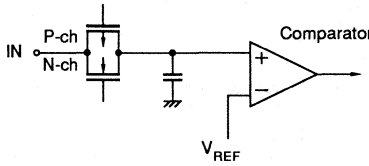


Type 6

Type 4

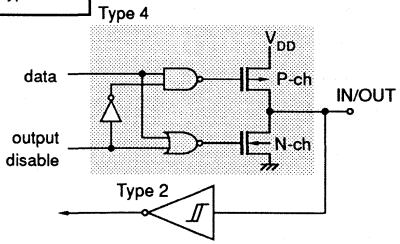


Type 7



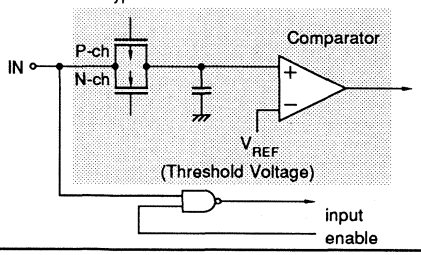
Type 8

Type 4



Type 9

Type 7



2

Absolute Maximum Ratings
Ta = 25°C

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5 to +7.0	V
	AV_{DD}		-0.5 to V_{DD} +0.5	V
	AV_{SS}		-0.5 to +0.5	V
Input Voltage	V_I		-0.5 to V_{DD}+0.5	V
Output Voltage	V_O		-0.5 to V_{DD}+0.5	V
Output Current Low	I_{OL}	at 1 Pin	4.0	mA
		All Output Pin Total	90	mA
Output Current High	I_{OH}	at 1 Pin	- 1.0	mA
		All Output Pin Total	-20	mA
Reference Voltage	AV_{REF}	f_{XX}≤16MHz	-0.5 to AV_{DD} ±0.3	V
Operating Temperature	t_{opt}		-10 to +70	°C
Storage Temperature	t_{stg}		-65 to +150	°C

Recommended Operating Conditions

OSC Frequency	Ta	V_{DD}
8 MHz < f_{XX} ≤ 16 MHz	-10 C to +70 C	+5.0V+10%

Capacitance (Ta=25°C,V_{DD}=V_{ss}=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f_C = 1MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins			20	pF
I/O Capacitance	C_{IO}	Returned to 0V			20	pF

DC Characteristics

Ta = -10°C to +70°C, V_{DD}=5.0V±10%, V_{SS}=0V

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL}			0		0.8	V
Input High Voltage	V_{IH1}	*1		2.2			V
	V_{IH2}	*2		$0.8V_{DD}$			
Output Low Voltage	V_{OL}	I_{OL}=2.0mA				0.45	V
Output High Voltage	V_{OH}	I_{OH}=-400μA		V_{DD}-1.0			V
Input Leakage Current	I_{LI}	0V≤V_I≤V_{DD}				±10	μA
Output Leakage Current	I_{LO}	0V≤V_O≤V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operation Mode			40	65	mA
	I_{DD2}	Halt Mode			20	35	mA
Data Retention Voltage	V_{DDDR}	STOP Mode		2.5			V
Data Retention Current	I_{DDDR}	STOP Mode	V_{DDDR}=2.5V		2	10	μA
			V_{DDR}=5.0±10%		10	50	μA

Notes:

*1. All except $\overline{RESET}$, X1, X2, P20/NMI, P21/INTE0, P22/INTE1/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{SCK}$

*2. $\overline{RESET}$, X!, X2, P20/NMI, P21/INTE0, P22/INTE1/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{SCK}$

2

AC Characteristics

Read/Write Operation Ta = -10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Normal memory read/write operation (with general-purpose memory /turbo access manager connected).

Parameter	Symbol	Test Conditions	Min.	Max.	Units
System Clock Cycle Time	t_{CYK}		125	250	ns
Address Setup Time to ASTB↓	t_{SAST}		32		ns
Address Hold from ASTB↓	t_{HSTA}		32		ns
Address to $\overline{RD}$↓ Delay Time	t_{DAR}		85		ns
Address Float Time from $\overline{RD}$↓	t_{FRA}			0	ns
Address to Data Input	t_{DAID}			222	ns
$\overline{RD}$↓ to Data Input	t_{DRID1}			112	ns
ASTB↓ to $\overline{RD}$↓ Delay Time	t_{DSTR}		42		ns
Data Hold Time from $\overline{RD}$↑	t_{HRID}		0		ns
$\overline{RD}$↑ to Adress Delay Time	t_{DRA}		37		ns
$\overline{RD}$ Width Low	t_{WRL}		157		ns
ASTB Width High	t_{WSTH}		37		ns
Adress to $\overline{WR}$↓ Delay Time	t_{DAW}		85		ns
ASTB↓ to Data Output	t_{DSTOD}			102	ns
$\overline{WR}$↓ to Data Output	t_{DWOD}			40	ns
ASTB↓ to $\overline{WR}$↓ Delay Time	t_{DSTW}		42		ns
Data Setup to $\overline{WR}$↑	t_{SODW}		147		ns
Data Hold Time from $\overline{WR}$↑	t_{HWOD}		32		ns
$\overline{WR}$↑ to ASTB↑ Delay Time	t_{DWST}		42		ns
$\overline{WR}$ Width Low	t_{WWL}		157		ns

Branch Operation

Continuous instruction code fetch operation (with general-purpose memory/turbo access manager connected).

Parameter	Symbol	Test Conditions	Min.	Max.	Units
$\overline{TAS}$ Width Low	t_{WTAL}		37		ns
$\overline{TAS}$ Width High	t_{WTAH}		42		ns
$\overline{TAS}$ ↑ to Data Input	t_{DTAID}			80	ns
TMD ↑ to $\overline{TAS}$ ↑	t_{DTMRTA}		157		ns
RD ↓ to Data Input	t_{DRID2}			65	ns
$\overline{TAS}$ Setup to ASTB ↓	t_{STAST}		32		ns
TMD Setup to ASTB ↓	t_{STMST}		42		ns
TMD ↓ to $\overline{TAS}$ ↑	t_{DTMFTA}		95		ns
ASTB ↓ to TMD ↓ Delay Time	t_{DSTTM}		85		ns
Data Hold Time from $\overline{TAS}$ ↑	t_{HTMID}		0		ns

Serial Operation

Ta = -10°C to +70°C, V_{DD}=5.0V±10%, V_{SS}=0V

Parameter	Symbol	Test Conditions		Min.	Max.	Units
$\overline{SCK}$ Cycle Time	t_{CYSK}	$\overline{SCK}$ Output	Note	1		μs
		$\overline{SCK}$ Input	External clock	1		μs
$\overline{SCK}$ Width Low	t_{WSKL}	$\overline{SCK}$ Output	Note	420		ns
		$\overline{SCK}$ Input	External clock	420		ns
$\overline{SCK}$ Width High	t_{WSKH}	$\overline{SCK}$ Output	Note	420		ns
		$\overline{SCK}$ Input	External clock	420		ns
SI Setup Time to $\overline{SCK}$ ↑	t_{SRXSK}			80		ns
SI Hold Time to $\overline{SCK}$ ↑	t_{HSKRX}			80		ns
SO Delay Time from $\overline{SCK}$ ↓	t_{DSKTX}				210	ns

Note: Internally divided by 8

2

A/D Converter Characteristics

Ta = -10°C to +70°C, V_{SS}=AV_{SS}=0V, 3.4V≤AV_{REF}≤AV_{DD}, V_{DD}=+5V±10%, V_{DD} - 0.5V ≤ AV_{DD} ≤ V_{DD}

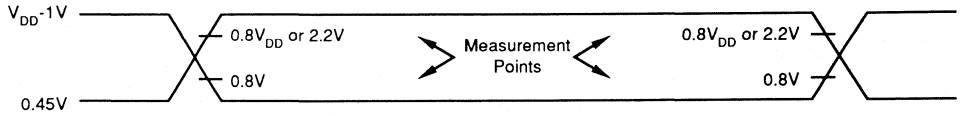
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Resolution			10			Bits
Relative Accuracy					±0.3%	FSR
Quatization Error					±1/2	LSB
Conversion Time	t_{CONV}		144			t_{CYK}
Sampling Time	t_{SAMP}		24			t_{CYK}
Zero Offset Error				±1.5		LSB
Gain Error				±1.5		LSB
Linearity Error				±1.5		LSB
Analog Input Voltage	V_{IAN}		0		VA_{REF}	V
VA_{REF} Current	AI_{REF}			1.0	3.0	mA
AV_{DD} supply Current	AI_{DD}			2.0	6.0	mA

Bus Timing Depending on Tcyk

Symbol	Calculation Expression	Min./Max.	Unit
t_{SAST}	0.5 T - 30	Min.	ns
t_{HSTA}	0.5 T - 30	Min.	ns
t_{DAR}	T - 40	Min.	ns
t_{DAID}	(2.5 + n) T - 90	Max.	ns
t_{DRID1}	(1.5 + n) T - 75	Max.	ns
t_{DSTR}	0.5 T - 20	Min.	ns
t_{DRA}	0.5 T - 25	Min.	ns
t_{WRL}	(1.5 + n) T - 30	Min.	ns
t_{WSTH}	0.5 T - 25	Min.	ns
t_{DAW}	T - 40	Min.	ns
t_{DSTOD}	0.5 T + 40	Max.	ns
t_{DSTW}	0.5 T - 20	Min.	ns
t_{SODW}	1.5 T - 40	Min.	ns
t_{HWOD}	0.5 T - 30	Min.	ns
t_{DWST}	0.5 T - 20	Min.	ns
t_{WWL}	(1.5 + n) T - 30	Min.	ns
t_{WTAL}	0.5 T - 25	Min.	ns
t_{WTAH}	0.5 T - 20	Min.	ns
t_{DTAID}	T - 45	Max.	ns
t_{DTMRTA}	1.5 T - 30	Min.	ns
t_{DRID2}	T - 60	Max.	ns
t_{STAST}	0.5 T - 30	Min.	ns
t_{STMST}	0.5 T - 20	Min.	ns
t_{DTMFTA}	T - 30	Min.	ns
t_{DSTTM}	T - 40	Min.	ns

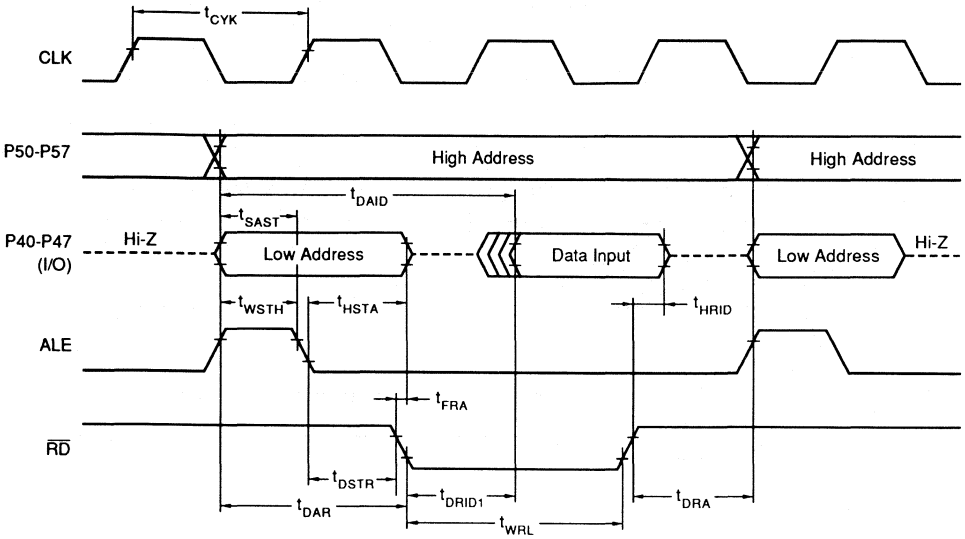
Note: t = T_{CYK} = $1/f_{CLK}$ (f_{CLK}: Internal System Clock)
n = number of wait cycles defined by user software
The parameters not included in the above list are not dependent on t_{CYK}.

AC Timing Measurement Points

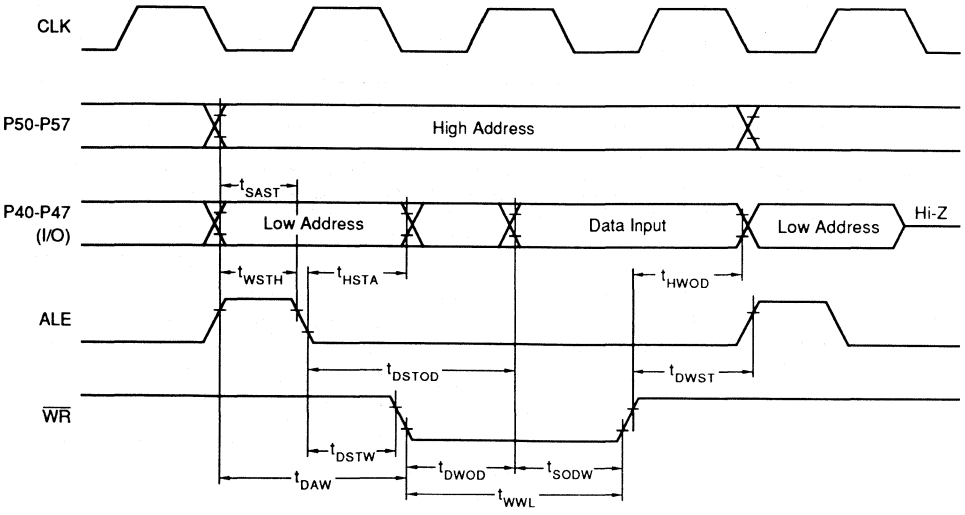


Timing Diagrams

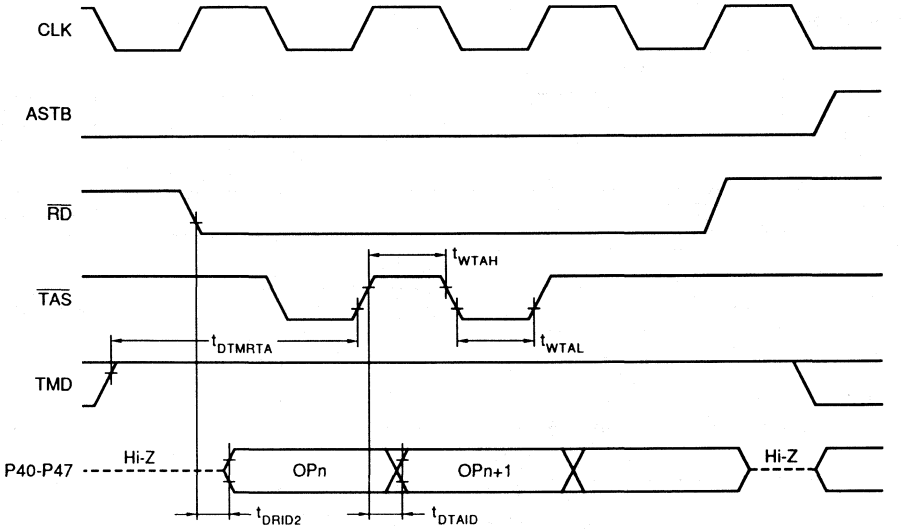
Read Operation



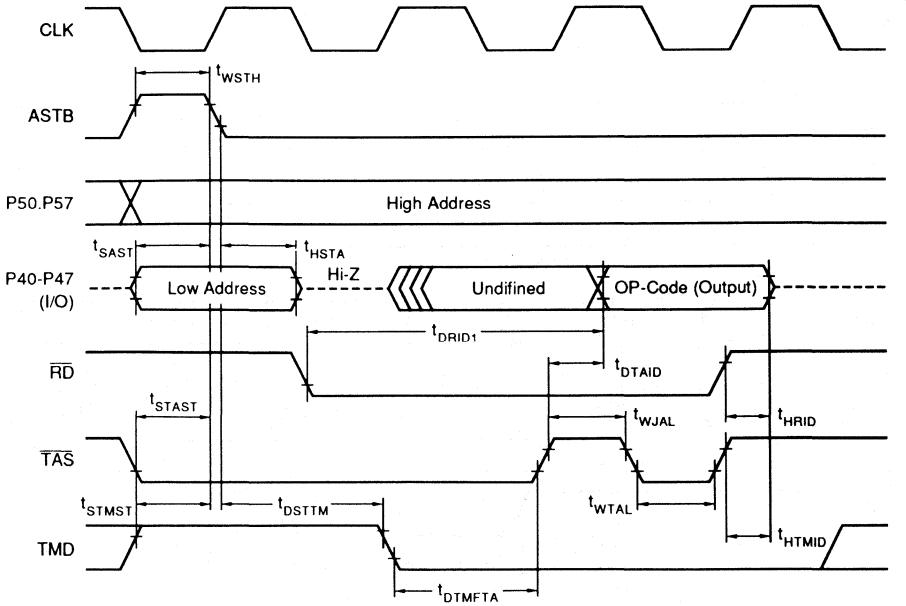
Write Operation



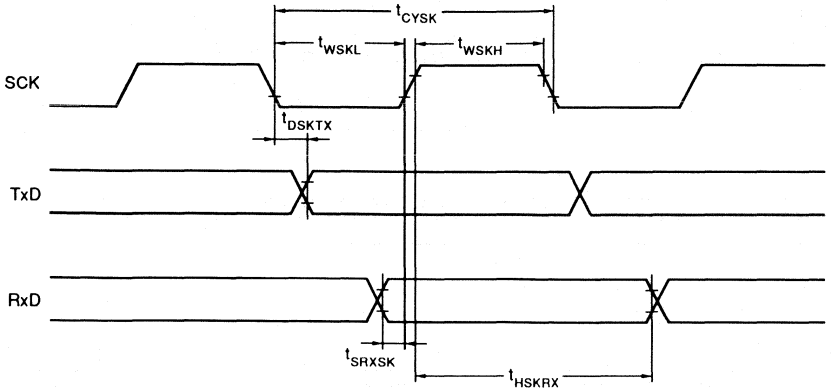
Turbo Fetch Operation



Branch Operation

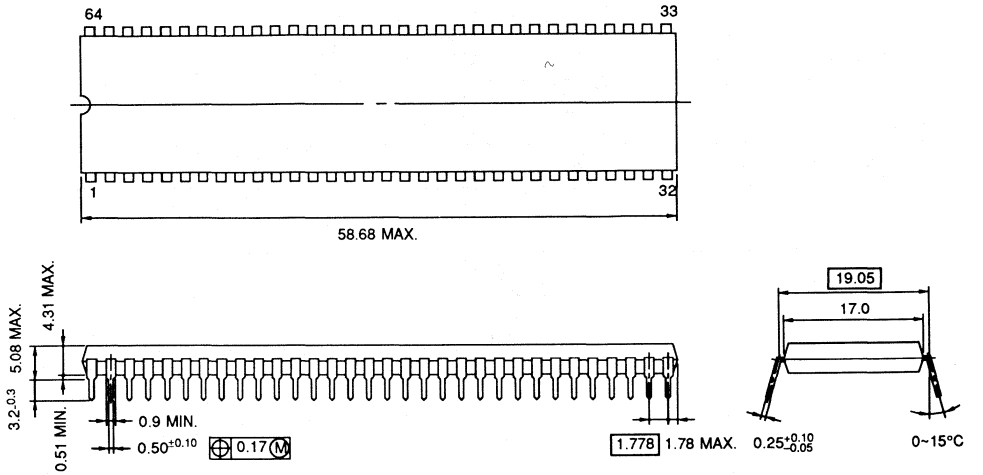


Serial Operation



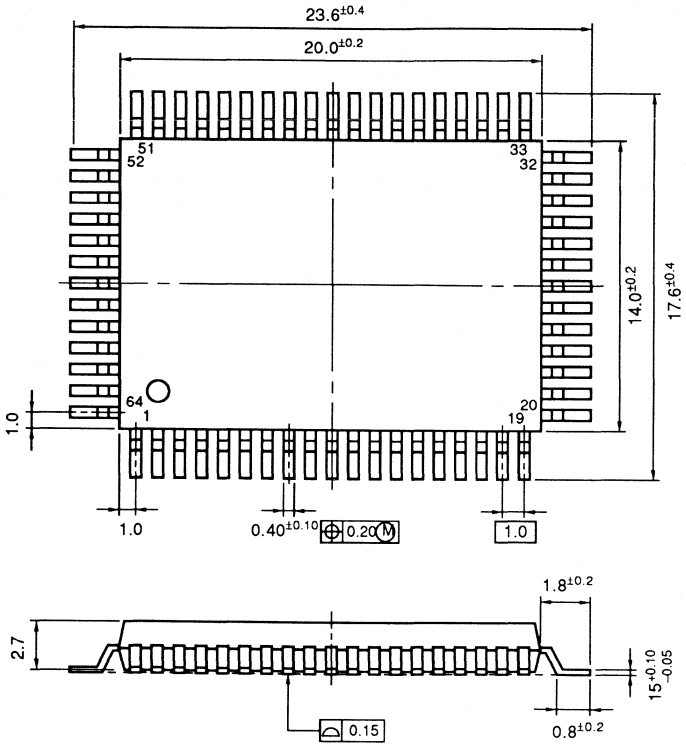
Package Dimensions (unit: mm)

64-Pin SDIP

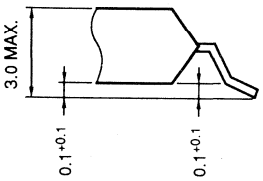


P64C-70-750A.C

64-Pin Flat Pack (QFP, 14 x 20)



Detail of Pin Shape



P64GF-100-3B8, 3BE

Description

The μPD78330/μPD78334 are high performance microcomputers designed for high end process control, such as automobile engine control and power train control. They are based on a 16-bit CPU (software compatible to 78320/322) with an 8-bit external data bus combined with a very powerful set of on-chip peripherals. They feature several 16/18-bit timers and counters, sequential and high speed PWM output functions, an 8-bit realtime output port plus an A/D converter, two serial interfaces and a huge number of I/O lines. For very efficient interrupt handling a three level program-controlled hardware priority interrupt controller is implemented. This interrupt controller supports three different methods of interrupt request handling including macro service and context switch. Designed in a 1.2μ CMOS process they can operate with a maximum oscillator frequency of 20 MHz. The μPD78330 is the ROMless version with 1K byte of on-chip RAM, the μPD78334 has the same RAM size plus 32K byte of mask programmed ROM. Both are supplied in 84-pin PLCC and a 94-pin plastic QFP package.

For development purpose, preproduction and applications with many different code versions an EPROM version will be available.

The μPD78330/334 have a special interface for a dedicated memory chip, the Turbo Access Manager (TAM). The TAM includes EPROM, RAM, I/O interfaces, and an instruction prefetch pointer that realizes instruction code fetches from external memory with same speed than this is fetched from on-chip ROM. This dedicated memory device allows for realtime execution with the ROMless Microcomputer plus TAM as well as ROM size expansion without speed penalty.

Features

- High end single chip microcomputer:
  - 16-bit CPU.
  - 8-bit external bus.
  - 32K bytes onchip ROM (μPD78334).
  - 1K bytes onchip RAM.
- Powerful instruction set:
  - Software compatible to 78320/322.
  - 16-bit arithmetic/logical instructions.
  - Multiply/divide (16 x 16 bits, 32 ÷ 16 bits).
  - Signed multiply instruction.
  - Bit manipulation instruction.
  - String instruction
- Minimum instruction time: 200nsec @20MHz input
- 3-byte instruction pre-fetch queue
- Powerful Real-time pulse unit:
  - One 18-bit free running timer.
  - Two 16-bit interval/free running timer.
  - One 16-bit interval timer
  - Six channel sequential PWM
  - Five timer outputs
  - Two channel high speed/high precision PWM output (39KHz @10MHz)
- Eight realtime output ports
- 10-bit A/D converter with 16 channels
- Two serial communication channels
- Watchdog timer
- Interface to Turbo Access Manager
- Standby function
- 84-pin PLCC/94-pin QFP packages

Ordering Information

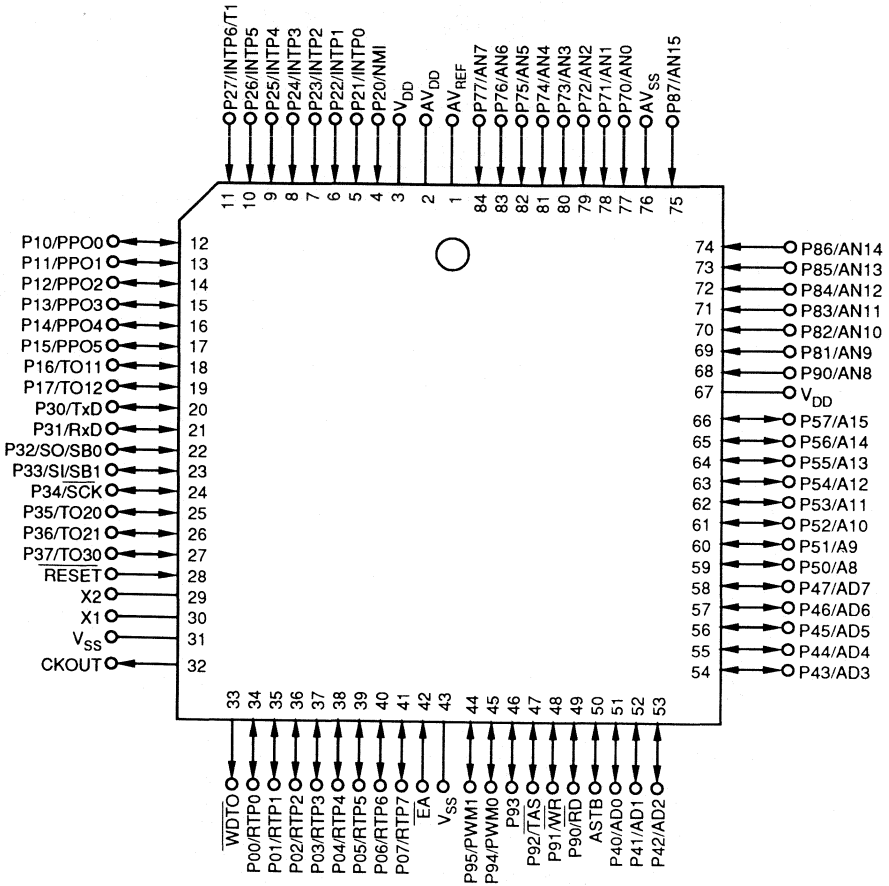
Part Number	Package Type	ROM
μPD78330L μPD78330GJ	84-pin PLCC 94-pin QFP	ROM less
μPD78334L μPD78334GJ	84-pin PLCC 94-pin QFP	32k ROM
μPD78P334L μPD78P334GJ	84-pin PLCC 94-pin QFP	32 OTPROM

Function table

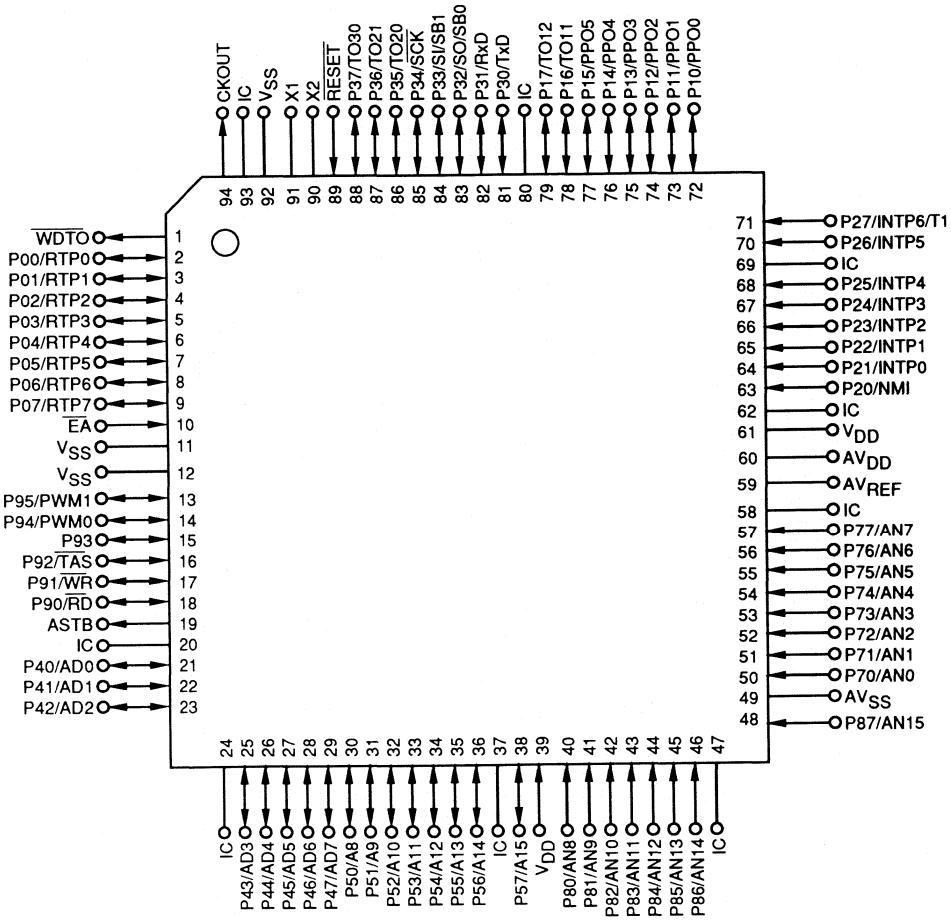
Function	Description
Number of basic instructions	109
Minimum instruction execution time	0.25 μs (internal clock frequency: 8 MHz)
Built-in memory	• ROM: 32K bytes • RAM: 1K bytes
Memory space	64K bytes (can externally be extended)
General-purpose register	8 bits x 16 x 8 banks
Instruction set	• 16-bit transfer or arithmetic/logical instruction • Unsigned multiply/divide instruction (16 bits x 16 bits, 32 bits + 16 bits) • Bit manipulation instruction (transfer, Boolean operation, set, reset, test) • Context switching instruction • String instruction
Real-time pulse unit	• 18/16-bit timer/counter: 1 18/16-bit compare registers: 5 18/16-bit capture registers: 3 18/16-bit capture/compare registers: 2 Pulse outputs: 6 • 16-bit timers/counters: 3 16-bit compare registers: 5 16-bit capture register: 1 Timer outputs: 5
Real-time output port	• Pulse outputs synchronized with RPU: 8
A/D converter	10-bit resolution: 16 channels
Interrupt function	• A 3-level priority can be specified by software. • One interrupt processing mode can be selected out of three types: vector interrupt function, macro service function, and context switching function.
I/O line	Input ports: 24 (16 ports for analog input) Output ports: 38
Serial interface	• With a dedicated baud rate generator • UART: 1 • Clock synchronous serial interface/SBI: 1
Package	• 84-pin PLCC • 94-pin plastic QFP
Others	• Control signal output function for the turbo access manager • Watchdog timer function • Standby function (HALT/STOP)

Pin configuration

a) 84-pin PLCC

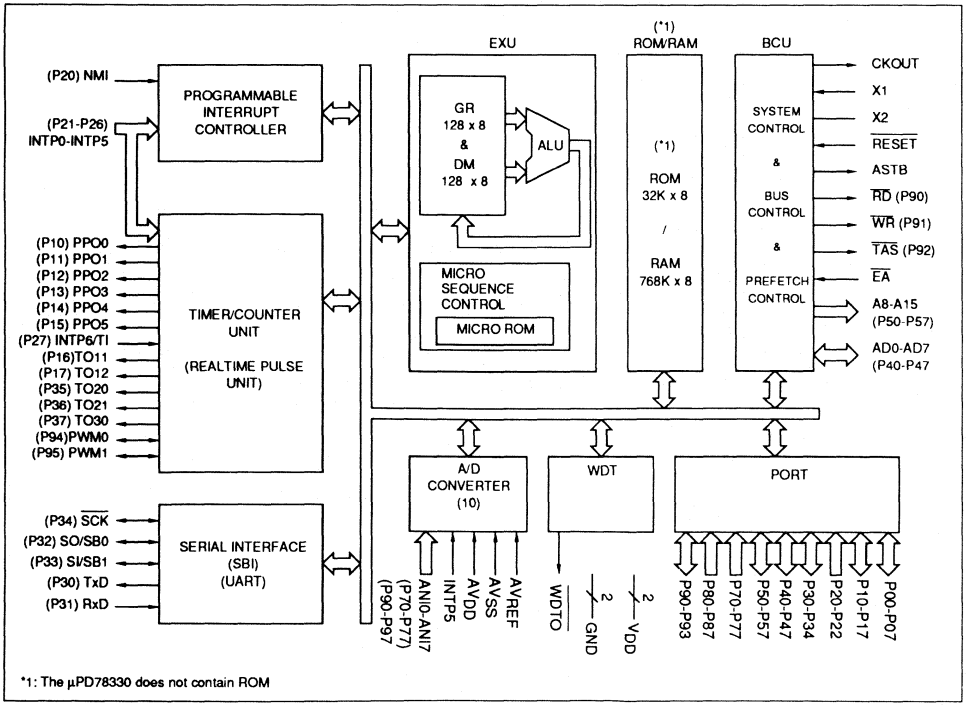


b) 94-pinplastic QFP



P00-P07:	Port 0
P10-P17:	Port 1
P20-P27:	Port 2
P30-P37:	Port 3
P40-P47:	Port 4
P50-P57:	Port 5
P70-P77:	Port 7
P80-P87:	Port 8
P90-P95:	Port 9
AD0-AD7:	Addresses 0 to 7 or data items 0 to 7
A8-A15:	Addresses 8 to 15
AN0-AN15:	Analog inputs 0 to 15
TI:	Timer input
TO11-TO30:	Timer outputs 11 to 30
CKOUT:	Clock output
PWM0-PWM1:	Pulse width modulation outputs 0 and 1
INTP0-INTP6:	Interrupt from peripherals 0 to 6
RTP0-RTP7:	Real-time ports 0 to 7
PPO0-PPO5:	Programmable pulse outputs 0 to 5
NMI:	Nonmaskable interrupt

T x D:	Transmit data
R x D:	Receive data
SI:	Serial input
SO:	Serial output
SB0-SB1:	Serial buses 0 and 1
RD:	Read strobe
WR:	Write strobe
ASTB:	Address strobe
EA:	External access
RESET:	reset
SCK:	Serial clock
TAS:	Turbo access output
X1-X2:	Crystal 1 or 2
WDTO:	Watchdog timer output
AV_{DD}:	Analog V_{DD}
AV_{REF}:	Analog reference voltage
AV_{SS}:	Analog V_{SS}
V_{DD}:	Power supply
V_{SS}:	Ground



*1: The μPD78330 does not contain ROM

Pin Functions

Ports

Pin name	I/O	Dual-function pin	Function
P00-P07	I/O	RTP0-RTP7	Port 0 8-bit I/O port. Can be specified as input and output bit by bit. These pins also function as a real-time output port.
P10-P15	I/O	PPO0-PPO5	Port 1 8-bit I/O port. Can be specified as input and output bit by bit. These pins also function as a timer output pins of the real-time pulse unit.
P16		TO11	
P17		TO12	
P20	I	NM1	Port 2 8-bit input dedicated port.
P21		INTP0	
P22		INTP1	
P23		INTP2	
P24		INTP3	
P25		INTP4	
P26		INTP5	
P27		INTP6/TI	
P30	I/O	TxD	Port 3 8-bit I/O port. Can be specified as input and output bit by bit. These pins also function as a serial interface pin or a timer output pin of the real-time pulse unit.
P31		RxD	
P32		SO/SB0	
P33		SI/SB1	
P34		$\overline{SCK}$	
P35		TO20	
P36		TO21	
P37		TO30	
P40-P47	I/O	AD0-AD7	Port 4 8-bit I/O port. Can be specified as input and output in 8-bit units.
P50-P57	I/O	A8-A15	Port 5 8-bit I/O port. Can be specified as input and output bit by bit.
P70-P77	I	AN0-AN7	Port 7 8-bit input dedicated port. These pins also function as a analog input pin.
P80-P87	I	AN8-AN15	Port 8 8-bit input dedicated port. These pins also function as a analoginput pin.
P90	I/O	$\overline{RD}$	Port 9 6-bit I/O port. Can be specified as input and output bit by bit.
P91		$\overline{WR}$	
P92		$\overline{TAS}$	
P93			
P94		PWM0	
P95		PWM1	

Other than Ports

Pin name	I/O	Dual-function pin	Function
RTP0-RTP7	O	P00-P07	Synchronized with a trigger signal sent from the real-time pulse unit (RPU) and output a pulse in real time.
PPO0-PPO5	O	P10-P15	Programmable pulse output from RPU.
TO11	O	P16	Timer output from the RPU.
TO12		P17	
NMI	I	P20	Nonmaskable interrupt request input.
INTP0-INTP5	I	P21-P26	External interrupt input pins.
INTP6		P27/TI	
TI	I	P27/INTP6	External count input to timer 1 (TM1).
TxD	O	P30	Serial data output of the asynchronous serial interface (UART).
RxD	I	P31	Serial data input of the UART.
SO	O	P32/SB0	Serial data output in the 3-wire mode of the clock synchronous serial interface.
SI	I	P33/SB1	Serial data input in the 3-wire mode of the clock synchronous serial interface.
SB0	I/O	P32/SO	Serial data I/O in the serial bus mode of the clock synchronous serial interface.
SB1		P33/SI	
SCK	I/O	P34	Serial clock I/O of the clock synchronous serial interface.
TO20	O	P35	Timer output from the RPU.
TO21		P36	
TO30		P37	
AD0-AD7	I/O	P40-P47	Multiplexed address/data bus when an external memory is expanded.
A8-A15	O	P50-P57	Address bus when an external memory is expanded.
AN0-AN7	I	P70-P77	Analog input to the A/D converter.
AN8-AN15		P80-P87	
$\overline{RD}$	O	P90	Read strobe signal output to the external device.
$\overline{WR}$		P91	Write strobe signal output to the external device.
$\overline{TAS}$		P92	Control signal output to access the turbo access manager.
PWM0-PWM1	O	P94 and P95	PWM signal output.
CKOUT	O	—	System clock output for the interface with the turbo access manager.
$\overline{WDTO}$	O	—	Output of the signal indicating that a watchdog timer interrupt occured.
ASTB	O	—	Address strobe signal output.
$\overline{EA}$	I	—	Input of the control signal to select external memory access: For the μPD78334, the $\overline{EA}$ pin is normally connected to the V_{DD} pin. Connecting the $\overline{EA}$ pin to the V_{SS} pin enters the ROM-less mode, enabling access to external memory. For the μPD78330, this pin is connected to the V_{SS} pin. The level of the $\overline{EA}$ pin cannot be changed during operations.
AV_{REF}	I	—	A/D converter reference voltage input.
AV_{DD}	—	—	Analog power supply of the A/D converter.
AV_{SS}	—	—	Ground of the A/D converter.
$\overline{RESET}$	I	—	System reset input.
X1	I	—	Crystal input pin for system clock oscillation: A clock signal provided externally is input to the X1 pin.
X2	—	—	
V_{DD}	—	—	Positive power supply pin.
V_{SS}	—	—	Ground pin.

I/O Circuits

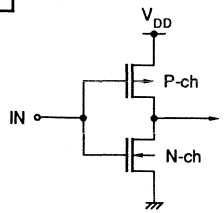
The type of I/O circuits of each pin is given in following table. The different types of I/O circuits are shown afterwards.

Input/Output Circuits of Each Pin

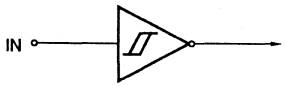
Pin	I/O circuit type
P00-P07	5
P10/PPO0-P15/PPO5	
P16/TO11, P17/TO12	
P20/NMI	2
P21/INTP0	
P22/INTP1	
P23/INTP2	
P24/INTP3	
P25/INTP4	
P26/INTP5	
P27/INTP6/TI	
P30/TxD	5
P31/RxD	
P32/SO/SB0	8
P33/SI/SB1	
P34/$\overline{\text{SCK}}$	
P35/TO20-P37/TO30	5
P40/AD0-P47/AD7	
P50/A8-P57/A15	
P70/AN0-P77/AN7	9
P80/AN8-P87/AN15	
P90/$\overline{\text{RD}}$	5
P91/$\overline{\text{WR}}$	
P92/$\overline{\text{TAS}}$	
P93	
P94/PWM0, P95/PWM1	
$\overline{\text{WDTO}}$	3
ASTB	4
CKOUT	3
$\overline{\text{EA}}$	1
$\overline{\text{RESET}}$	2

Input/Output Circuits of Each Pin

Type 1

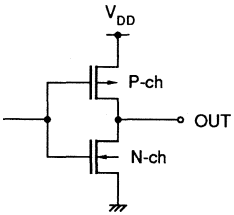


Type 2

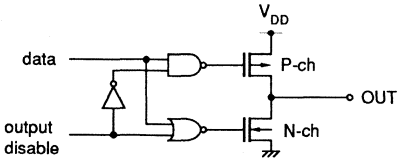


Schmitt trigger input with hysteresis characteristics.

Type 3

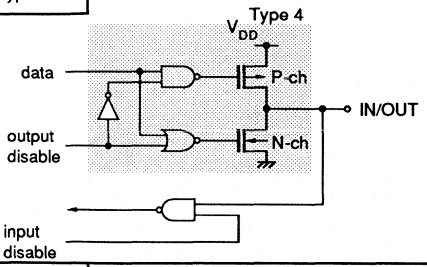


Type 4

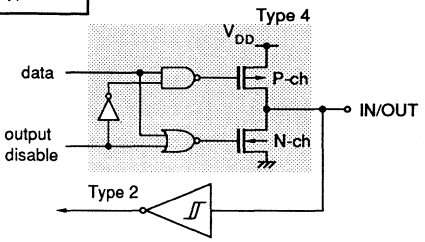


Push-pull output which can output high impedance (Both the positive and negative channels are off).

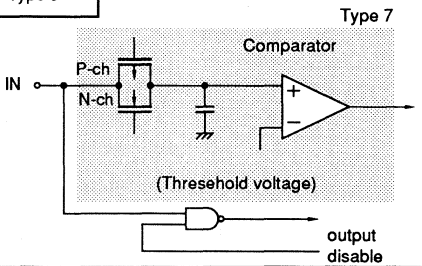
Type 5



Type 8



Type 9



Handling of unused pins

Pin	Recommended connection method
P00-P07	Input status: To be connected to the V_{SS} or V_{DD} pin via a pull-up resistor.
P10-P17	Output status: Open
P20-P27	To be connected to the V_{SS} pin.
P30-P37	Input status: To be connected to the V_{SS} or V_{DD} pin via a pull-up resistor.
P40-P47	Output status: Open
P50-P57	
P70-P77	To be connected to the V_{SS} pin.
P80-P87	
P90-P95	Input status: To be connected to the V_{SS} or V_{DD} pin via a pull-up resistor. Output status: Open
CKOUT	Open
$\overline{WDTO}$	
ASTB	
AV_{DD}	To be connected to the V_{DD} pin.
AV_{REF}	To be connected to the V_{SS} pin.
AV_{SS}	

Difference Between μPD78334/330 and μPd78322/320

Function \ Product		μPD78334	μPD78330	μPD78322	μPD78320
Number of basic instructions		109			
Minimum instruction execution time		250ns (when internal clock operates at 8 MHz or when external clock operates at 16 MHz)			
Internal memory	ROM	32768 x 8 bits	—	16384 x 8 bits	—
	RAM	1024 x 8 bits		640 x 8 bits	
Memory space		64K bytes			
I/O line	Input	24 (analog input: 16)		24 (analog input: 8)	
	Output	—			
	I/O	46	28	39	21
Real-time pulse unit		• 18/16-bit timer/counter: 1 18/16-bit compare register: 5 18/16-bit capture register: 3 18/16-bit capture/compare register: 2 • 16-bit timer/counter 3 16-bit compare register: 5 16-bit capture register: 1 • Timer output: 5 • Programmable pulse output: 6		• 18/16-bit free running timer: 1 • 16-bit timer/event counter: 1 • 16-bit compare register: 6 • 18-bit capture register: 4 • 18-bit capture/compare register: 2 • Real-time output port:	
Serial communication interface		• Dedicated baud rate generator : Provided • UART : 1 channel • SBI • Three-wire serial I/O : 1 channel			
A/D converter		10-bit resolution, 16 inputs		10-bit resolution, 8 inputs	
Interrupt		• External: 8, internal: 13 • 3-level programmable priority			
		• Three processing modes: Vectored interrupt function, context switching function, and macro service function			
Instruction set		Much more instructions are added as compared with the μPD78312 and μPD78310.			
Other specifications		• Watchdog timer: Provided • Standby function (STOP/HALT)			
		• Can directly be connected to the turbo access manager μPD71P302		• Can directly be connected to the turbo access manager μPD71P301	
Package		• 84-pin PLCC • 94-pin plastic QFP		• 68-pin PLCC • 74-pin plastic QFP	

2

Absolute Maximum Ratings
Ta = 25°C

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5 to +7.0	V
	AV_{DD}		-0.5 to V_{DD} +0.5	V
	AV_{SS}		-0.5 to +0.5	V
Input Voltage	V_I		-0.5 to V_{DD}+0.5	V
Output Voltage	V_0		-0.5 to V_{DD}+0.5	V
Output Current Low	I_{OL}	at 1 Pin	4.0	mA
		All Output Pin Total	90	mA
Output Current High	I_{OH}	at 1 Pin	-1.0	mA
		All Output Pin Total	-20	mA
Reference Voltage	AV_{REF}	f_{XX}≤16MHz	-0.5 to AV_{DD} ±0.3	V
Operating Temperature	T_{opt}		-10 to +70	°C
Storage Temperature	T_{stg}		-65 to +150	°C

Recommended Operating Conditions

OSC Frequency	Ta	V_{DD}
8 MHz < f_{XX} ≤ 16 MHz	-10 C to +70 C	+5.0V±10%

Capacitance (Ta=25°C,V_{DD}=V_{ss}=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f_C = 1MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins			20	pF
I/O Capacitance	C_{IO}	Returned to 0V			20	pF

DC Characteristics

Ta = -10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL}			0		0.8	V
Input High Voltage	V_{IH1}	*1		2.2			V
	V_{IH2}	*2		$0.8V_{DD}$			
Output Low Voltage	V_{OL}	I_{OL}=2.0mA				0.45	V
Output High Voltage	V_{OH}	I_{OH}=-400μA		V_{DD}-1.0			V
Input Leakage Current	I_{LI}	0V≤V_I≤V_{DD}				±10	μA
Output Leakage Current	I_{LO}	0V≤V_O≤V_{DD}				±10	μA
V_{DD} Supply Current	I_{DD1}	Operation Mode			40	65	mA
	I_{DD2}	Halt Mode			20	35	mA
AV_{DD} Supply Current	AI_{DD}				2.0	6.0	mA
Data Retention Voltage	V_{DDDR}	STOP Mode		2.5			V
Data Retention Current	I_{DDDR}	STOP Mode	V_{DDDR}=2.5V		2	10	μA
			V_{DDR}=5.0±10%		10	50	μA

Notes:

*1. All except $\overline{RESET}$, X1, X2, P20/NMI, P21/INTE0, P22/INTE1,P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{SCK}$

*2. $\overline{RESET}$, X!, X2, P20/NMI, P21/INTE0, P22/INTE1, P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{SCK}$

AC Characteristics

Read/Write Operation Ta = -10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Normal memory read/write operation (with general-purpose memory /turbo access manager connected).

Parameter	Symbol	Test Conditions	Min.	Max.	Units
System Clock Cycle Time	t_{CYK}		125	250	ns
Address Setup Time to ASTB↓	t_{SAST}		32		ns
Address Hold from ASTB↓	t_{HSTA}		32		ns
Address to $\overline{RD}$↓ Delay Time	t_{DAR}		85		ns
Address Float Time from $\overline{RD}$↓	t_{FRA}			0	ns
Address to Data Input	t_{DAID}			222	ns
$\overline{RD}$↓ to Data Input	t_{DRID1}			112	ns
ASTB↓ to $\overline{RD}$↓ Delay Time	t_{DSTR}		42		ns
Data Hold Time from $\overline{RD}$↑	t_{HRID}		0		ns
$\overline{RD}$↑ to Adress Delay Time	t_{DRA}		37		ns
$\overline{RD}$ Width Low	t_{WRL}		157		ns
ASTB Width High	t_{WSTH}		37		ns
Adress to $\overline{WR}$↓ Delay Time	t_{DAW}		85		ns
ASTB↓ to Data Output	t_{DSTOD}			102	ns
$\overline{WR}$↓ to Data Output	t_{DWOD}			40	ns
ASTB↓ to $\overline{WR}$↓ Delay Time	t_{DSTW}		42		ns
Data Setup to $\overline{WR}$↑	t_{SODW}		147		ns
Data Hold Time from $\overline{WR}$↑	t_{HWOD}		32		ns
$\overline{WR}$↑ to ASTB↑ Delay Time	t_{DWST}		42		ns
$\overline{WR}$ Width Low	t_{WWL}		157		ns

Serial Operation

Ta = -10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions		Min.	Max.	Units
$\overline{SCK}$ Cycle Time	t_{CYSK}	$\overline{SCK}$ Output	Note	1		μs
		$\overline{SCK}$ Input	External clock	1		μs
$\overline{SCK}$ Width Low	t_{WSKL}	$\overline{SCK}$ Output	Note	420		ns
		$\overline{SCK}$ Input	External clock	420		ns
$\overline{SCK}$ Width High	t_{WSKH}	$\overline{SCK}$ Output	Note	420		ns
		$\overline{SCK}$ Input	External clock	420		ns
SI Setup Time to $\overline{SCK}$ ↑	t_{SRXSK}			80		ns
SI Hold Time to $\overline{SCK}$ ↑	t_{HSKRX}			80		ns
SO Delay Time from $\overline{SCK}$ ↓	t_{DSKTX}				210	ns

Note: Internally divided by 8

2

A/D Converter Characteristics

Ta = -10°C to +70°C, V_{SS}=AV_{SS}=0V, 3.4V≤AV_{REF}≤AV_{DD}, V_{DD}=+5V±10%, V_{DD} - 0.5V ≤ AV_{DD} ≤ V_{DD}

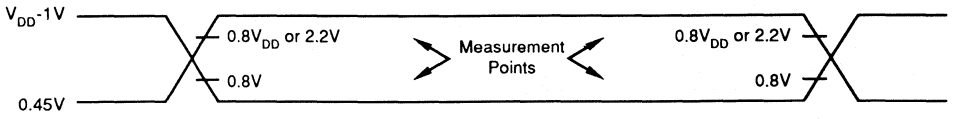
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Resolution			10			Bits
Relative Accuracy					±0.2%	FSR
Quatization Error					±1/2	LSB
Conversion Time	t_{CONV}	t_{CYK} ≥ 125ns	144			t_{CYK}
Sampling Time	t_{SAMP}	t_{CYK} ≥ 125ns	24			t_{CYK}
Zero Offset Error				±1.5		LSB
Gain Error				±1.5		LSB
Linearity Error				±1.5		LSB
Analog Input Voltage	V_{IAN}		0		VA_{REF}	V
AV_{REF} Current	AI_{REF}			1.0	3.0	mA
AV_{DD} supply Current	AI_{DD}			2.0	6.0	mA

Bus Timing Depending on Tcyk

Symbol	Calculation Expression	Min./Max.	Unit
t_{SAST}	0.5 T - 30	Min.	ns
t_{HSTA}	0.5 T - 30	Min.	ns
t_{DAR}	T - 40	Min.	ns
t_{DAID}	(2.5 + n) T - 90	Max.	ns
t_{DRID1}	(1.5 + n) T - 75	Max.	ns
t_{DSTR}	0.5 T - 20	Min.	ns
t_{DRA}	0.5 T - 25	Min.	ns
t_{WRL}	(1.5 + n) T - 30	Min.	ns
t_{WSTH}	0.5 T - 25	Min.	ns
t_{DAW}	T - 40	Min.	ns
t_{DSTOD}	0.5 T + 40	Max.	ns
t_{DSTW}	0.5 T - 20	Min.	ns
t_{SODWR}	1.5 T - 40	Min.	ns
t_{HWOD}	0.5 T - 30	Min.	ns
t_{DWST}	0.5 T - 20	Min.	ns
t_{WWL}	(1.5 + n) T - 30	Min.	ns

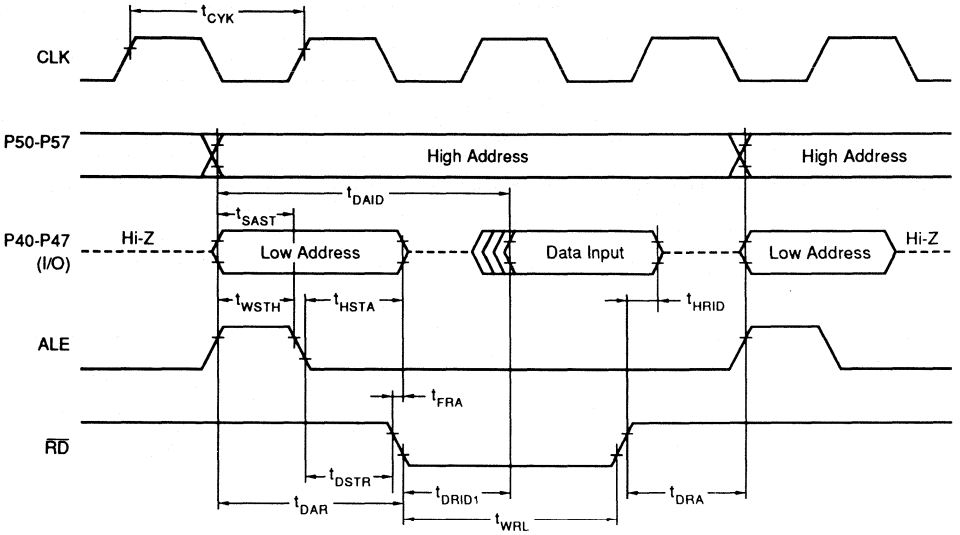
Note: t = T_{CYK} = 1/f_{CLK} (f_{CLK}: Internal System Clock)
n = number of wait cycles defined by user software
The parameters not included in the above list are not dependent on t_{CYK}.

AC Timing Measurement Points

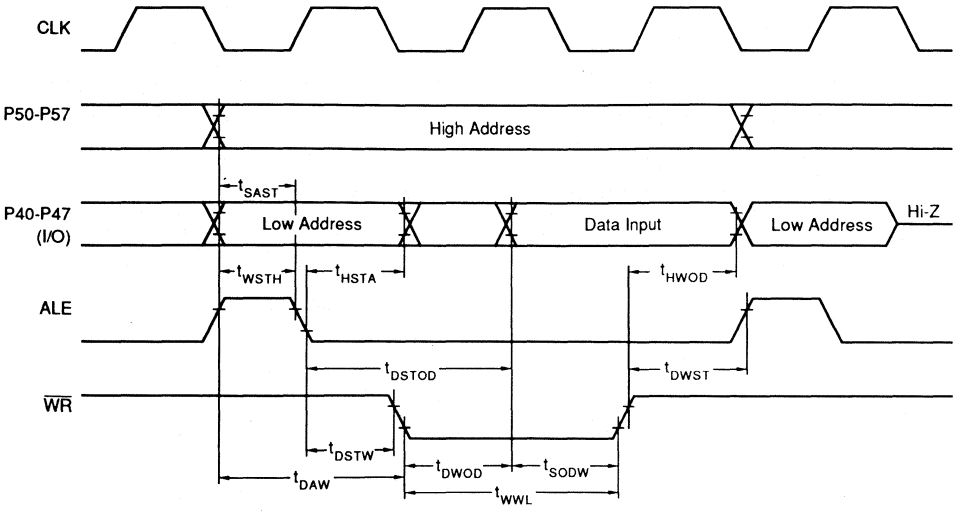


Timing Diagrams

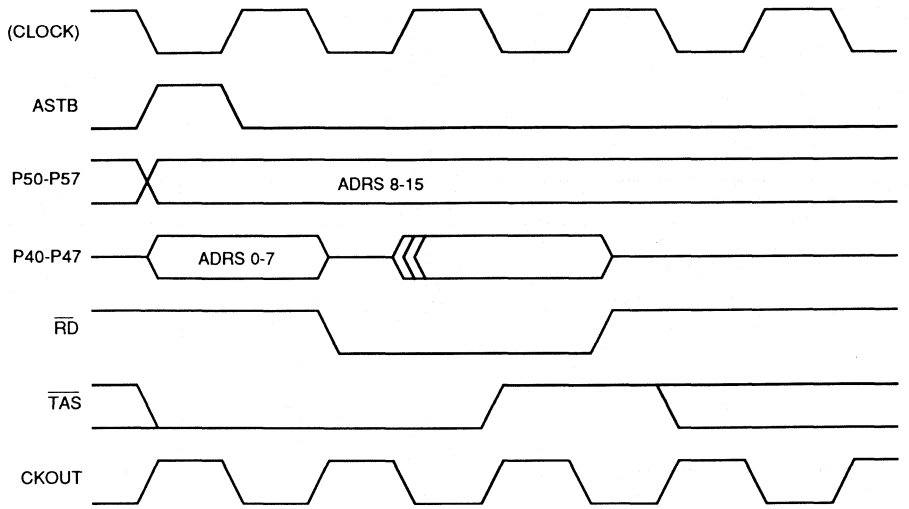
Read Operation



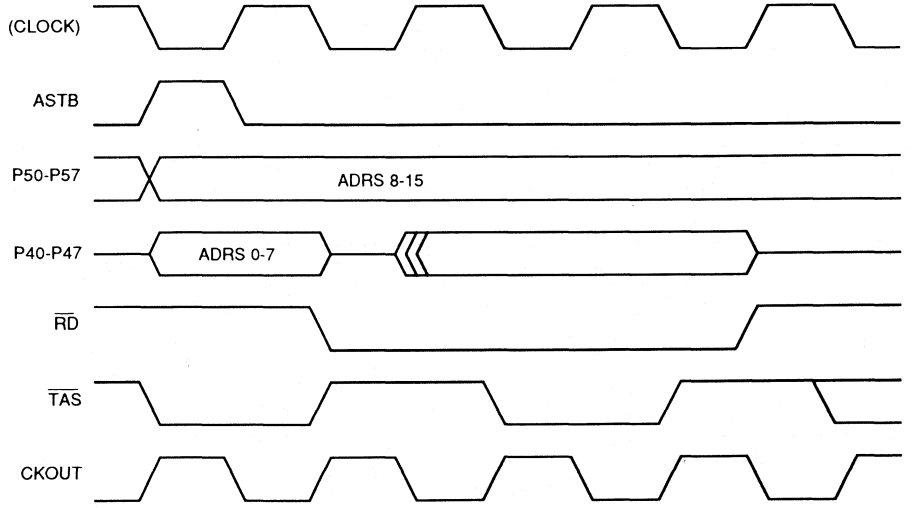
Write Operation



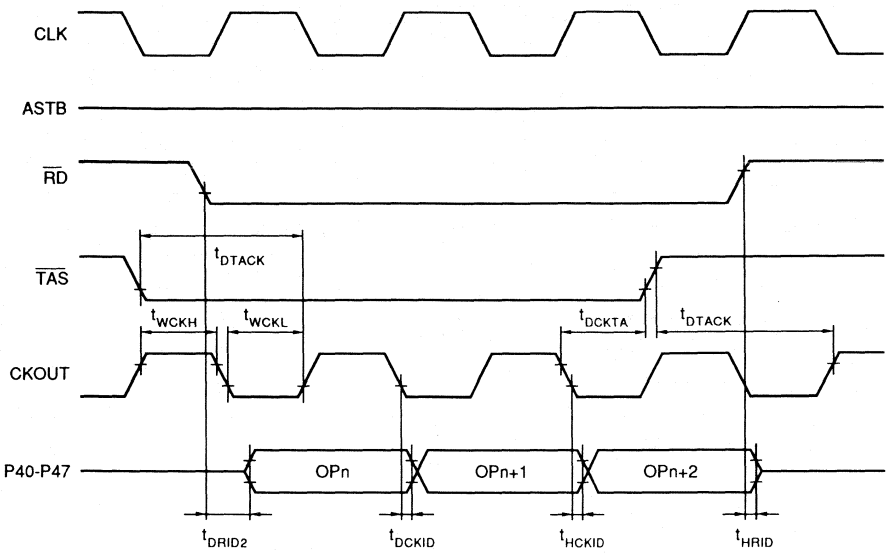
Normal Fetch Operation (No Wait)



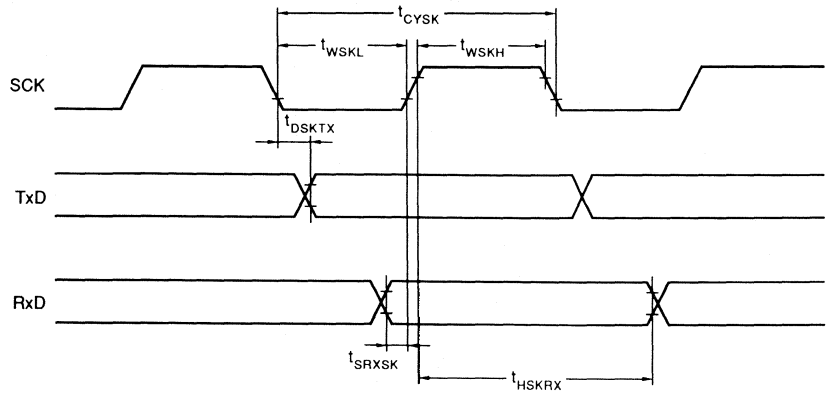
Normal Fetch Operation (1 Wait)



Turbo Fetch Operation



Serial Operation



Absolute Maximum Ratings
Ta = 25°C

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5 to +7.0	V
	AV_{DD}		-0.5 to V_{DD} +0.5	V
	AV_{SS}		-0.5 to +0.5	V
Input Voltage	V_I		-0.5 to V_{DD}+0.5	V
Output Voltage	V_O		-0.5 to V_{DD}+0.5	V
Output Current Low	I_{OL}	at 1 Pin	4.0	mA
		All Output Pin Total	90	mA
Output Current High	I_{OH}	at 1 Pin	-1.0	mA
		All Output Pin Total	-20	mA
Reference Voltage	AV_{REF}	$f_{XX} \leq$ 20 MHz	-0.5 to AV_{DD} ±0.3	V
Operating Temperature	T_{opt}		-10 to +70	°C
Storage Temperature	T_{stg}		-65 to +150	°C

Recommended Operating Conditions

OSC Frequency	Ta	V_{DD}
8 MHz < $f_{XX} \leq$ 20 MHz	-10 C to +70 C	+5.0V±5%

Capacitance (Ta=25°C,V_{DD}=V_{ss}=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f_C = 1MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins			20	pF
I/O Capacitance	C_{IO}	Returned to 0V			20	pF

DC Characteristics

Ta = -10°C to +70°C, V_{DD}=5.0V±5%, V_{ss}=0V

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL}			0		0.8	V
Input High Voltage	V_{IH1}	*1		2.2			V
	V_{IH2}	*2		$0.8V_{DD}$			
Output Low Voltage	V_{OL}	I_{OL}=2.0mA				0.45	V
Output High Voltage	V_{OH}	I_{OH}=-400μA		V_{DD}-1.0			V
Input Leakage Current	I_{LI}	$0V \le V_I \le V_{DD}$				±10	μA
Output Leakage Current	I_{LO}	$0V \le V_O \le V_{DD}$				±10	μA
V_{DD} Supply Current	I_{DD1}	Operation Mode			40	70	mA
	I_{DD2}	Halt Mode			20	40	mA
AV_{DD} Supply Current	AI_{DD}				2.0	6.0	mA
Data Retention Voltage	V_{DDDR}	STOP Mode		2.5			V
Data Retention Current	I_{DDDR}	STOP Mode	V_{DDDR}=2.5V		2	10	μA
			V_{DDR}=5.0±5%		10	50	μA

Notes:

*1. All except $\overline{RESET}$, X1, X2, P20/NMI, P21/INTE0, P22/INTE1,P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{SCK}$

*2. $\overline{RESET}$, X!, X2, P20/NMI, P21/INTE0, P22/INTE1, P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{SCK}$

2

AC Characteristics

Read/Write Operation Ta = -10°C to +70°C, V_{DD}=5.0V±5%, V_{ss}=0V

Normal memory read/write operation (with general-purpose memory /turbo access manager connected).

Parameter	Symbol	Test Conditions	Min.	Max.	Units
System Clock Cycle Time	t_{CYK}		100	250	ns
Address Setup Time to ASTB↓	t_{SAST}		20		ns
Address Hold from ASTB↓	t_{HSTA}		20		ns
Address to $\overline{RD}$↓ Delay Time	t_{DAR}		60		ns
Address Float Time from $\overline{RD}$↓	t_{FRA}			0	ns
Address to Data Input	t_{DAID}			160	ns
$\overline{RD}$↓ to Data Input	t_{DRID1}			75	ns
ASTB↓ to $\overline{RD}$↓ Delay Time	t_{DSTR}		30		ns
Data Hold Time from $\overline{RD}$↑	t_{HRID}		0		ns
$\overline{RD}$↑ to Adress Delay Time	t_{DRA}		25		ns
$\overline{RD}$ Width Low	t_{WRL}		120		ns
ASTB Width High	t_{WSTH}		25		ns
Adress to $\overline{WR}$↓ Delay Time	t_{DAW}		60		ns
ASTB↓ to Data Output	t_{DSTOD}			90	ns
$\overline{WR}$↓ to Data Output	t_{DWOD}			40	ns
ASTB↓ to $\overline{WR}$↓ Delay Time	t_{DSTW}		30		ns
Data Setup to $\overline{WR}$↑	t_{SODW}		110		ns
Data Hold Time from $\overline{WR}$↑	t_{HWOD}		20		ns
$\overline{WR}$↑ to ASTB↑ Delay Time	t_{DWST}		30		ns
$\overline{WR}$ Width Low	t_{WWL}		120		ns

Serial Operation

Ta = -10°C to +70°C, V_{DD}=5.0V±5%, V_{ss}=0V

Parameter	Symbol	Test Conditions		Min.	Max.	Units
$\overline{SCK}$ Cycle Time	t_{CYSK}	$\overline{SCK}$ Output	Note	800		ns
		$\overline{SCK}$ Input	External clock	800		ns
$\overline{SCK}$ Width Low	t_{WSKL}	$\overline{SCK}$ Output	Note	320		ns
		$\overline{SCK}$ Input	External clock	320		ns
$\overline{SCK}$ Width High	t_{WSKH}	$\overline{SCK}$ Output	Note	320		ns
		$\overline{SCK}$ Input	External clock	320		ns
SI Setup Time to $\overline{SCK}$ ↑	t_{SRXSK}			80		ns
SI Hold Time to $\overline{SCK}$ ↑	t_{HSKRX}			80		ns
SO Delay Time from $\overline{SCK}$ ↓	t_{DSKTX}				210	ns

Note: Internally divided by 8

2

A/D Converter Characteristics

Ta = -10°C to +70°C, V_{SS}=AV_{SS}=0V, 3.4V≤AV_{REF}≤AV_{DD}, V_{DD}=+5V±5%, V_{DD} - 0.5V ≤ AV_{DD} ≤ V_{DD}

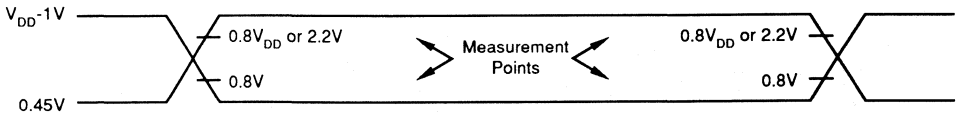
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Resolution			10			Bits
Relative Accuracy					±0.2%	FSR
Quatization Error					±1/2	LSB
Conversion Time	t_{CONV}	100 ≤ t_{CYK} < 125ns	192			t_{CYK}
		t_{CYK} ≥ 125ns	144			t_{CYK}
Sampling Time	t_{SAMP}	100 ≤ t_{CYK} < 125ns	40			t_{CYK}
		t_{CYK} ≥ 125ns	24			t_{CYK}
Zero Offset Error				±1.5		LSB
Gain Error				±1.5		LSB
Linearity Error				±2.0		LSB
Analog Input Voltage	V_{IAN}		0		VA_{REF}	V
AV_{REF} Current	AI_{REF}			1.0	3.0	mA
AV_{DD} supply Current	AI_{DD}			2.0	6.0	mA

Bus Timing Depending on Tcyk

Symbol	Calculation Expression	Min./Max.	Unit
t_{SAST}	0.5 T - 30	Min.	ns
t_{HSTA}	0.5 T - 30	Min.	ns
t_{DAR}	T - 40	Min.	ns
t_{DAID}	(2.5 + n) T - 90	Max.	ns
t_{DRID1}	(1.5 + n) T - 75	Max.	ns
t_{DSTR}	0.5 T - 20	Min.	ns
t_{DRA}	0.5 T - 25	Min.	ns
t_{WRL}	(1.5 + n) T - 30	Min.	ns
t_{WSTH}	0.5 T - 25	Min.	ns
t_{DAW}	T - 40	Min.	ns
t_{DSTOD}	0.5 T + 40	Max.	ns
t_{DSTW}	0.5 T - 20	Min.	ns
t_{SODWR}	1.5 T - 40	Min.	ns
t_{HWOD}	0.5 T - 30	Min.	ns
t_{DWST}	0.5 T - 20	Min.	ns
t_{WWL}	(1.5 + n) T - 30	Min.	ns

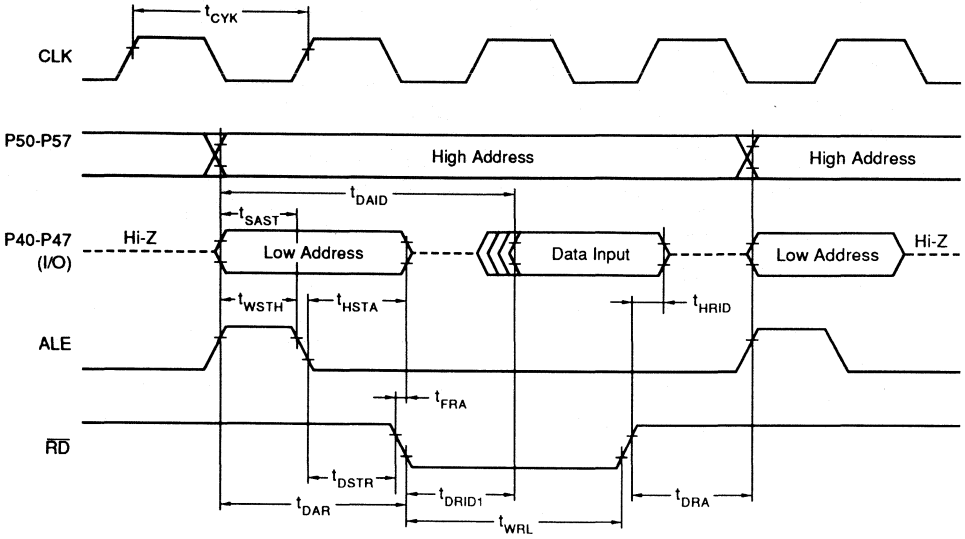
Note: t = T_{CYK} = $1/f_{CLK}$ (f_{CLK}: Internal System Clock)
n = number of wait cycles defined by user software
The parameters not included in the above list are not dependent on t_{CYK}.

AC Timing Measurement Points

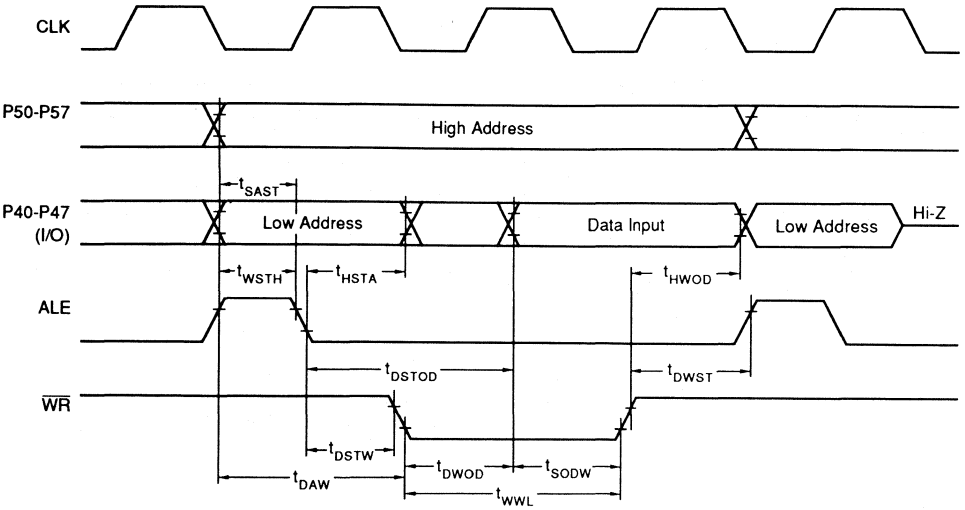


Timing Diagrams

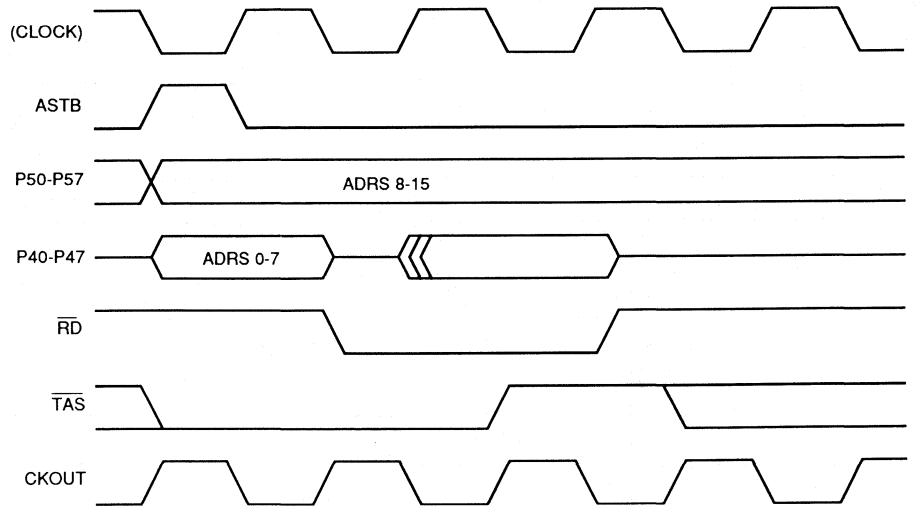
Read Operation



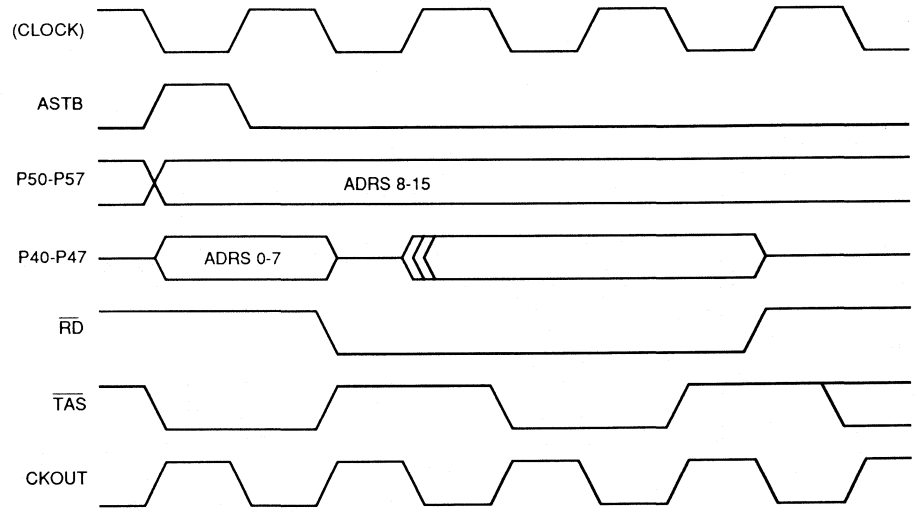
Write Operation



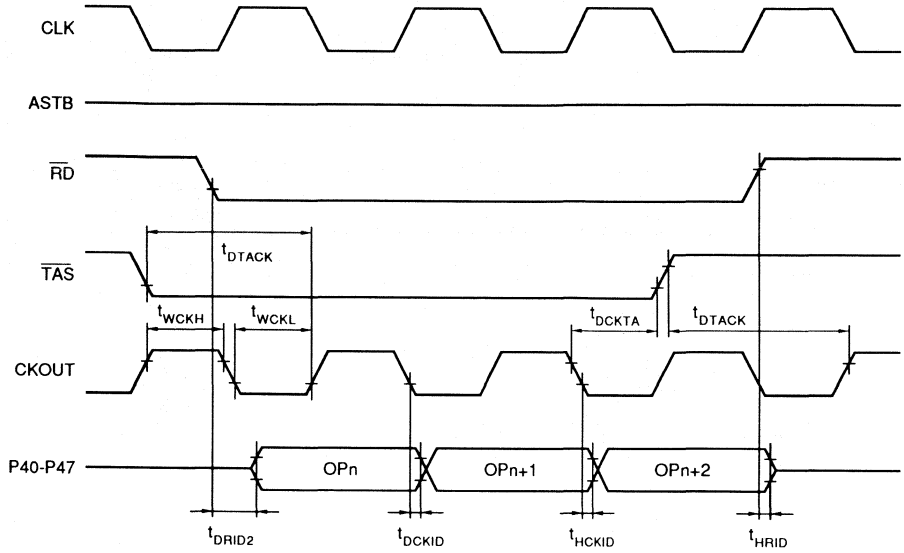
Normal Fetch Operation (No Wait)



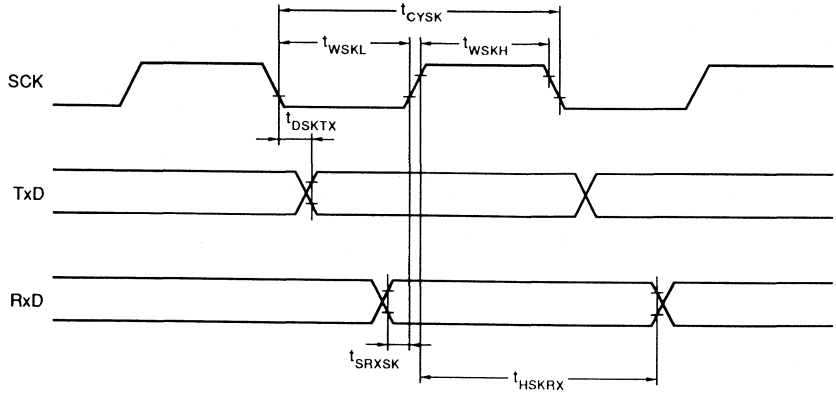
Normal Fetch Operation (1 Wait)



Turbo Fetch Operation



Serial Operation



Automotive -A- Grade

Absolute Maximum Ratings
Ta = 25°C

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5 to +7.0	V
	AV_{DD}		-0.5 to V_{DD} +0.5	V
	AV_{SS}		-0.5 to +0.5	V
Input Voltage	V_I		-0.5 to V_{DD}+0.5	V
Output Voltage	V_O		-0.5 to V_{DD}+0.5	V
Output Current Low	I_{OL}	at 1 Pin	4.0	mA
		All Output Pin Total	90	mA
Output Current High	I_{OH}	at 1 Pin	-1.0	mA
		All Output Pin Total	-20	mA
Reference Voltage	AV_{REF}	f_{XX}≤16MHz	-0.5 to AV_{DD} ±0.3	V
Operating Temperature	t_{opt}		-40 to +85	°C
Storage Temperature	t_{stg}		-65 to +150	°C

Recommended Operating Conditions

OSC Frequency	Ta	V_{DD}
8 MHz < f_{XX} ≤ 16 MHz	-40 C to +85 C	+5.0V+10%

Capacitance (Ta=25°C,V_{DD}=V_{ss}=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f_C = 1MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins			20	pF
I/O Capacitance	C_{IO}	Returned to 0V			20	pF

DC Characteristics

Ta = -40°C to +85°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL}			0		0.8	V
Input High Voltage	V_{IH1}	*1		2.2			V
	V_{IH2}	*2		$0.8V_{DD}$			
Output Low Voltage	V_{OL}	I_{OL}=2.0mA				0.45	V
Output High Voltage	V_{OH}	I_{OH}=-400μA		V_{DD}-1.0			V
Input Leakage Current	I_{LI}	0V≤V_I≤V_{DD}				±10	μA
Output Leakage Current	I_{LO}	0V≤V_O≤V_{DD}				±10	μA
V_{DD} Supply Current	I_{DD1}	Operation Mode			45	70	mA
	I_{DD2}	Halt Mode			25	40	mA
AV_{DD} Supply Current	AI_{DD}				2.0	6.0	mA
Data Retention Voltage	V_{DDDR}	STOP Mode		2.5			V
Data Retention Current	I_{DDDR}	STOP Mode	V_{DDDR}=2.5V		2	10	μA
			V_{DDR}=5.0±10%		10	50	μA

Notes:

*1. All except $\overline{\text{RESET}}$, X1, X2, P20/NMI, P21/INTE0, P22/INTE1,P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{\text{SCK}}$

*2. $\overline{\text{RESET}}$, X1, X2, P20/NMI, P21/INTE0, P22/INTE1, P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{\text{SCK}}$

AC Characteristics

Read/Write Operation Ta = -40°C to +85°C, V_{DD}=5.0V±10%, V_{ss}=0V

Normal memory read/write operation (with general-purpose memory /turbo access manager connected).

Parameter	Symbol	Test Conditions	Min.	Max.	Units
System Clock Cycle Time	t_{CYK}		125	250	ns
Address Setup Time to ASTB↓	t_{SAST}		32		ns
Address Hold from ASTB↓	t_{HSTA}		32		ns
Address to $\overline{RD}$↓ Delay Time	t_{DAR}		85		ns
Address Float Time from $\overline{RD}$↓	t_{FRA}			0	ns
Address to Data Input	t_{DAID}			222	ns
$\overline{RD}$↓ to Data Input	t_{DRID1}			112	ns
ASTB↓ to $\overline{RD}$↓ Delay Time	t_{DSTR}		42		ns
Data Hold Time from $\overline{RD}$↑	t_{HRID}		0		ns
$\overline{RD}$↑ to Adress Delay Time	t_{DRA}		37		ns
$\overline{RD}$ Width Low	t_{WRL}		157		ns
ASTB Width High	t_{WSTH}		37		ns
Adress to $\overline{WR}$↓ Delay Time	t_{DAW}		85		ns
ASTB↓ to Data Output	t_{DSTOD}			102	ns
$\overline{WR}$↓ to Data Output	t_{DWOD}			40	ns
ASTB↓ to $\overline{WR}$↓ Delay Time	t_{DSTW}		42		ns
Data Setup to $\overline{WR}$↑	t_{SODW}		147		ns
Data Hold Time from $\overline{WR}$↑	t_{HWOD}		32		ns
$\overline{WR}$↑ to ASTB↑ Delay Time	t_{DWST}		42		ns
$\overline{WR}$ Width Low	t_{WWL}		157		ns

Serial Operation

Ta = -40°C to +85°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions		Min.	Max.	Units
$\overline{SCK}$ Cycle Time	t_{CYSK}	$\overline{SCK}$ Output	Note	1		μs
		$\overline{SCK}$ Input	External clock	1		μs
$\overline{SCK}$ Width Low	t_{WSKL}	$\overline{SCK}$ Output	Note	420		ns
		$\overline{SCK}$ Input	External clock	420		ns
$\overline{SCK}$ Width High	t_{WSKH}	$\overline{SCK}$ Output	Note	420		ns
		$\overline{SCK}$ Input	External clock	420		ns
SI Setup Time to $\overline{SCK}$ ↑	t_{SRXSK}			80		ns
SI Hold Time to $\overline{SCK}$ ↑	t_{HSKRX}			80		ns
SO Delay Time from $\overline{SCK}$ ↓	t_{DSKTX}				210	ns

Note: Internally divided by 8

2

A/D Converter Characteristics

Ta = -40°C to +85°C, V_{SS}=AV_{SS}=0V, 3.4V≤AV_{REF}≤AV_{DD}, V_{DD}=+5V±10%, V_{DD} - 0.5V ≤ AV_{DD} ≤ V_{DD}

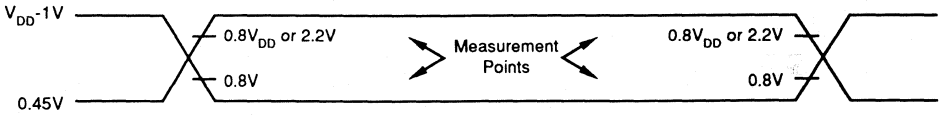
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Resolution			10			Bits
Relative Accuracy					±0.2%	FSR
Quatization Error					±1/2	LSB
Conversion Time	t_{CONV}	t_{CYK} ≥ 125ns	144			t_{CYK}
Sampling Time	t_{SAMP}	t_{CYK} ≥ 125ns	24			t_{CYK}
Zero Offset Error				±1.5		LSB
Gain Error				±1.5		LSB
Linearity Error				±1.5		LSB
Analog Input Voltage	V_{IAN}		0		VA_{REF}	V
AV_{REF} Current	AI_{REF}			1.0	3.0	mA
AV_{DD} supply Current	AI_{DD}			2.0	6.0	mA

Bus Timing Depending on Tcyk

Symbol	Calculation Expression	Min./Max.	Unit
t_{SAST}	0.5 T - 30	Min.	ns
t_{HSTA}	0.5 T - 30	Min.	ns
t_{DAR}	T - 40	Min.	ns
t_{DAID}	(2.5 + n) T - 90	Max.	ns
t_{DRID1}	(1.5 + n) T - 75	Max.	ns
t_{DSTR}	0.5 T - 20	Min.	ns
t_{DRA}	0.5 T - 25	Min.	ns
t_{WRL}	(1.5 + n) T - 30	Min.	ns
t_{WSTH}	0.5 T - 25	Min.	ns
t_{DAW}	T - 40	Min.	ns
t_{DSTOD}	0.5 T + 40	Max.	ns
t_{DSTW}	0.5 T - 20	Min.	ns
t_{SODWR}	1.5 T - 40	Min.	ns
t_{HWOD}	0.5 T - 30	Min.	ns
t_{DWST}	0.5 T - 20	Min.	ns
t_{WWL}	(1.5 + n) T - 30	Min.	ns

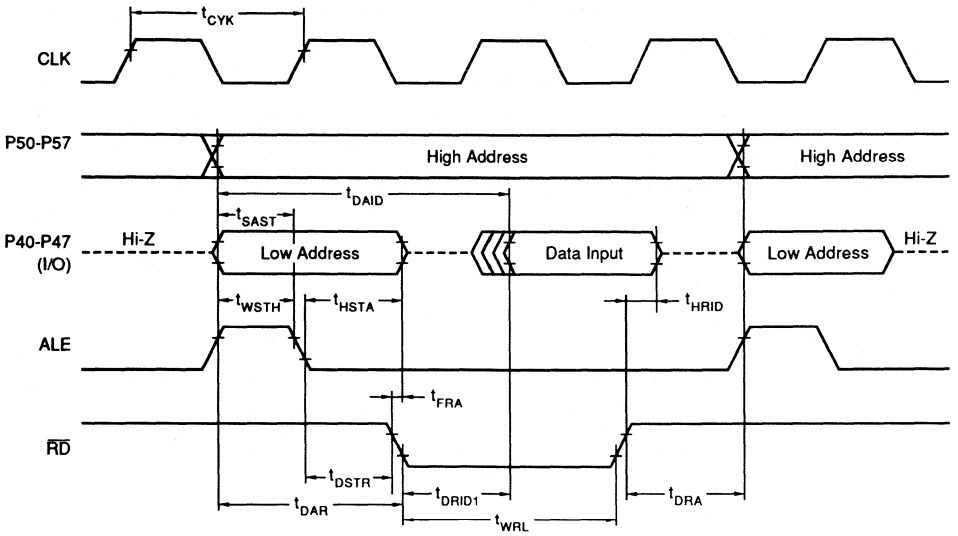
Note: t = T_{CYK} = $1/f_{CLK}$ (f_{CLK}: Internal System Clock)
n = number of wait cycles defined by user software
The parameters not included in the above list are not dependent on t_{CYK}.

AC Timing Measurement Points

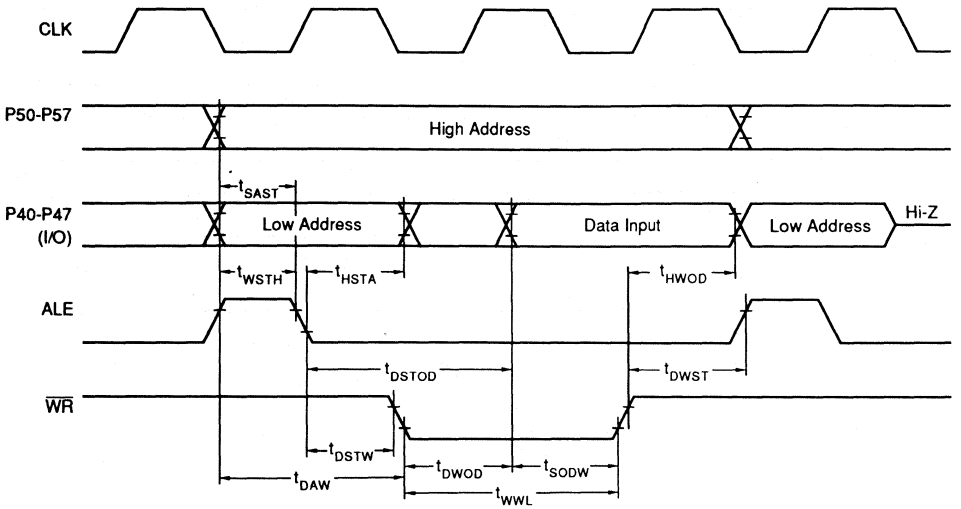


Timing Diagrams

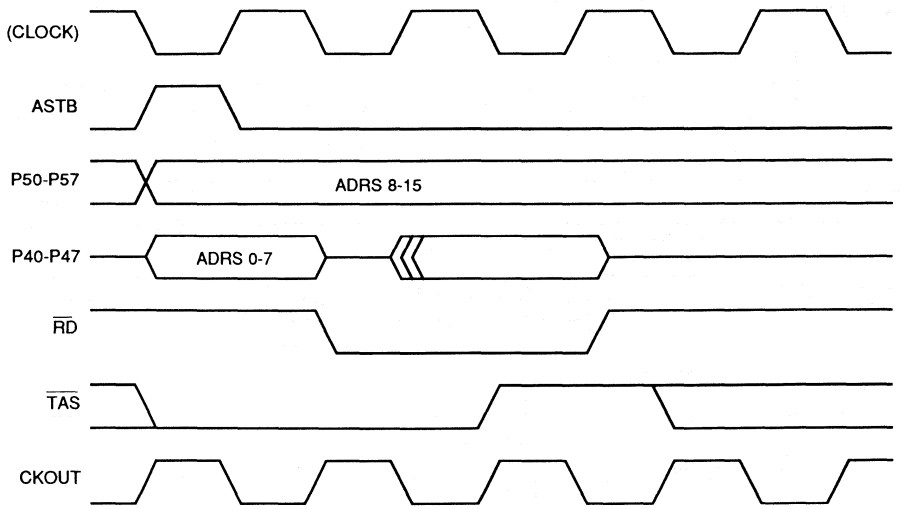
Read Operation



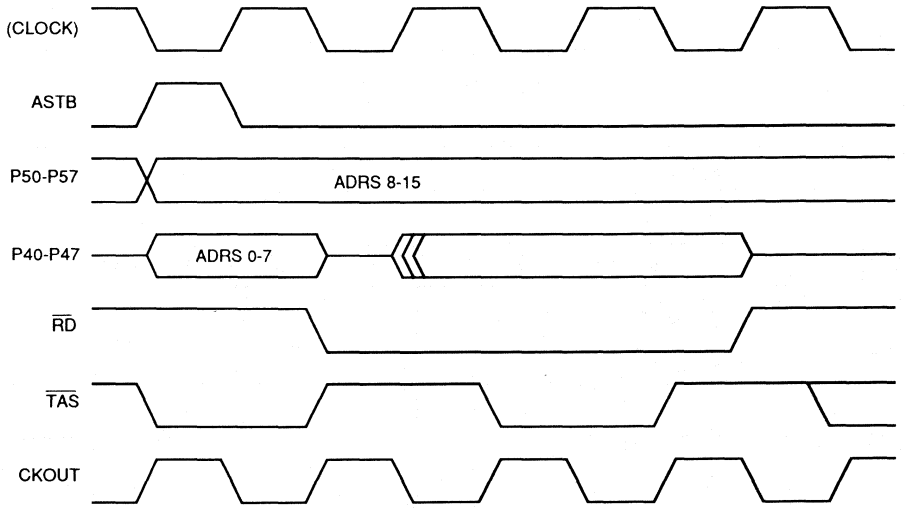
Write Operation



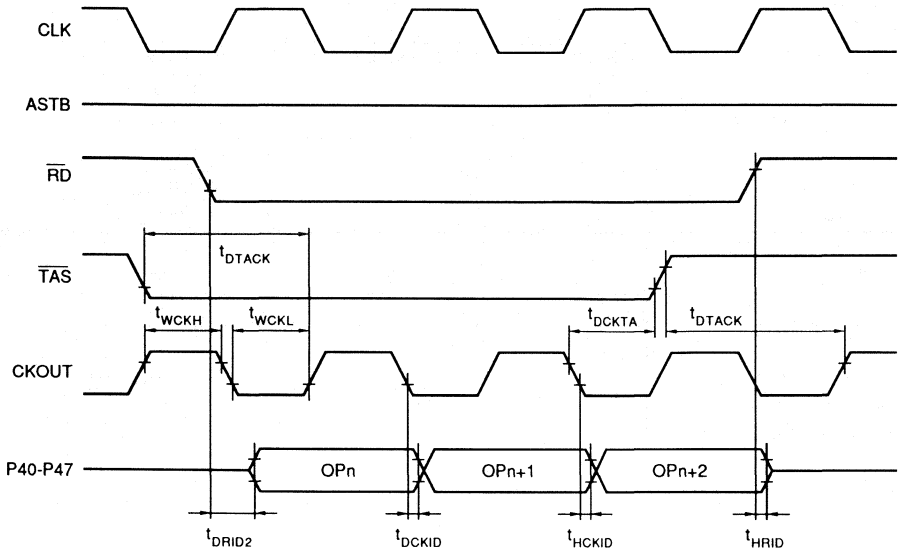
Normal Fetch Operation (No Wait)



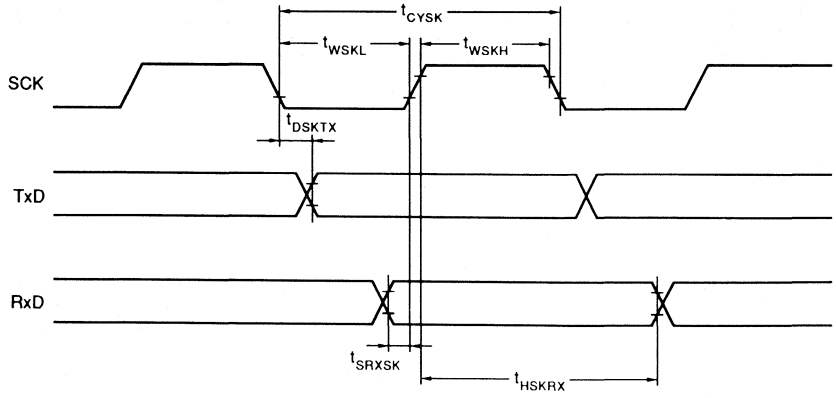
Normal Fetch Operation (1 Wait)



Turbo Fetch Operation



Serial Operation



Automotive -S- Grade

Absolute Maximum Ratings
Ta = 25°C

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5 to +7.0	V
	AV_{DD}		-0.5 to V_{DD} +0.5	V
	AV_{SS}		-0.5 to +0.5	V
Input Voltage	V_I		-0.5 to V_{DD}+0.5	V
Output Voltage	V_O		-0.5 to V_{DD}+0.5	V
Output Current Low	I_{OL}	at 1 Pin	4.0	mA
		All Output Pin Total	90	mA
Output Current High	I_{OH}	at 1 Pin	-1.0	mA
		All Output Pin Total	-20	mA
Reference Voltage	AV_{REF}		-0.5 to AV_{DD} ±0.3	V
Operating Temperature	T_{opt}	$f_{XTAL} \leq 12$ MHz	-40 to +110	°C
Storage Temperature	T_{stg}		-65 to +150	°C

Recommended Operating Conditions

OSC Frequency	Ta	V_{DD}
8 MHz < $f_{XX} \leq$ 12 MHz	-40°C to +110°C	+5.0V+10%

Capacitance ($Ta=25°C, V_{DD}=V_{SS}=0V$)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f_C = 1MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins			20	pF
I/O Capacitance	C_{IO}	Returned to 0V			20	pF

DC Characteristics

Ta = -40°C to +110°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL}			0		0.8	V
Input High Voltage	V_{IH1}	*1		2.2			V
	V_{IH2}	*2		$0.8V_{DD}$			
Output Low Voltage	V_{OL}	I_{OL}=2.0mA				0.45	V
Output High Voltage	V_{OH}	I_{OH}=-400μA		V_{DD}-1.0			V
Input Leakage Current	I_{LI}	$0V \le V_I \le V_{DD}$				±10	μA
Output Leakage Current	I_{LO}	$0V \le V_O \le V_{DD}$				±10	μA
V_{DD} Supply Current	I_{DD1}	Operation Mode			45	70	mA
	I_{DD2}	Halt Mode			25	40	mA
AV_{DD} Supply Current	AI_{DD}				2.0	6.0	mA
Data Retention Voltage	V_{DDDR}	STOP Mode		2.5			V
Data Retention Current	I_{DDDR}	STOP Mode	V_{DDDR}=2.5V		2	10	μA
			V_{DDR}=5.0±10%		10	50	μA

Notes:

*1. All except $\overline{RESET}$, X1, X2, P20/NMI, P21/INTE0, P22/INTE1,P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{SCK}$

*2. $\overline{RESET}$, X1, X2, P20/NMI, P21/INTE0, P22/INTE1, P23/INTE2, P24/INTE3, P25/INTE4, P26/INTE5, P27/INTE6/TI, P32/SB0/SO, P33/SB1/SI, P34/$\overline{SCK}$

AC Characteristics

Read/Write Operation Ta = -40°C to +110°C, V_{DD}=5.0V±10%, V_{ss}=0V

Normal memory read/write operation (with general-purpose memory /turbo access manager connected).

Parameter	Symbol	Test Conditions	Min.	Max.	Units
System Clock Cycle Time	t_{CYK}		166	250	ns
Address Setup Time to ASTB↓	t_{SAST}		43		ns
Address Hold from ASTB↓	t_{HSTA}		43		ns
Address to $\overline{RD}$↓ Delay Time	t_{DAR}		116		ns
Address Float Time from $\overline{RD}$↓	t_{FRA}			0	ns
Address to Data Input	t_{DAID}			315	ns
$\overline{RD}$↓ to Data Input	t_{DRID1}			164	ns
ASTB↓ to $\overline{RD}$↓ Delay Time	t_{DSTR}		53		ns
Data Hold Time from $\overline{RD}$↑	t_{HRID}		0		ns
$\overline{RD}$↑ to Adress Delay Time	t_{DRA}		48		ns
$\overline{RD}$ Width Low	t_{WRL}		209		ns
ASTB Width High	t_{WSTH}		48		ns
Adress to $\overline{WR}$↓ Delay Time	t_{DAW}		116		ns
ASTB↓ to Data Output	t_{DSTOD}			133	ns
$\overline{WR}$↓ to Data Output	t_{DWOD}			40	ns
ASTB↓ to $\overline{WR}$↓ Delay Time	t_{DSTW}		53		ns
Data Setup to $\overline{WR}$↑	t_{SODW}		209		ns
Data Hold Time from $\overline{WR}$↑	t_{HWOD}		43		ns
$\overline{WR}$↑ to ASTB↑ Delay Time	t_{DWST}		53		ns
$\overline{WR}$ Width Low	t_{WWL}		209		ns

Serial Operation

Ta = -40°C to +110°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions		Min.	Max.	Units
$\overline{SCK}$ Cycle Time	t_{CYSK}	$\overline{SCK}$ Output	Note	1.3		μs
		$\overline{SCK}$ Input	External clock	1.3		μs
$\overline{SCK}$ Width Low	t_{WSKL}	$\overline{SCK}$ Output	Note	580		ns
		$\overline{SCK}$ Input	External clock	580		ns
$\overline{SCK}$ Width High	t_{WSKH}	$\overline{SCK}$ Output	Note	580		ns
		$\overline{SCK}$ Input	External clock	580		ns
SI Setup Time to $\overline{SCK}$ ↑	t_{SRXSK}			80		ns
SI Hold Time to $\overline{SCK}$ ↑	t_{HSKRX}			80		ns
SO Delay Time from $\overline{SCK}$ ↓	t_{DSKTX}				210	ns

Note: Internally divided by 8

2

A/D Converter Characteristics

Ta = -40°C to +85°C, V_{SS}=AV_{SS}=0V, 3.4V≤AV_{REF}≤AV_{DD}, V_{DD}=+5V±10%, V_{DD} - 0.5V ≤ AV_{DD} ≤ V_{DD}

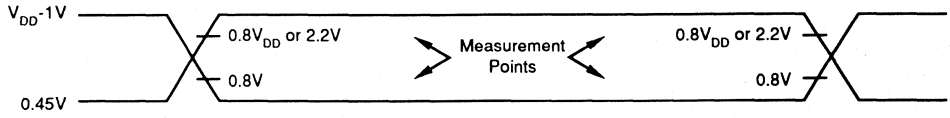
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Resolution			10			Bits
Relative Accuracy		-40°C ≤ T_C ≤ 75°C			±0.2%	FSR
		-40°C ≤ T_C ≤ 125°C			±0.4%	FSR
Quatization Error					±1/2	LSB
Conversion Time	t_{CONV}	t_{CYK} ≥ 166ns	144			t_{CYK}
Sampling Time	t_{SAMP}	t_{CYK} ≥ 166ns	24			t_{CYK}
Zero Offset Error				±1.5		LSB
Gain Error				±1.5		LSB
Linearity Error				±2.0		LSB
Analog Input Voltage	V_{IAN}		0		VA_{REF}	V
AV_{REF} Current	AI_{REF}			1.0	3.0	mA
AV_{DD} supply Current	AI_{DD}			2.0	6.0	mA

Bus Timing Depending on Tcyk

Symbol	Calculation Expression	Min./Max.	Unit
t_{SAST}	0.5 T - 45	Min.	ns
t_{HSTA}	0.5 T - 40	Min.	ns
t_{DAR}	T - 50	Min.	ns
t_{DAID}	(2.5 + n) T - 100	Max.	ns
t_{DRID1}	(1.5 + n) T - 85	Max.	ns
t_{DSTR}	0.5 T - 30	Min.	ns
t_{DRA}	0.5 T - 35	Min.	ns
t_{WRL}	(1.5 + n) T - 40	Min.	ns
t_{WSTH}	0.5 T - 35	Min.	ns
t_{DAW}	T - 50	Min.	ns
t_{DSTOD}	0.5 T + 50	Max.	ns
t_{DSTW}	0.5 T - 30	Min.	ns
t_{SODWR}	1.5 T - 50	Min.	ns
t_{HWOD}	0.5 T - 40	Min.	ns
t_{DWST}	0.5 T - 30	Min.	ns
t_{WWL}	(1.5 + n) T - 40	Min.	ns

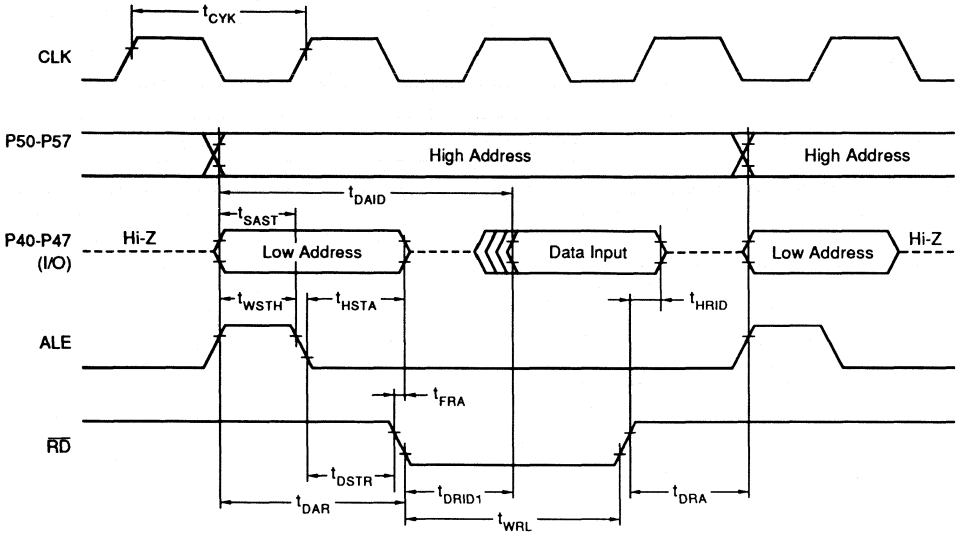
Note: t = T_{CYK} = $1/f_{CLK}$ (f_{CLK}: Internal System Clock)
n = number of wait cycles defined by user software
The parameters not included in the above list are not dependent on t_{CYK}.

AC Timing Measurement Points

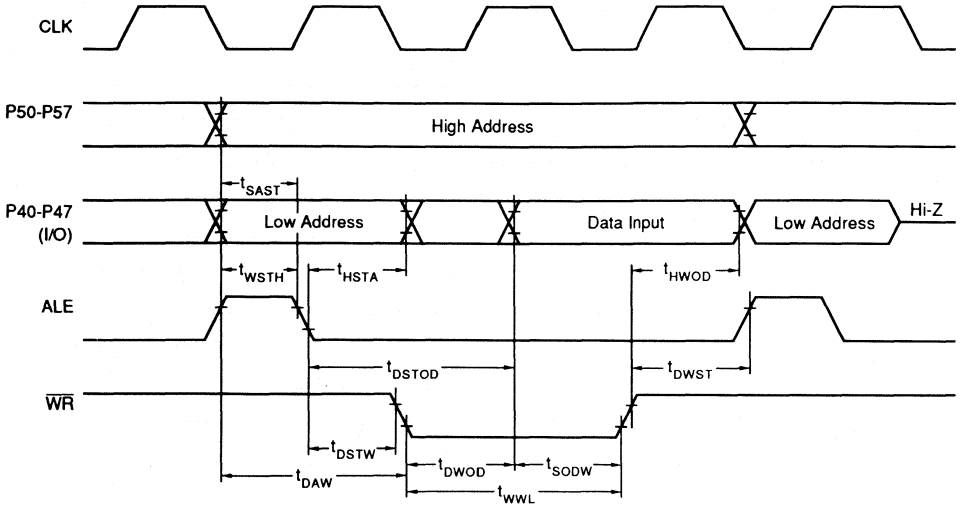


Timing Diagrams

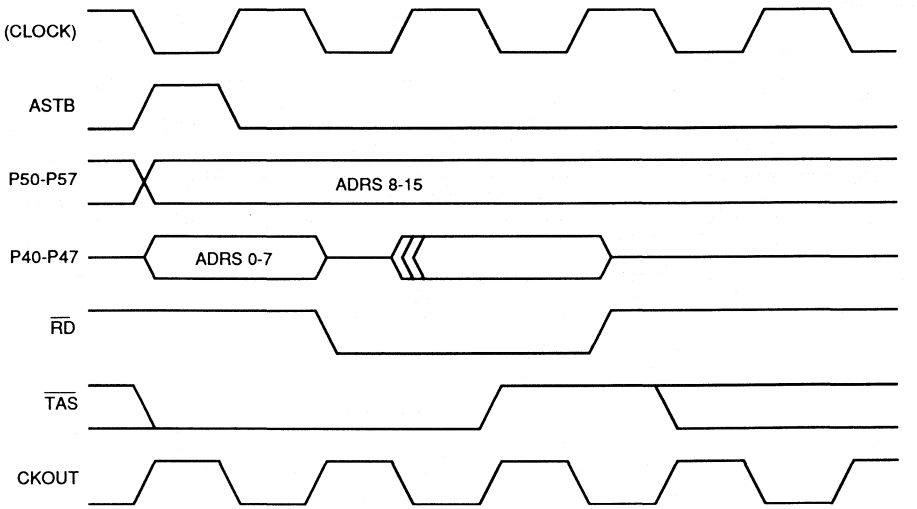
Read Operation



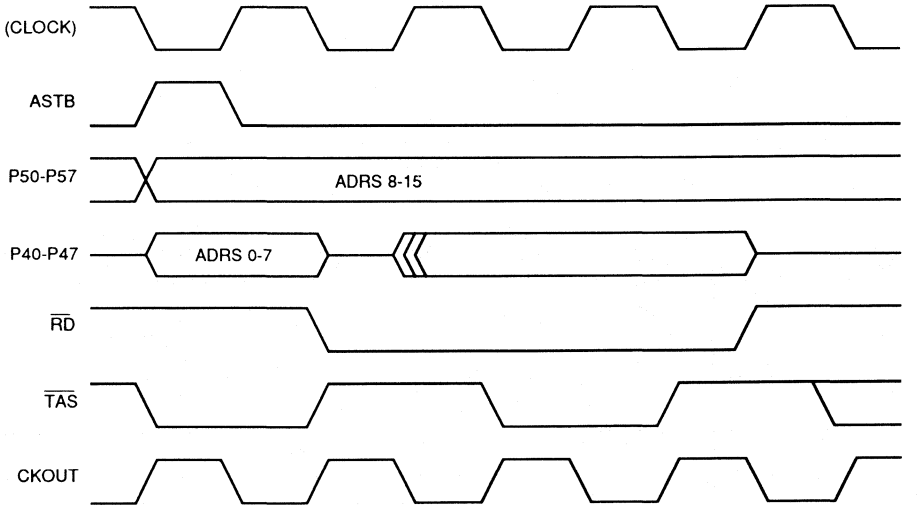
Write Operation



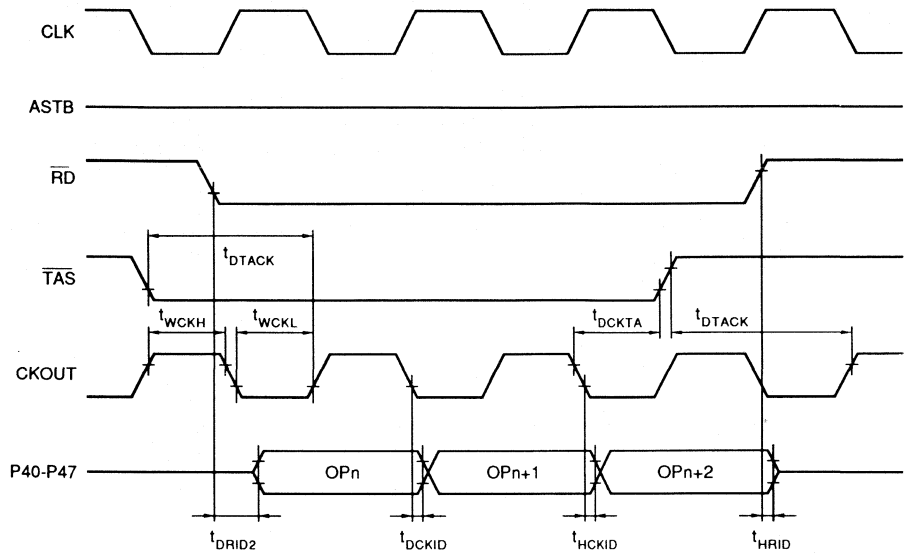
Normal Fetch Operation (No Wait)



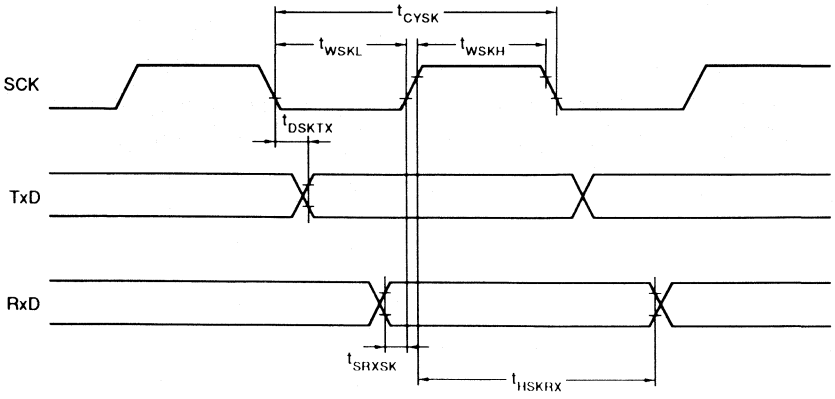
Normal Fetch Operation (1 Wait)



Turbo Fetch Operation

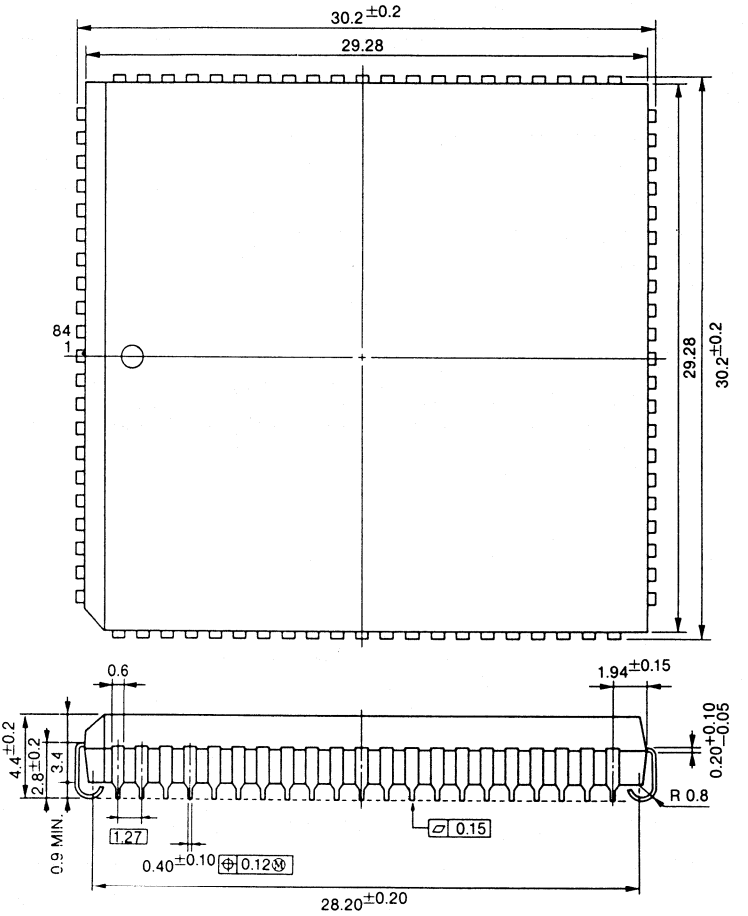


Serial Operation



Package Dimensions (unit: mm)

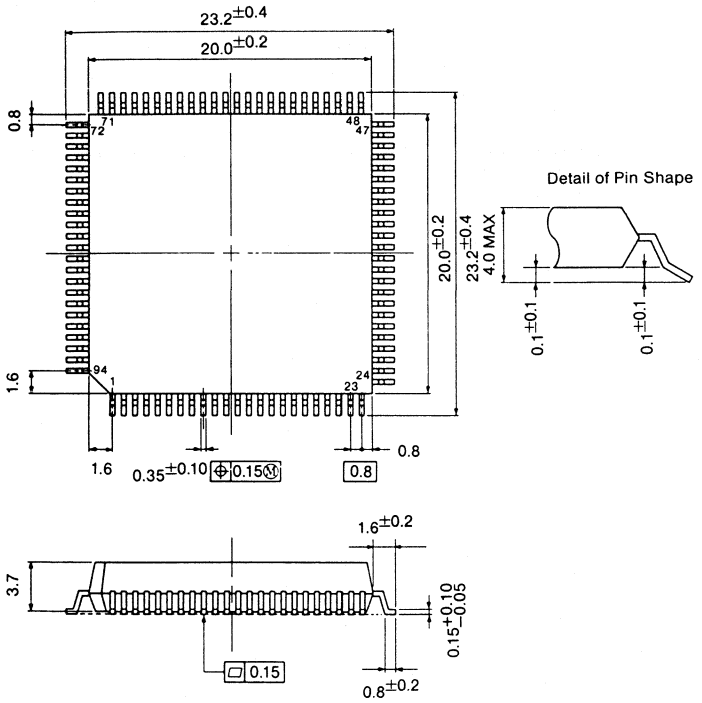
84-pin PLCC



P84L-50A3

Package Dimensions (unit: mm)

94-pin plastic Flat (QFP



Description

The μPD71P301 is a peripheral LSI device for microcomputer applications. It integrates a 16-Kbyte PROM, 1-Kbyte SRAM, 16 I/Os, plus memory access and bus interface functions etc. When used with μPD78320/322, μPD78323/324 or μPD78327/328 having a high speed memory accesssing function, the memory access controller of the μPD71P301 operates efficiently, so that instruction codes can be successively fetched from the PROM at amximum microcomputer speed. One word will be fetched per clock cycle without having the address supplied from the microcomputer. Due to this fast interface this device is called Turbo Access Manager (TAM1).

The μPD71P301 can also be directly connected as ROM and RAM expansion to other microcomputers or microprocessors equiped with an address data multiplex bus (i.e. μPD78310/312, μPD78C10/C11/C12/C14), of course without the special speed advantage. The 16 I/O lines are implemented to recover two ports which are required to connect μPD71P301 to a microcomputer. The μPD71P301 allows compact application systems to be configured.

Features

- Fast memory access function
  Opcode & data read speed: 1 word per clock cycle (max.)
- Directly connectable to address/data multiplex bus
- Internal memory space relocation function
  For 1-Mbyte/64-Kbyte memory
- External expanded address output function
- Chip Select signal output function (4 outputs)
- Cascadable for larger PROM size
- EPROM: 16 Kbytes
- SRAM: 1 Kbytes
- I/O Lines: 16
- CMOS

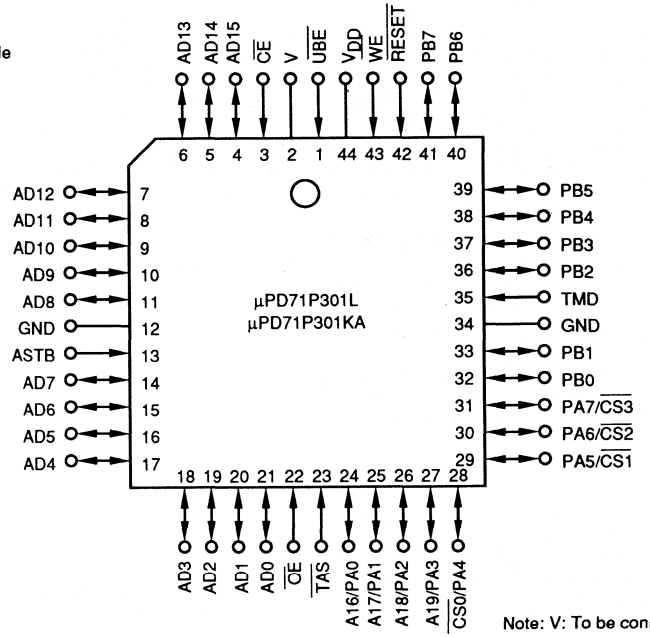
Ordering Information

Part Number	Package Type	ROM
μPD71P301KA	44-Pin LCC	UVPROM
μPD71P301KB	64-Pin LCC	
μPD71P301L	44-Pin PLCC	OTPROM
μPD71P301GF	64-Pin Flat	

2

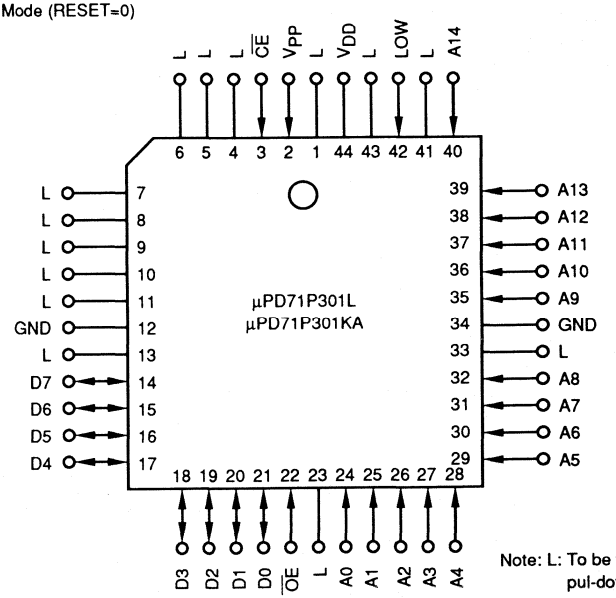
Pin Configuration

44-Pin LCC/PLCC
Normal Operating Mode



Note: V: To be connected to V_{DD}.

EPROM Programming Mode (RESET=0)



Note: L: To be fixed low with external pul-down resistor

Pin Identification

Symbol	Function
$\overline{UBE}$	Upper Byte Enable
$\overline{CE}$	Chip Enable
AD0 to AD15	Address/Data Bus
ASTB	Address Strobe
$\overline{OE}$	Output Enable
$\overline{TAS}$	Turbo Access Strobe

Symbol	Function
PA0 to PA7	Port A
PB0 to PB7	Port B
TMD	Turbo Mode
$\overline{RESET}$	Reset
$\overline{WE}$	Write Enable
A16 to A19	Address Bus

Pin Functions

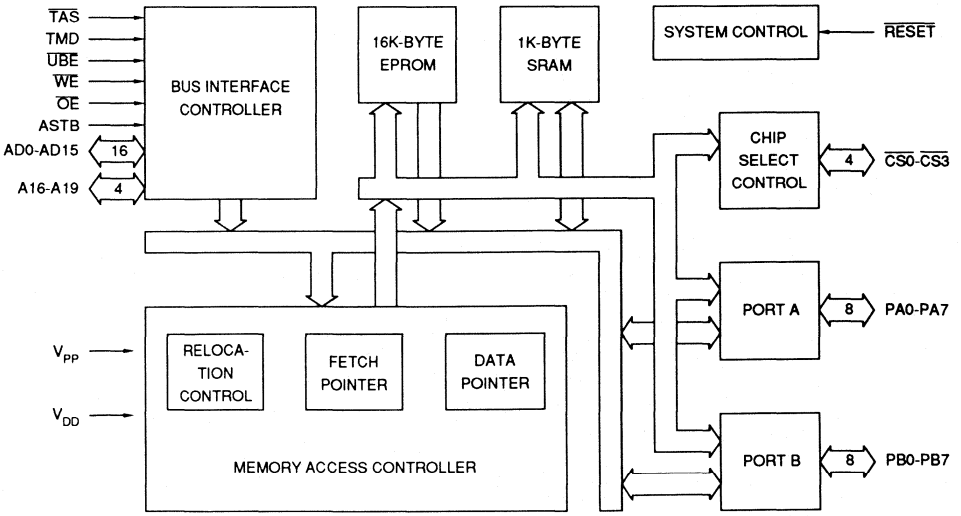
Normal Operating Mode

Pin Name	Input/ Output	Function	Dual Function Pins
PA0 to PA3	Input/ Output	8-bit input/output port I/O specifiable in byte units	A16 to A19
PA4 to PA7			$\overline{CS0}$ to $\overline{CS3}$
PB0 to PB7	Input/ Output	8-bit input/output port I/O specifiable in bit units	—
AD0 to AD15	Input/ Output	Address/data multiplex bus	—
A16 to A19	Input	Address input pins	PA0 to PA3
$\overline{RESET}$	Input	System Reset signal input pin	—
ASTB	Input	Input pin for timing which latches AD0 to AD15, TAS, and TMD.	—
TMD	Input	Input pin for control signal which specifies turbo access mode.	—
$\overline{TAS}$	Input	Input pin for control signal which specifies turbo access mode. Control of increment timing for turbo pointer and fetch pointer, and read/write timing.	—
$\overline{CE}$	Input	Chip Enable signal input pin	—
$\overline{OE}$	Input	Output Enable signal input pin	—
$\overline{WE}$	Input	Write Enable signal input pin	—
$\overline{UBE}$	Input	16-bit bus/8-bit bus selection signal input pin	—
$\overline{CS0}$ to $\overline{CS3}$	Output	Chip select outputs	PA4 to PA7
V_{DD}	—	Positive power supply pin	—
GND	—	Ground potential pin	—

PROM Programming Mode

Pin Name	Input/Output	Function
A0 to A14	Input	Address input pins
D0 to D7	Input/Output	Data input/output pins
$\overline{CE}$	Input	Chip Enable signal input pin
$\overline{OE}$	Input	Output Enable signal input pin
$\overline{RESET}$	Input	PROM mode setting pin
V_{PP}	Input	High-voltage application pin for program writing/verifying
V_{DD}	—	Positive power supply pin
GND	—	Ground potential pin

Block Diagram



Bus Interface Functions

This section describes the relationship between the various control signals used when the μPD71P301 is connected to a CPU.

Data Bus Width Selection

The data bus width is determined by the level of the UBE pin in the interval between the rise from low to high of the RESET signal, and the first subsequent fall of the ASTB signal. (See Table 3-1.)
Therefore, when the μPD71P301 is connected to a CPU with an 8-bit data bus, the $\overline{UBE}$ pin should be tied to V_{DD} with a pull-up resistor. And when connected to a CPU with a 16-bit data bus, the $\overline{UBE}$ pin should be tied to GND with a pull-down resistor, and the $\overline{UBE}$ pin and the pin which cvontrols the data bus width on the CPU side should be connected. The data bus operates as shown in Table 3-2.

Data Bus Width Selection

UBE Signal Level between RESET and ASTB	Data Bus Width	Functions of AD0 to AD7	Functions of AD8 to AD15
High	8 bits	A0 to A7 / D0 to D7	A8 to A15
Low	16 bits	A0 to A7 / D0 to D7	A8 to A15 / D8 to D15

Data Bus Operations

Data Bus Width	$\overline{UBE}$	A0	$\overline{OE}$	$\overline{WE}$	Data Bus AD0 to AD15		Memory Contents	
					AD8 to AD15	AD0 to AD7	Odd Addresses	Even Addresses
8 bits	1	0	0	1	High impedance	Read data (L)	—	—
	1	1	0	1	High impedance	Read data (H)	—	—
	1	0	1	0	High impedance	Write data (L)	—	Write data (L)
	1	1	1	0	High impedance	Write data (H)	Write data (H)	—
16 bits	0	0	0	1	Read data (H)	Read data (L)	—	—
	0	0	1	0	Write data (H)	Write data (L)	Write data (H)	Write data (L)
	0	1	0	1	Read data (H)	High impedance	—	—
	0	1	1	0	Write data (H)	*	Write data (H)	—
	1	0	0	1	High impedance	Read data (L)	—	—
	1	0	1	0	High impedance	Write data (L)	—	Write data (L)
	1	1	0	1	High impedance	Read data (H)	—	—
	1	1	1	0	High impedance	Write data (H)	Write data (H)	—

Note 1: H denotes odd-numbered address, L even-numbered.
2: A0 denotes least significant bit of address:
3: For combinations other than the above, data bus operation is indeterminate.
4: Asterisk (*) indicates dependence upon CPU output.

Connection To CPU With Fast Memory Access Function

A CPU which has a fast memory access function can use the μPD71P301's consecutive opcode fetch mode. CPU's with a fast memory access function are the μPD78322 and μPD78320.

Pins are connected as shown below.

CPU Pin Name	μPD71P301 Pin Name
ASTB	ASTB
AD0 to AD15	AD0 to AD15
$\overline{RD}$	$\overline{OE}$
$\overline{WR}$	$\overline{WE}$
TMD	TMD
$\overline{TAS}$	$\overline{TAS}$
	$\overline{UBE}$: With 8-bit data bus CPU, tie to V_{DD} with pull-up resistor. With 16-bit data bus CPU, tie to GND with pull-down resistor.
	$\overline{CE}$: Connect to GND.

Connection To CPU Without Fast Memory Access Function

In the case of a CPU which does not have a fast memory access function, the μPD71P301's consecutive opcode fetch mode cannot be used.

Pins are connected as shown below.

CPU Pin Name	μPD71P301 Pin Name
ASTB	ASTB
AD0 to AD15	AD0 to AD15
$\overline{RD}$	$\overline{OE}$
$\overline{WR}$	$\overline{WE}$
	TMD = 0
	$\overline{TAS}$ = 1
	$\overline{UBE}$: With 8-bit data bus CPU, tie to V_{DD} with pull-up resistor. With 16-bit data bus CPU, tie to GND with pull-down resistor.
	$\overline{CE}$: When using standby function, control CE pin or TMD pin externally. (See 3.7 "Standby Function".)

Application Examples

Microcomputer To Which μPD71P301 Can Be Connected

The Table below lists some of the microcomputers to which μPD71P301 can be connected.

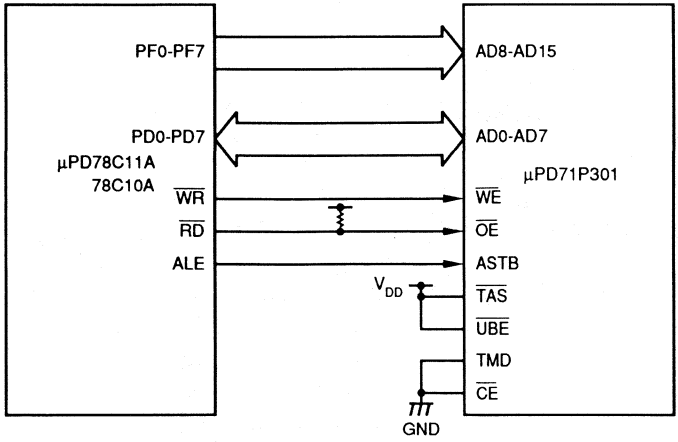
Table 8-1 Microcomputer to which μPD71P301 can be Connected
(V_{DD} = +5V ±10%, Ta = -10°C to 70°C)

Microcomputer Name	Oscillation Frequency
μPD78C11A, 78C12A, 78C14, 78C10A	15 MHz
μPD78224, 78220	12 MHz
μPD78214, 78213	12 MHz
μPD78312A, 78310A	12 MHz
μPD78322, 78320	16 MHz
μPD78328, 78327	16 MHz

Connection Example

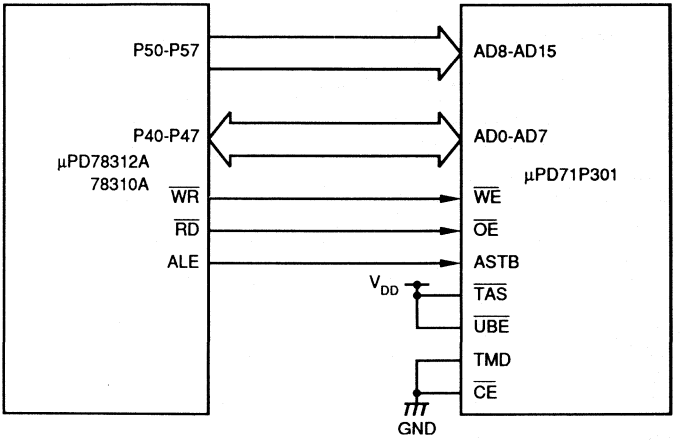
In the following μPD71P301 application example, a singlechip microcomputer is connected.

Example Of Connection To μPD78C11A or μPD78C10A



Connection to μPD78C11A or μPD78C10A

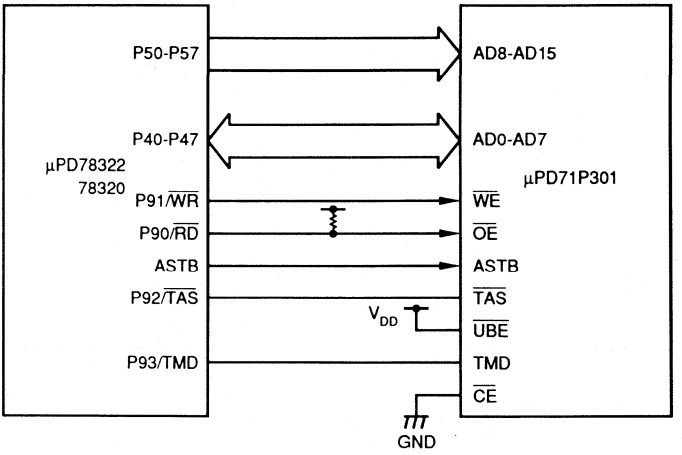
Example Of Connection To μPD78312A or μPD78310A



Connection to μPD78312A or μPD78310A

Example Of Connection To μPD78322 or μPD78320

The continuos instruction code fetch operation can be carried out.

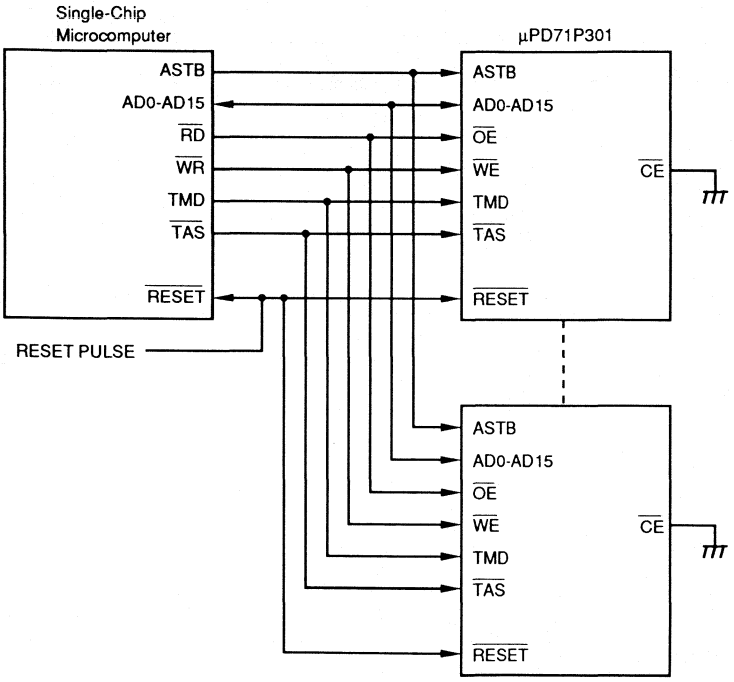


Connection to μPD78322 or μPD78320

Connection of More Than One μPD71P301

Connect the corresponding pins of two or more μPD71P301s. Execute mapping using the relation function so that the memory spaces do not overlap.

If the memory space has 1M byte or less, set CE pin to the low level.



Connection of more than One μPD71P301

Absolute Maximum Ratings
Ta = 25°C

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5 ~ + 7.0	V
	V_{PP}		-0.5 ~ +13.5	V
Input Voltage	V_I	Except TMD/A9	-0.5 ~ V_{DD} +0.5	V
	V_I	TMD/A9	-0.5 ~ +13.5	V
Output Voltage	V_O		-0.5 ~ V_{DD} +0.5	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	-4.0	mA
		All Output Pin Total	-50	mA
Operating Temperature	T_{opt}		-10 ~ +70	°C
Storage Temperature	T_{stg}		-65 ~ +150	°C

Capacitance (Ta=25°C,V_{DD}=V_{ss}=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f_C = 1MHz Unmeasured pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	C_{IO}				20	pF

DC Characteristics
Ta = -10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH1}	Except $\overline{RESET}$	2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$	0.8 V_{DD}		V_{DD}	
Input Low Voltage	V_{IL1}	Except $\overline{RESET}$	0		0.8	V
	V_{IL2}	$\overline{RESET}$	0		0.2 V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL}=2.0mA			0.45	V
Output High Voltage	V_{OH1}	I_{OH}=-1.0mA	V_{DD}-1.0			V
	V_{OH2}	I_{OH}=-100μA	V_{DD}-0.5			V
Input Leakage Current	I_{LI}	0V≤V_I≤V_{DD}			±10	μA
Output Leakage Current	I_{LO}	0V≤V_O≤V_{DD}			±10	μA
V_{DD} supply current	I_{DD1}	Operation mode		40		mA
	I_{DD2}	Standby mode		1		μA
V_{PP} Supply Current	I_{PP}	Operation mode		1		μA

AC Characteristics (V_{DD}=5.0V±10%, Ta = -10°C to +70°C)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ASTB High-Level Width	t_{ASWH}		30			ns
Address Setup Time (to ASTB↓)	t_{SAAS}		25			ns
Address Hold Time (from ASTB↓)	t_{HASA}		20			ns
$\overline{OE}$ Delay Time from ASTB↓	t_{DASOE}		20			ns
Data Output Time (from $\overline{OE}$↓)	t_{DOEOD}	C_L = 100 pF	0			ns
Data Hold Time (from $\overline{OE}$↑)	t_{HOEOD}	C_L = 100 pF	0			ns
$\overline{OE}$ Low-Level Width	t_{OEWL}		80			ns
TMD Setup Time (to ASTB↓)	t_{STMAS}		48			ns
TMD↓ Delay Time from ASTB↓	t_{DASTM}		60			ns
$\overline{TAS}$↑ Delay Time from TMD↓	t_{DTMFTA}		90			ns
$\overline{TAS}$↑ Delay Time from TMD↑	t_{DTMRTA}		80			ns
$\overline{TAS}$ Setup Time (to ASTB↓)	t_{STAAS}		30			ns
TMD↑ Delay Time from $\overline{TAS}$↑	t_{DTATM}		30			ns
Data Output Time (from $\overline{TAS}$↑)	t_{DODTA}	C_L = 100 pF			60	ns
Data Hold Time (from $\overline{TAS}$↑)	t_{HODTA}		0		40	ns
$\overline{TAS}$ Cycle Time	t_{CYTA}		99			ns
$\overline{TAS}$ High-Level Width	t_{WTAH}		30			ns
$\overline{TAS}$ Low-Level Width	t_{WTAL}		30			ns
Data Output from Address	t_{DAOD}				180	ns
Port Data Hold Time (from ASTB↑)	t_{HPDAS}	C_L = 100 pF	0			ns
Port Data Hold Time (from $\overline{TAS}$↑)	t_{HPDTA}	C_L = 100 pF	0			ns
Port Data Output Time (from $\overline{TAS}$↑)	t_{DPDTA}	C_L = 100 pF			75	ns
Port Address Output Time from Address	t_{DAPA}	C_L = 100 pF			110	ns
$\overline{CE}$ Setup Time (to $\overline{OE}$↑)	t_{SCEOE}		30			ns
Port Data Hold Time (from TMD↑)	t_{HTMPD}		0			ns
Port Data Output Time from TMD↑	t_{DTMPD}				100	ns
$\overline{WE}$ Low-Level Width	t_{WEWL}		100			ns
Data Setup Time (to $\overline{WE}$↑)	t_{SIDWE}		80			ns
Data Hold Time (from $\overline{WE}$↑)	t_{HWEID}		10			ns
$\overline{WE}$↓ Hold Time from ASTB↓	t_{DASWE}		20			ns
$\overline{WE}$↓ Hold Time from Addess	t_{DAWE}		60			ns

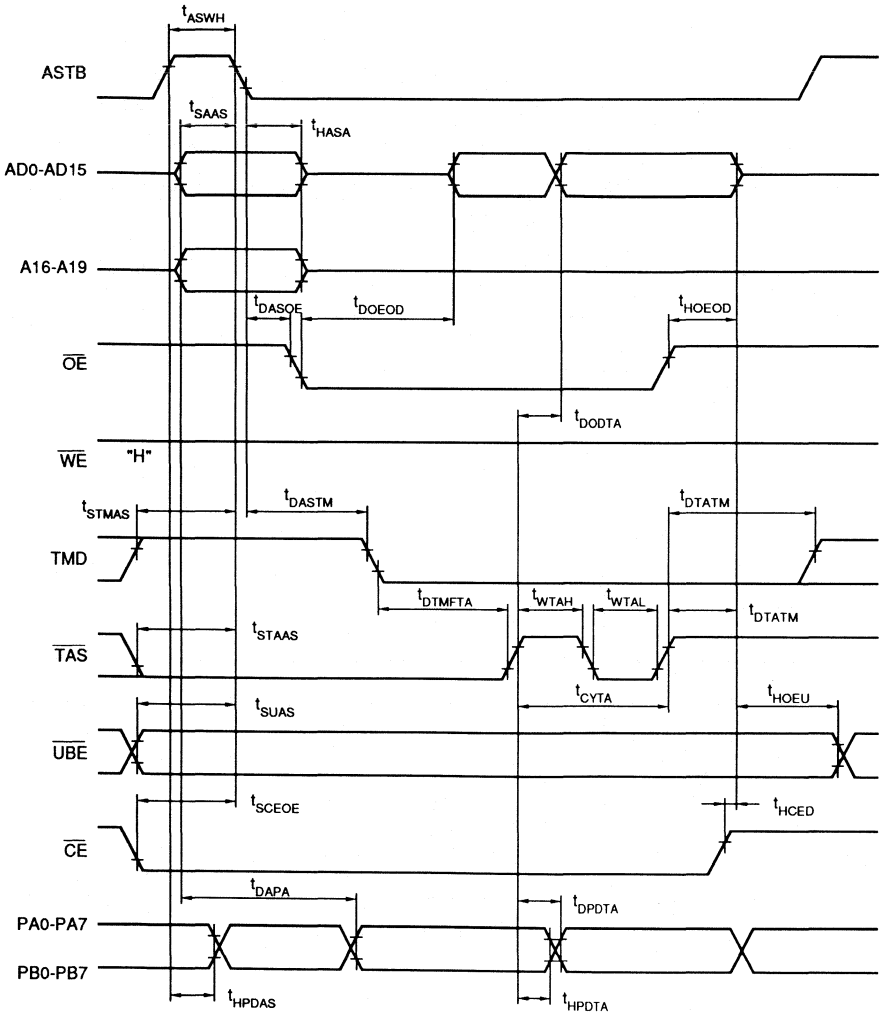
(to be continued)

AC Characteristics (V_{DD}=5.0V±10%, Ta = -10°C to +70°C) (cont'd)

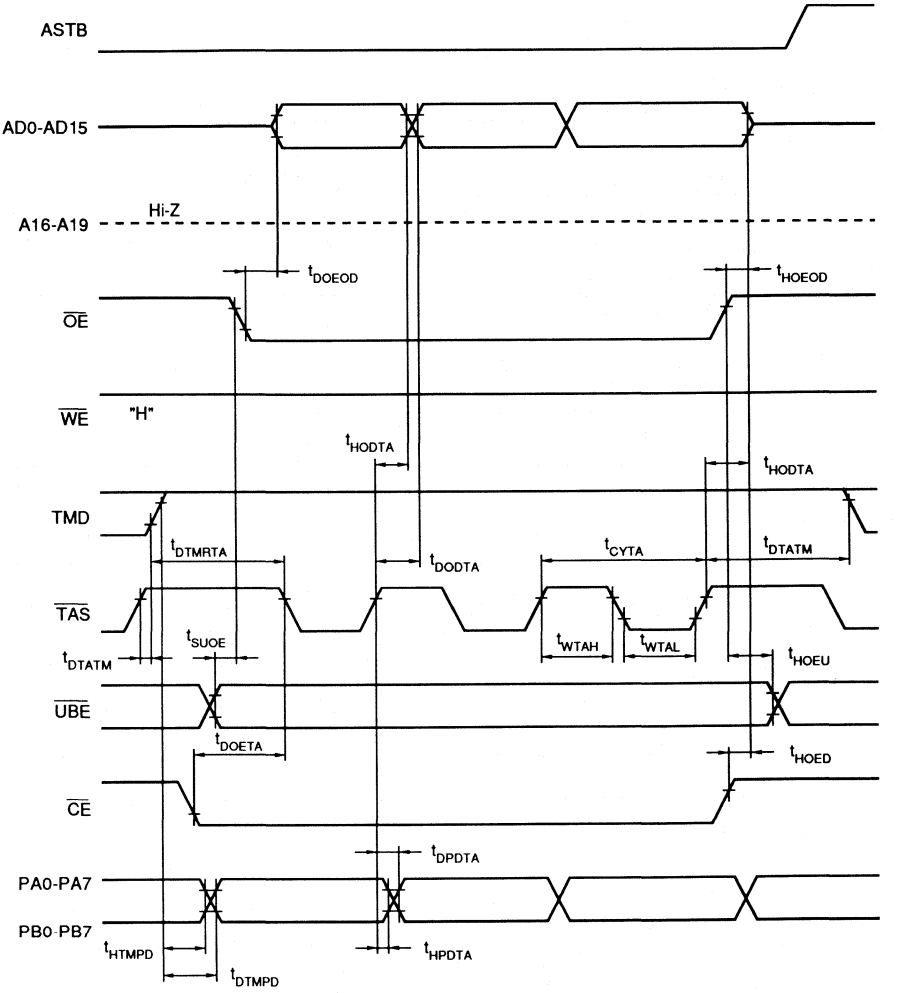
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
$\overline{UBE}$ Setup Time (to ASTB↓)	t_{SUAS}		30			ns
$\overline{UBE}$ Hold Time (from $\overline{OE}$↑)	t_{HOEU}		20			ns
$\overline{UBE}$ Hold Time (from $\overline{WE}$↑)	t_{HWEU}		20			ns
Data Setup Time (to $\overline{TAS}$↑)	t_{SIDTA}		80			ns
$\overline{WE}$↑ Delay Time from $\overline{TAS}$↑	t_{DTAWE}		0			ns
ASTB Interval Time	t_{INTAS}		30			ns
$\overline{UBE}$ Setup Time (to $\overline{OE}$↓)	t_{SUOE}		25			ns
$\overline{TAS}$↑ Delay Time from ASTB↓	t_{DASTAR}		180			ns
ASTB↑ Delay Time from $\overline{TAS}$↑	t_{DTAAS}		10			ns
$\overline{TAS}$↓ Delay Time from ASTB↓	t_{DASTAF}		30			ns
TMD Hold Time (from $\overline{WE}$↑)	t_{HTMWE}		20			ns
Write Data Hold Time (from $\overline{TAS}$↑)	t_{HTAID}		10			ns
Data Hold Time (from $\overline{CE}$↑)	t_{HCID}	C_L = 100 pF	0			ns
$\overline{TAS}$↓ Delay Time from $\overline{CE}$↓	t_{DCETA}		100			ns
$\overline{CE}$↑ Delay Time from $\overline{WE}$↓	t_{DWEFCE}		20			ns
$\overline{TAS}$↓ Delay Time from $\overline{CE}$↑	t_{DCETA}		20			ns
$\overline{RESET}$ Low-Level Width	t_{WRESL}		0.5			ns
$\overline{RESET}$ High-Level Width	t_{WRESH}		0.5			ns
Setup Time (to $\overline{RESET}$↑)	t_{SURES}		50			ns
Hold Time (from $\overline{RESET}$↑)	t_{HRESU}		500			ns
ASTB↓ from $\overline{RESET}$↑ (first memory access)	t_{DRESAS}		150			ns
$\overline{CE}$ Setup Time (to ASTB↓)	t_{SCEAS}		25			ns
Data Hold Time (from $\overline{CE}$↑)	t_{HCED}	C_L = 100 pF	0		40	ns
$\overline{CE}$↑ Delay Time from $\overline{WE}$↑	t_{DWERCE}		20			ns
$\overline{CE}$↑ Delay Time from $\overline{OE}$↑	t_{DOECE}		20			ns
Data Output Time (from $\overline{CE}$↓)	t_{DCEOD}	When $\overline{CE}$ = 0	0		150	ns

Timing Waveforms

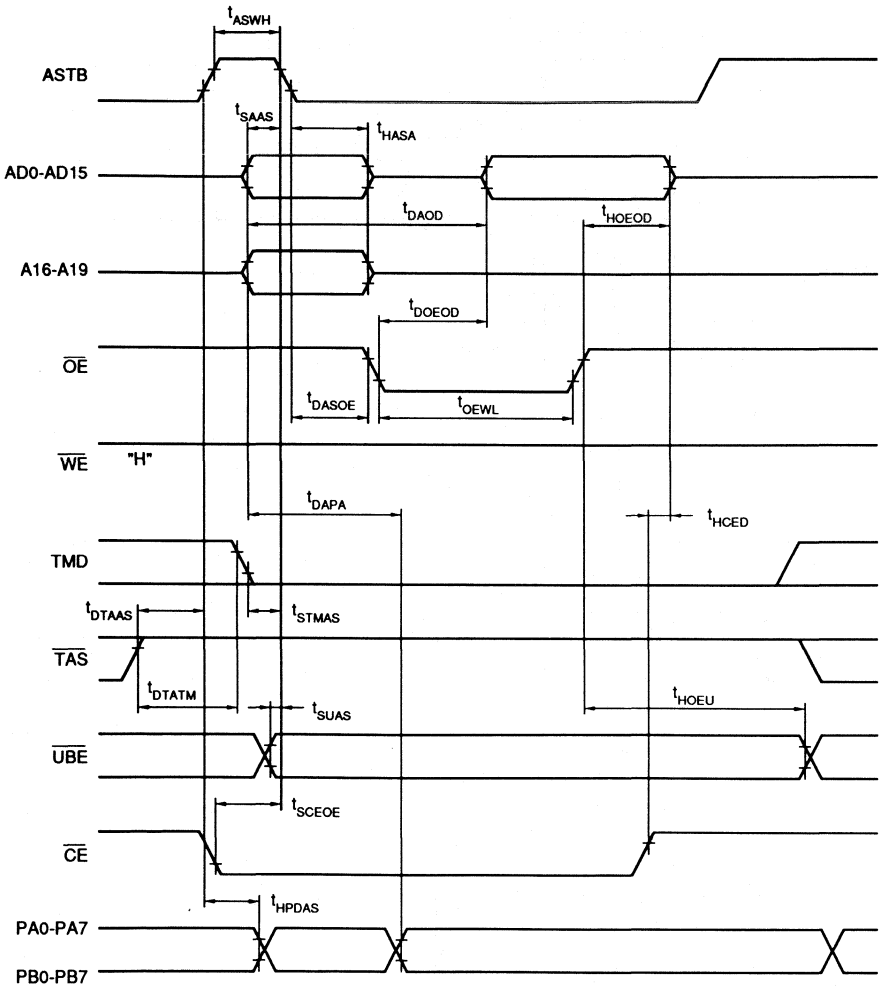
Branch Operation Mode



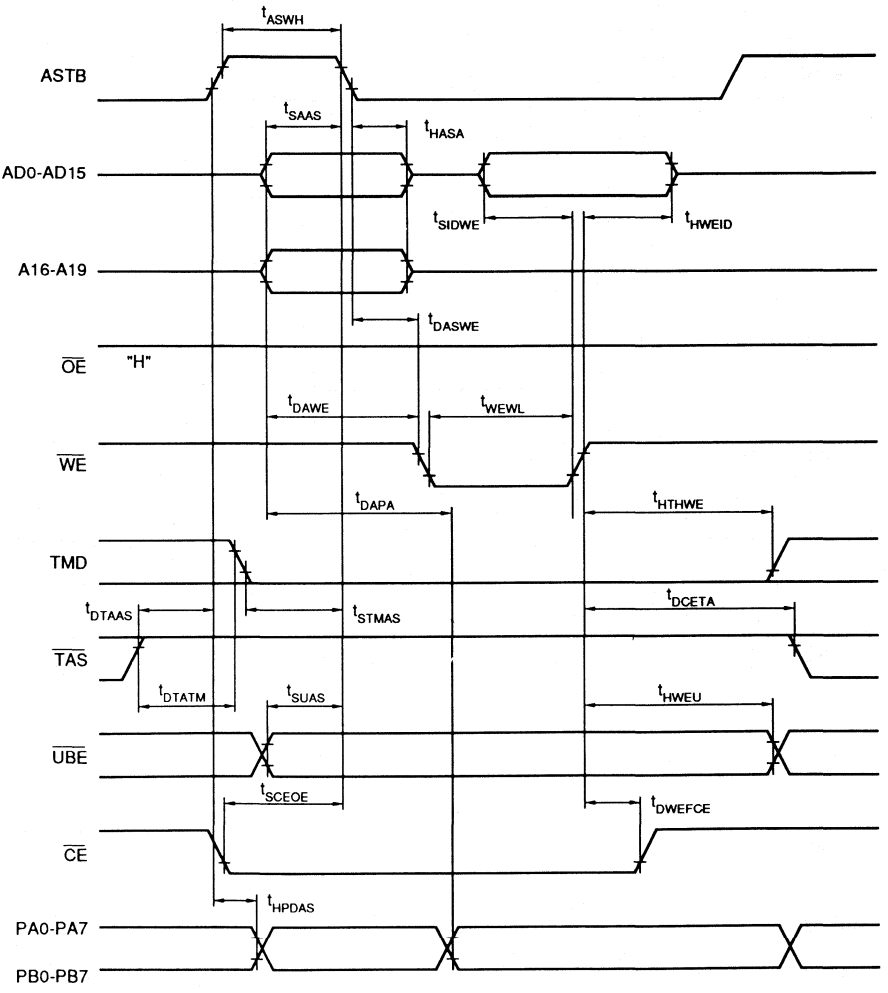
Continuous Instruction Code Fetch Mode



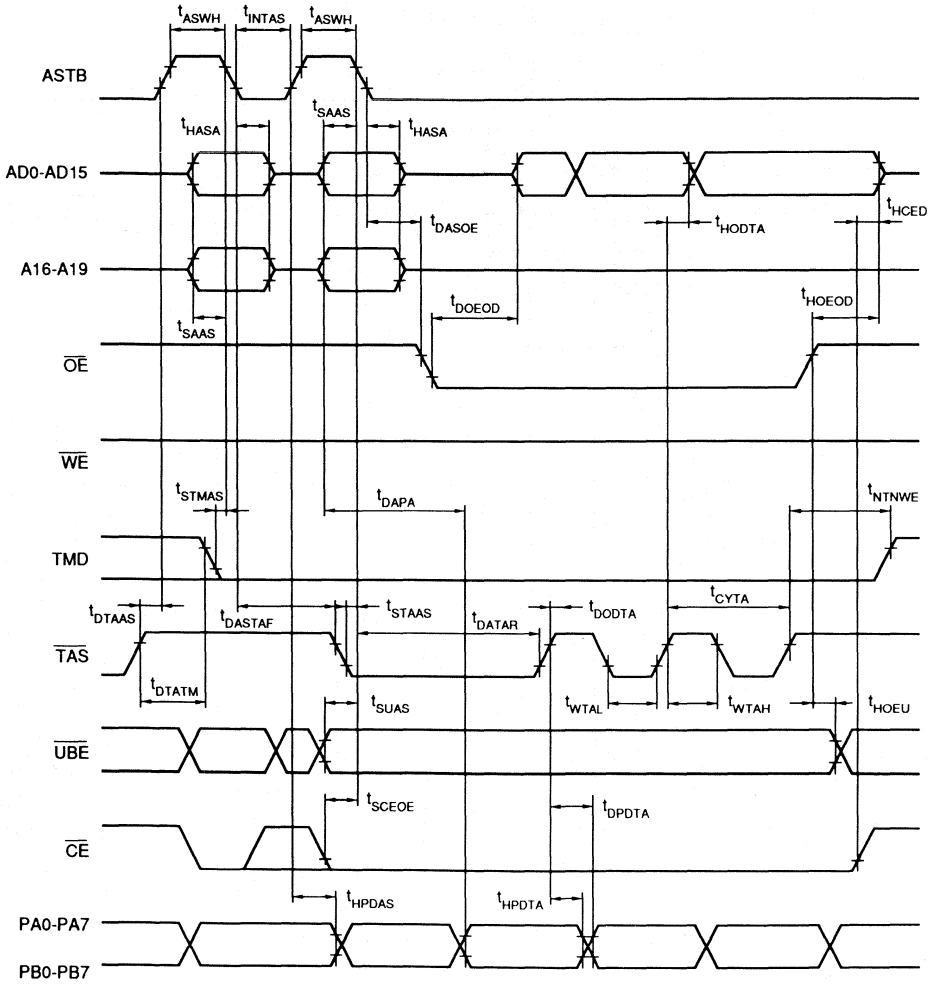
Discontinuous Data Read Mode



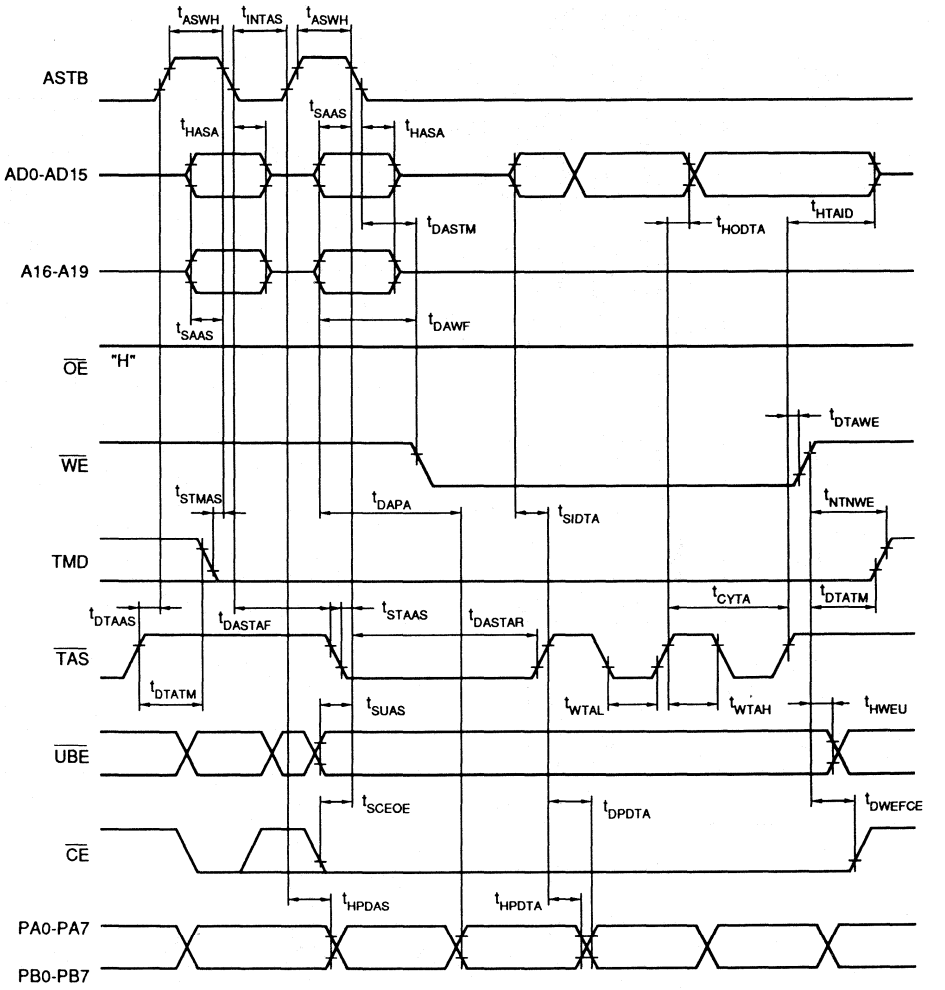
Discontinuous Data Write Mode



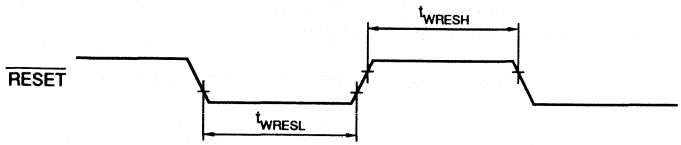
Continuous Data Read Mode

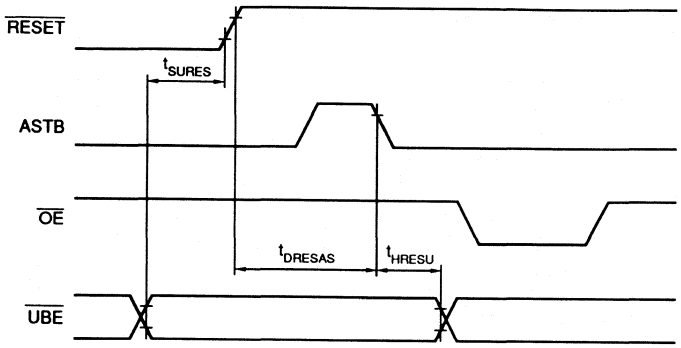


Continuous Data Write Mode



Other Mode


t_{WRESH}
RESET
t_{WRESL}


RESET
t_{SURES}
ASTB
OE
t_{DRESAS}
t_{HRESU}
UBE

PROM Programming Mode

Two types of μPD71P301 program memories are available, the reprogrammable PROM. The normal programming mode or the PROM programming mode can be selected by changing the $\overline{\text{RESET}}$ input level.

CAUTION 1: In case of μPD71P301KA equipped with an erase window, apply a protective seal to the erase window in all cases except for PROM erase.

2: The one-time programmable μPD71P301L is not equipped with an erase window and cannot erase ultra violet rays.

PROM Programming Operation Mode

When $\overline{\text{RESET}}$ pin is set to the low level, the μPD71P301 is enable for PROM programming (write/verify/read). The Table below lists the PROM programming modes which can be set using $\overline{\text{CE}}$ and $\overline{\text{OE}}$ pins.

PROM Programming Modes

Operation Mode	CE	OE	V_{PP}	V_{DD}	RESET
Read	L	L	+5 V	+5 V	L
Output disable	L	H			
Standby	H	x*			
Program	L	H	+12.5 V	+6 V	
Program verify	H	L			
Program inhibit	H	H			

*: x: L or H

Unused Pin Treatment

Fix all pins which have no function in the PROM programming mode to the low level using an external pull-down resistor.

PROM Write Procedure

Use the following PROM write procedure. Data can be written at high speeds.

(1) Supply +6 V and +12.5 V to the V_{DD} and V_{PP} pins, respectively.

(2) Supply an initial address.

(3) Supply write data.

(4) Supply $\overline{\text{CE}}$ pin with a 1 ms program pulse (active low).

(5) Set the verify mode. If data has been written, go to (7). If data has not been written goto (7) and repeat (3) to (5). If data cannot be written by repeating the write operation 25 times, go to (6).

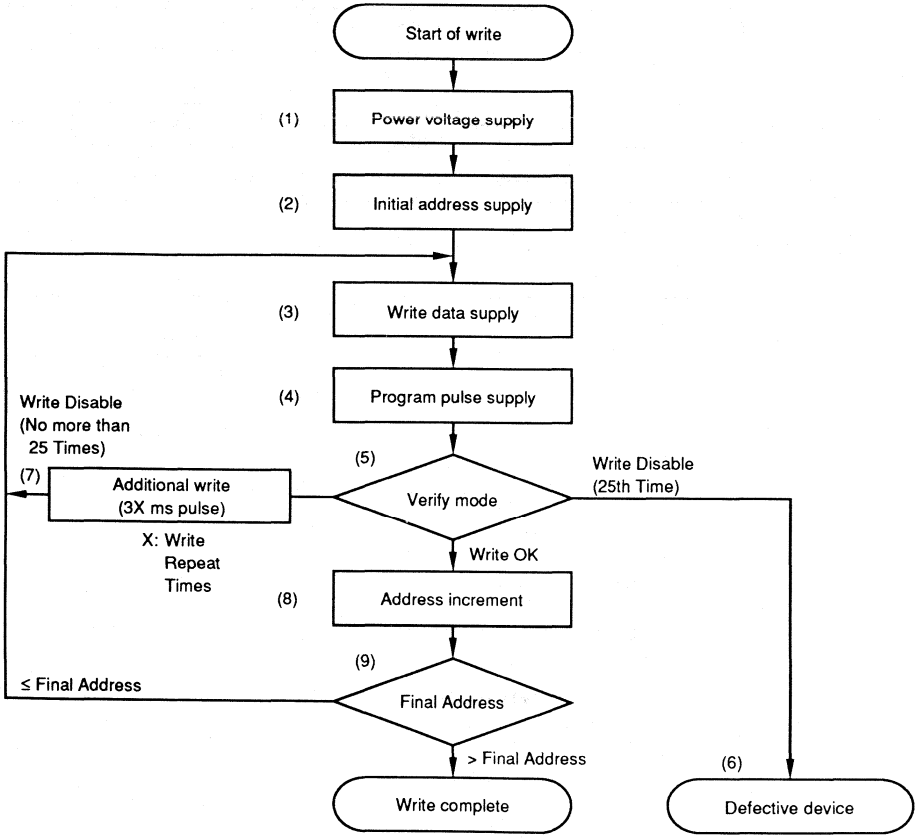
(6) Stop the write operation by judging the device to be defective.

(7) Supply write data and supply $\overline{\text{CE}}$ pin with ((3) to (5) repeat times: X) x 3 ms program pulses (additional write).

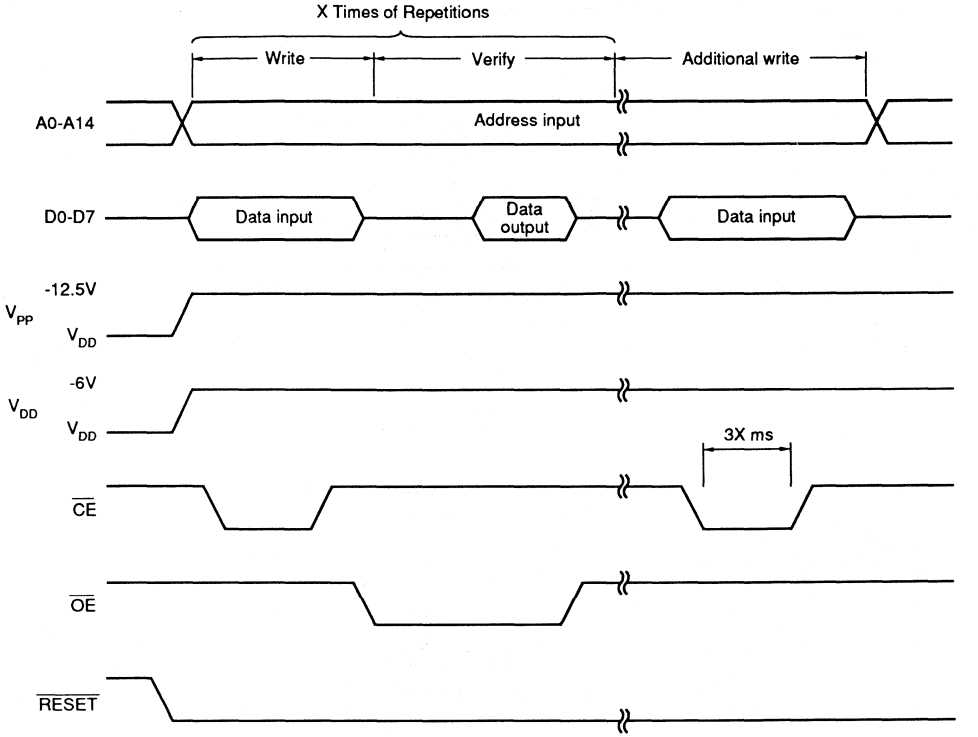
(8) Increment the addess.

(9) Repeat (3) to (8) up to the last address.

The Figure below is a flowchart of the PROM write operations.



Write Flowchart



PROM Write/Verify Timings

PROM Read Procedure

PROM contents can be read into the external data buses (D0 to D7) by using the following procedure:

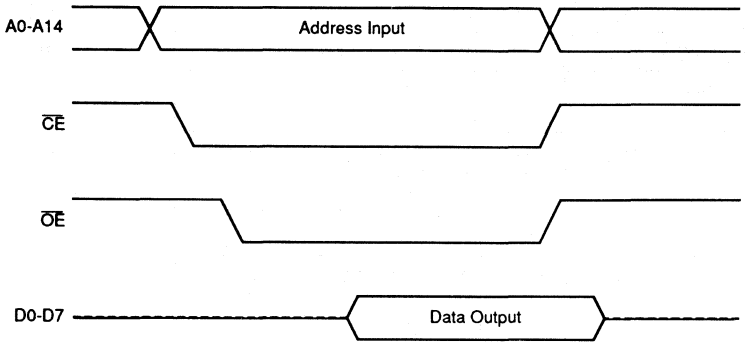
(1) Suplly +5 V to V_{DD} and V_{PP} pins.

(2) Input the address to be read to A0 to A14 pins.

(3) Set the read mode.

(4) Output data to D0 to D7 pins.

The Figure below shows the timings of these operations.



PROM Read Timings

Erasion Characteristics (μPD71P301KA Only)

The μPD71P301KA can erase (FFH) the programmed data contents by applying rays having a wavelength of shorter than about 400 nm.

When erasing the μPD71P301KA program memory contents, normally apply ultra violet rays having a wavelength of 254 nm. A minimum of 15 Ws/cm^2 (ultra violet ray strength x erase time) is necessary for erasing the μPD71P301KA contents completely. The erase time is about 15 to 20 minutes (when a 12000 μW/cm^2 ultra violet lamp is used). The erase time may become longer due to deterioration of the ultra violet lamp performance, fouling of the package window section, etc. For proper erasure, place the μPD71P301KA within 2.5 cm of the ultra violet lamp. If the ultra violet lamp has s filter, remove the filter and carry out the erase operation.

Erase Window Seal (μPD71P301KA Only)

To prevent erroneous erasure due to rays coming from sources other than PROM contents erase lamp or preventing an internal circuit other than the PROM circuit from malfunctioning due to rays, apply a protective seal to the erase window in cases except PROM contents erasure.

DC Programming Characteristics

(Ta = 25°C ±5°C, V_{IP} = 12.0V ±0.5V, V_{SS} = 0V)

Parameter	Symbol	Symbol*	Test Conditions	Min.	Typ.	Max.	Unit
Input Voltage High	V_{IH}	V_{IH}		2.2		V_{DDP}+0.3	V
Input Voltage Low	V_{IL}	V_{IL}		-0.3		0.8	V
Input Leakage Current	V_{LIP}	L_{LI}	$0 \le V_I \le V_{DDP}$			10	μA
Output Voltage High	V_{OH}	V_{OH}	I_{OH} = -400 μA	2.4			V
Output Voltage Low	V_{OL}	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Input Voltage	V_{A9}		TMD/A9 pin			±10	μA
Output Leakage Current	I_{LO}		$0 \le V_O \le V_{DDP}$, $\overline{OE} = V_{IH}$			10	μA
PROG Pin High-Voltage Input Current	I_{IP}					±10	μA
V_{DDP} Supply Voltage	V_{DDP}	V_{DD}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode		$V_{PP} = V_{DDP}$		V
V_{DDP} Supply Current	I_{DD}	I_{DD}	Program memory write mode		10	30	mA
			Program memory read mode $\overline{CE} = V_{IL}$, $V_I = V_{IH}$		10	30	mA
V_{PP} Supply Current	I_{PP}	I_{PP}	Program memory write mode $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		10	30	mA
			Program memory read mode		1	100	μA

* Symbol of the corresponding μPD27C256A

AC Programming Characteristics

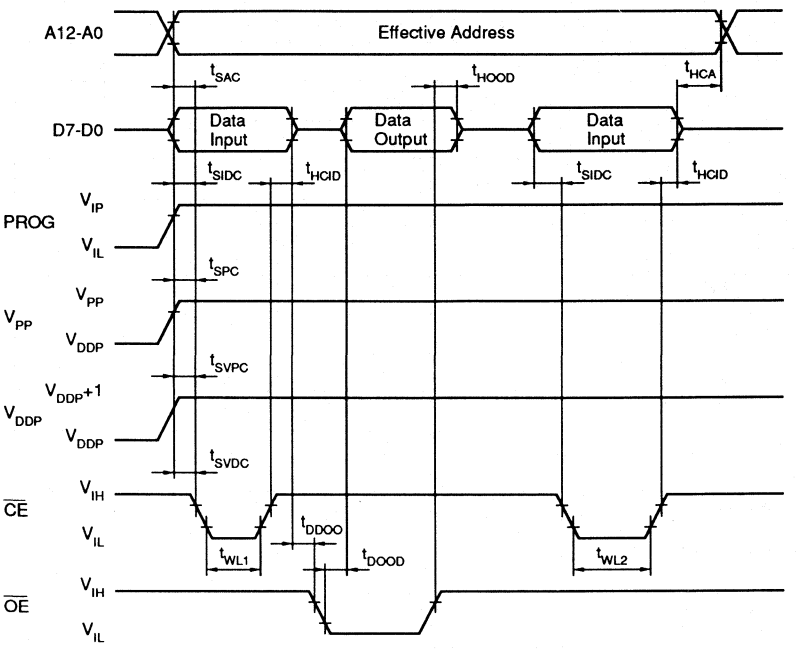
(Ta = 25°C ±5°C, V_{IP} = 12.0V ±0.5V, V_{SS} = 0V)

Parameter	Symbol	Symbol*	Test Conditions	Min.	Typ.	Max.	Unit
Address Setup Time (to $\overline{CE}\downarrow$)	t_{SAC}	t_{AS}		2			μs
$\overline{OE}\downarrow$ Delay Time from Data	t_{DDOO}	t_{OES}		2			μs
Input Data Setup Time (to $\overline{CE}\downarrow$)	t_{SIDC}	t_{DS}		2			μs
Address Hold Time (from $\overline{CE}\uparrow$)	t_{HCA}	t_{AH}		2			μs
Input Data Hold Time (from $\overline{CE}\uparrow$)	t_{HCID}	t_{DH}		2			μs
Output Data Hold Time (from $\overline{OE}\uparrow$)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} Setup Time (to $\overline{CE}\downarrow$)	t_{SVPC}	t_{VPS}		2			μs
V_{DDP} Setup Time (to $\overline{CE}\downarrow$)	t_{SVDC}	t_{VDS}		2			μs
Initial Program Pulse Width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Additional Program Pulse Width	t_{WL2}	t_{OPW}		2.85		78.75	ms
PROG High-Voltage Input Setup Time (to $\overline{CE}\downarrow$)	t_{SPC}			2			μs
Data Output Time from Address	t_{DAOD}	t_{ACC}	$\overline{OE} = V_{IL}$			2	μs
Data Output Time from $\overline{OE}\downarrow$	t_{DOOD}	t_{OE}				1	μs
Data Hold Time (from $\overline{OE}\uparrow$)	t_{HCOD}	t_{DF}		0		130	ns
Data Hold Time (from Address)	t_{HAOD}	t_{OH}	$\overline{OE} = V_{IL}$	0			ns

* Symbol of the corresponding μPD27C256A

2

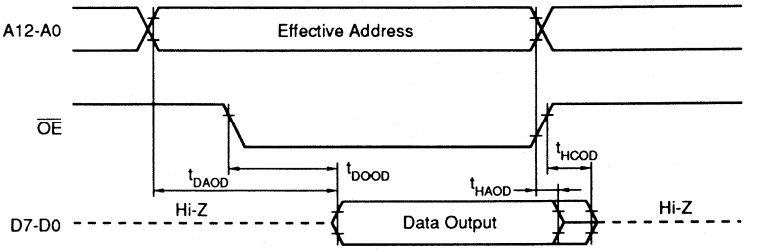
PROM Write Mode Timings



CAUTION: 1: Apply V_{DDP} before V_{PP} and shut it off after V_{PP}.

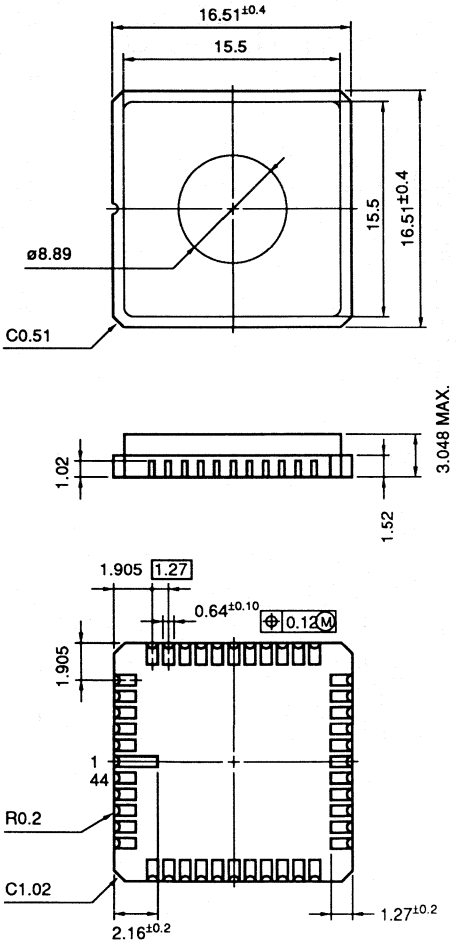
2: Do not allow V_{PP} to become +13 V or more including an overshoot.

PROM Read Mode Timings



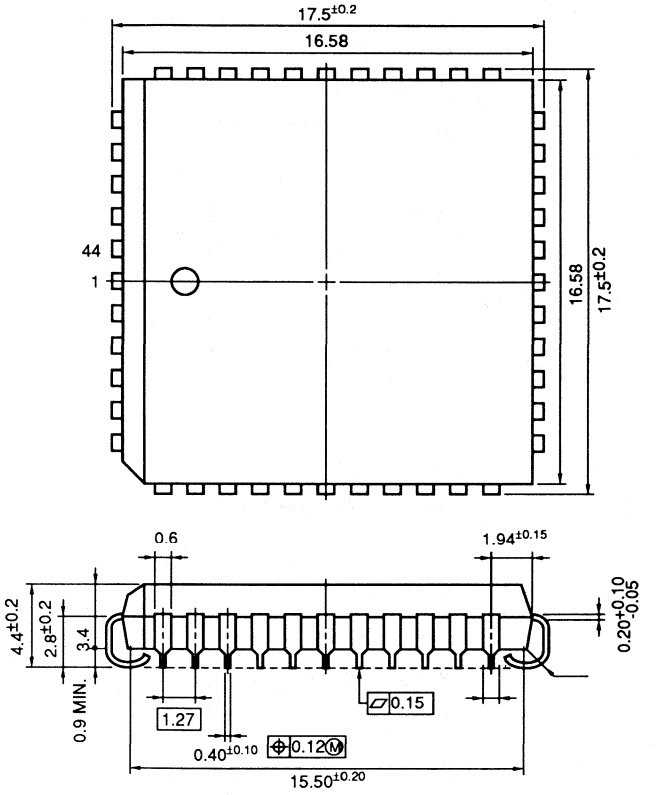
Package Information

44-Pin LCC Package (Unit: mm)



X44KW-50A

44-Pin PLCC Package (Unit: mm)



P44L-50A1

Appendix A. Caution Relating to Operation of More Than One μPD71P301

A.1 Continuous Operation Mode

As shown in Appendix Figure A-1, when mapping the μPD71P301 in the memory area leading to the general-purpose memory or I/O device, the μPD71P301 may malfunction if its address output is input to the general-purpose memory or I/O device.

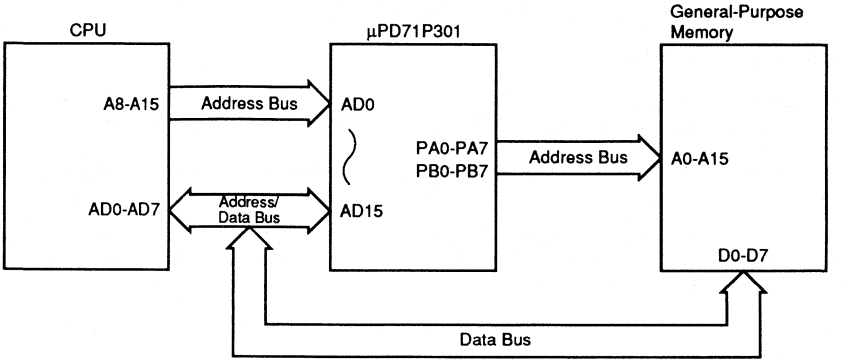
When the μPD71P301 carries out the continuous data read operation, 1 is added to the internal address and the sum becomes the address output.

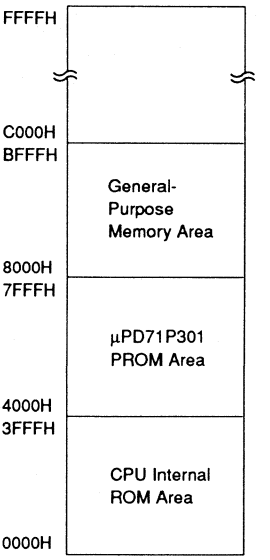
For example, when continuously reading the contents at addresses 7FFEH and 7FFFH in the continues instruction fetch operation, 1 is added to each μPD71P301 address (refer to Appendix Figure A-2). Thus, the μPD71P301 address will collide on the data bus with the general-purpose memory data mapped at address 8000H in the cycle of reading data at address 7FFFH.

Both data will also collide with each other when the chip select address is specified at 8000H using the chip select signal output function of the μPD71P301.

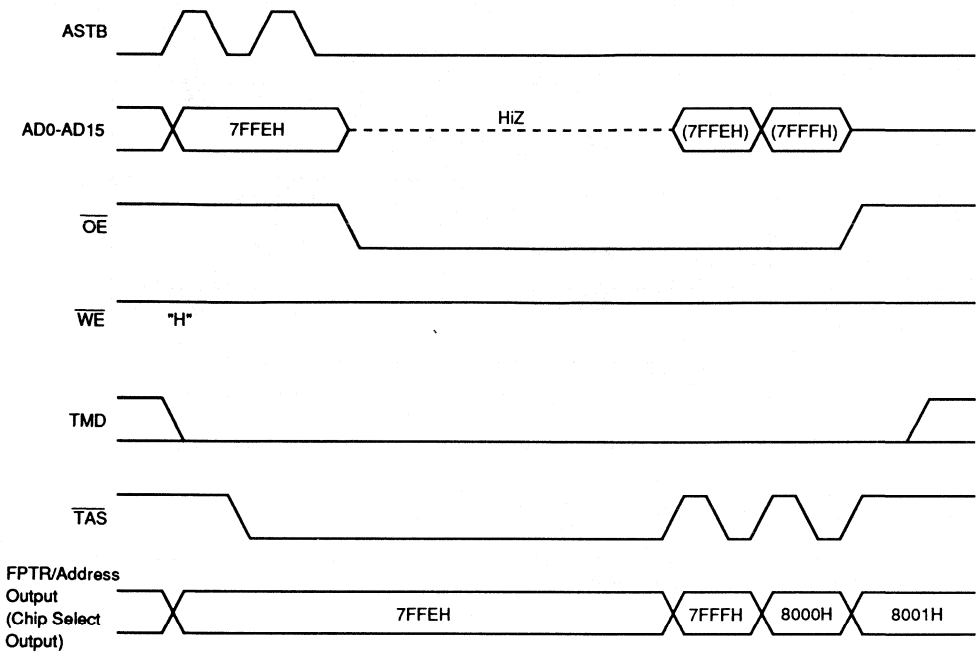
Note the following:
- Do not map the general-purpose memory or I/O device at consecutive addresses.
- When mapping at consecutive addresses, do not carry out the continuous operation on the boundary area.

Examples of circuits against data collision on the bus are shown in Appendix Figure A-3 (in case of general-purpose memory connection) and Appendix Figure A-4 (in case of I/O device connection).

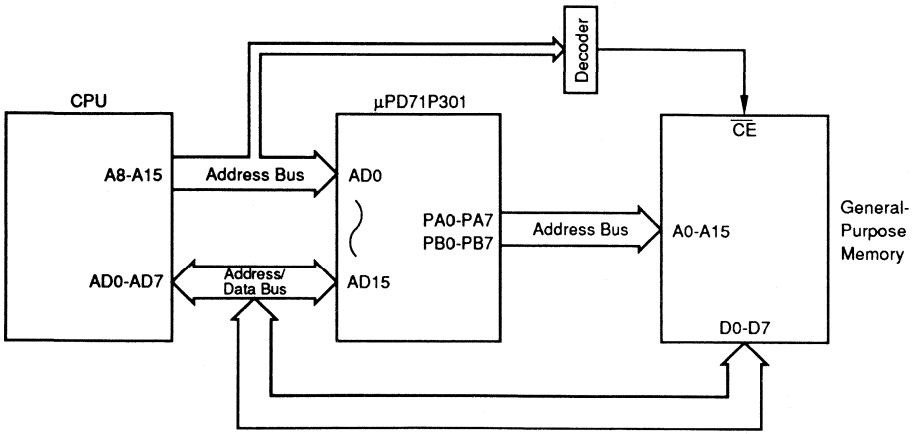




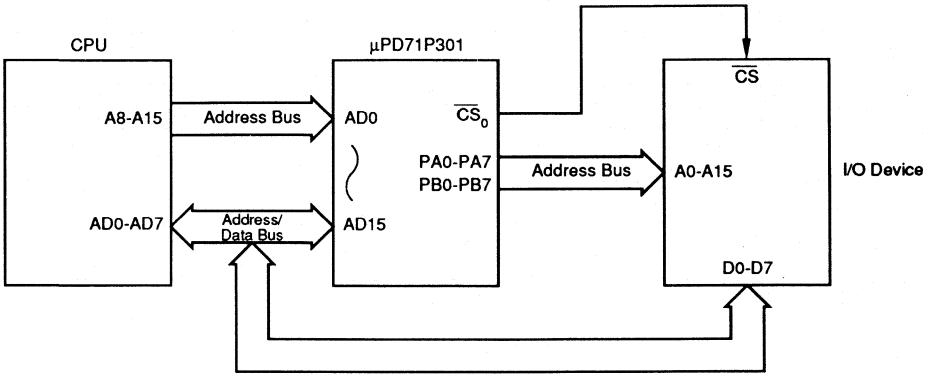
Appendix Figure A-1 Example of Parallel Connection with General-Purpose Memory



Appendix Figure A-2 Continuous Data Read Operation Example (Timing Chart)



Appendix Figure A-3 Example of Circuit to Prevent Data Collision (in Case of General-Purpose Memory Connection)



Appendix Figure A-4 Example of Circuit to Prevent Data Collision (in Case of I/O Device)

A.2 Caution Relating to Chip Select Output

When using the chiip select signal output function of the μPD71P301, the μPD71P301 may malfunction if the chip select address is set to overlap the μPD71P301 mapping address.

Description

The μPD71P302 is a peripheral LSI device, a Turbo Access Manager (TAM2) for microcomputer use which integrates a 16k Byte EPROM, 1k Byte SRAM, 32 I/Os, plus memory access and bus interface functions. When used in combination with μPD78330/334 or μPD78600/602 the TAM2 provides ROM and RAM expansion with the same speed as internal ROM/RAM of the microcomputers. One word will be fetched per clock cycle without having the address supplied from the microcomputer. Without the speed advantage the μPD71P302 can also be connected to other microcomputers or microprocessors which have a multiplexed address/data bus. The TAM2 allows compact application systems configurations due to efficient memory size expansion.

Features

- High speed memory access function
  opcode & data read speed: 1 word per clock cycle (max)
- Directly connectable to address/data multiplex bus
- Internal memory space relocation function
  For 1M-byte memory
- External expanded address output function
- Chip select signal output function (4 outputs)
- Cascadable for ROM size expansion
- EPROM: 16k bytes
- SRAM: 1k byte
- I/O Lines: 32

Ordering Information

Part Number	Package Type	ROM
μPD71P302KB	64-PIN LCC	UVPROM
μPD71P302KC	68-PIN LCC	
μPD71P302RQ	64-PIN QUIP	
μPD71P302GF	64-PIN QFP	OTPROM
μPD71P302L	68-PIN PLCC	
μPD71P302GQ	64-PIN QUIP	

LCC = Leadless Chip Carrier
QFP = Quad-Flat Pack (SMD)
PLCC = Plastic Leaded chip carrier

2

Difference Between μPD71P302 and μPD71P301

The Table of The Functional Difference Between The μPD71P302 And The μPD71P301

Function	μPD71P302	μPD71P301
Operating Mode	Normal opcode fetch mode High-speed opcode fetch mode Normal data read mode Normal data write mode High-speed data read mode High-speed data write mode Non-clock normal data read mode Non-clock normal data write mode	Branch Consecutive opcode fetch Non-consecutive data read Non-consecutive data write Consecutive data read Consecutive data write
Synchronizing signal	CLK	$\overline{TAS}$
Ports Port mode control by AR	PORT0, PORT1, PORT4, PORT5 Controlled by AR13, AR14, AR15 AR13: P40 to 47, P50 to 57/ A0 to 7, A8 to A15 AR14: P00 to 03 / CS0 to 03 AR15: P04 to 07 / A16 to 19	PORTA, PORTB Controlled by the combination of AR13, AR14, AR15, to A0 to 15, CS0 to 3, A16 to A19
Data bus width setting	Setting by AR register bit "DBW"	Setting by the UBE level during RESET to the first ASTB
Access cycle control	Programmable to 1-clock mode or 2-clock mode by AR register	1-access / 1-TAS-cycle only
Package	64FP/LCC, 64QUIP, 68PLCC/LCC	44PLCC/LCC, 64FP/LCC, 64QUIP
Standby control	• At non-clock normal data read/write mode • CE=1, ASTB=0, OE=1, LWE=1, HWE=1 • At modes except the non-clock normal data read/write mode • ASTB=0, OE=1, LWE=1, HWE=1, CLK=1/0 • At chip select function enable • add TAS=1, TMD=1 to above one	• CE=1, ASTB=0 or • CE=0, ASTB=0, the condition disabled by the relocation function • At chip select function enable • add TAS=1, TMD=1 to above one

The Table of The Functional Difference Between The μPD71P302 And The μPD71P301

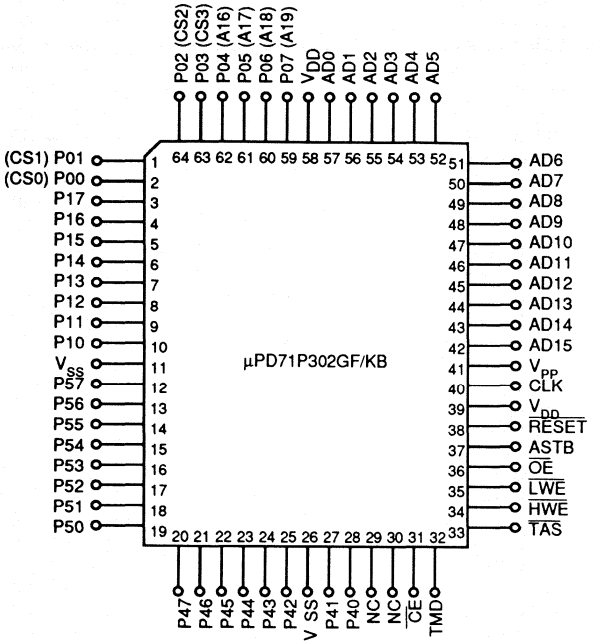
Memory access operation		Operating Mode	
		μPD71P302	μPD71P301/μPD71P301A*
Data access for microcomputer provided TAM I/F	Opcode fetch in normal memory access cycle	Normal opcode fetch	Non-consecutive data read
	Setting FPTR High-speed fetch	Normal data read High-speed opcode fetch	Branch Consecutive opcode fetch
	Data read in normal memory access cycle	Normal data read	Non-consecutive data read
	Data write in normal memory access cycle	Normal data write	Non-consecutive data write
	Setting DPTR for consecutive data read/write	Normal data read and Normal data write	Not required
	High-speed data read	High-speed data read	Consecutive data read
	High-speed data write	High-speed data write	Consecutive data write
Data access for microcomputer not provided TAM I/F	data read	Non-clock normal data read	Non-consecutive data read
	data write	Non-clock normal data write	Non-consecutive data write

*: Under development

2. Pin configuration (Top View)

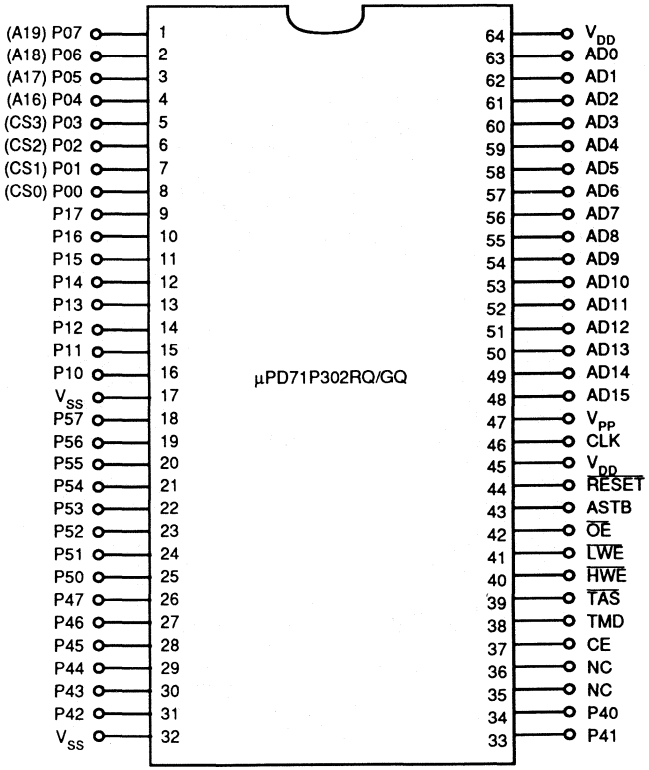
68-Pin LCC/PLCC configuration will be announced later.

(1) Normal Operating Mode ($\overline{RESET}$=1)
(i) 64-Pin LCC/FLAT Configuration

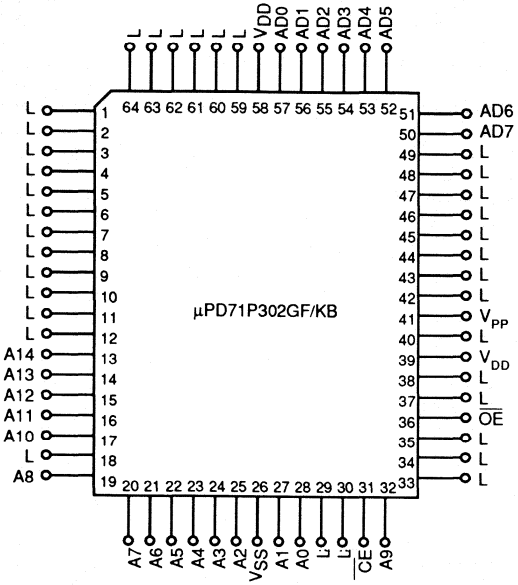


2

(ii) 64-Pin QUIP Configuration

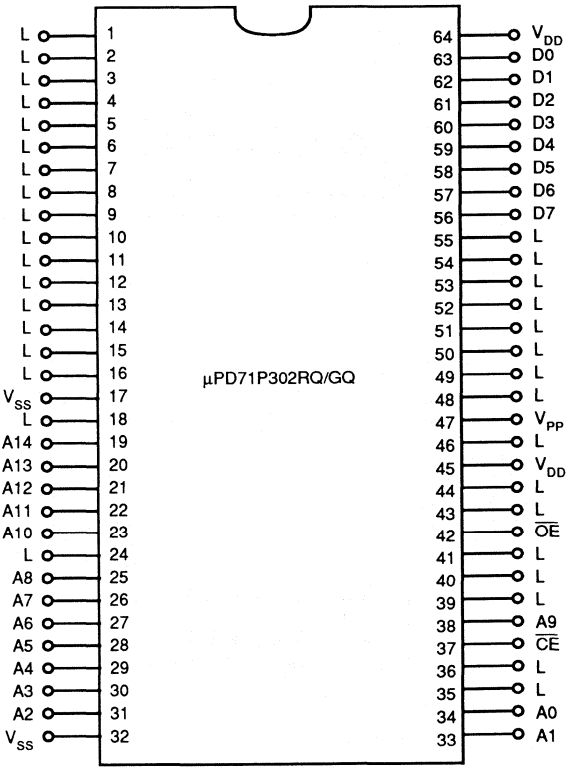


(2) PROM Programming Mode ($\overline{RESET}$=0)
(i) 64-Pin LCC/FLAT Configuration



L: Pull down

(ii) 64-Pin QUIP Configuration



L: PULL DOWN

RESET	:	Reset	TMD	:	Turbo Mode
CE	:	Chip Enable	P00 to P07	:	Port 0
AD0 to AD15	:	Address/Data Bus	P10 to P17	:	Port 1
ASTB	:	Address Strobe	P40 to P47	:	Port 4
OE	:	Output Enable	P50 to A57	:	Port 5
LWE	:	Lower Write Enable	A16 to A19	:	Address Bus
HWE	:	Higher Write Enable	CS0-CS3	:	Chip Select
TAS	:	Turbo Access Strobe			

64-Pin LCC	64-Pin QUIP	EPROM Program Mode	Operating Mode
59	1	NC	P07 (PORT0 Input/Output)
60	2	NC	P06 (PORT0 Input/Output)
61	3	NC	P05 (PORT0 Input/Output)
62	4	NC	P04 (PORT0 Input/Output)
63	5	NC	P03 (PORT0 Input/Output)
64	6	NC	P02 (PORT0 Input/Output)
1	7	NC	P01 (PORT0 Input/Output)
2	8	NC	P00 (PORT0 Input/Output)
3	9	NC	P17 (PORT1 Input/Output)
4	10	NC	P16 (PORT1 Input/Output)
5	11	NC	P15 (PORT1 Input/Output)
6	12	NC	P14 (PORT1 Input/Output)
7	13	NC	P13 (PORT1 Input/Output)
8	14	NC	P12 (PORT1 Input/Output)
9	15	NC	P11 (PORT1 Input/Output)
10	16	NC	P10 (PORT1 Input/Output)
11	17	V_{SS} (GND)	V_{SS} (GND)
12	18	NC	P57 (PORT5 Input/Output)
13	19	A14 (Address Input)	P56 (PORT5 Input/Output)
14	20	A13 (Address Input)	P55 (PORT5 Input/Output)
15	21	A12 (Address Input)	P54 (PORT5 Input/Output)
16	22	A11 (Address Input)	P53 (PORT5 Input/Output)
17	23	A10 (Address Input)	P52 (PORT5 Input/Output)
18	24	NC	P51 (PORT5 Input/Output)
19	25	A8 (Address Input)	P50 (PORT5 Input/Output)
20	26	A7 (Address Input)	P47 (PORT4 Input/Output)
21	27	A6 (Address Input)	P46 (PORT4 Input/Output)
22	28	A5 (Address Input)	P45 (PORT4 Input/Output)
23	29	A4 (Address Input)	P44 (PORT4 Input/Output)
24	30	A3 (Address Input)	P43 (PORT4 Input/Output)
25	31	A2 (Address Input)	P42 (PORT4 Input/Output)
26	32	V_{SS} (GND)	V_{SS} (GND)
27	33	A1 (Address Input)	P41 (PORT4 Input/Output)
28	34	A0 (Address Input)	P40 (PORT4 Input/Output)
29	35	NC	NC
30	34	NC	NC
31	37	$\overline{CE}$ (CHIP ENABLE Input)	$\overline{CE}$ (CHIP ENABLE Input)
32	38	A9 (Address Input)	TMD (TURBO MODE Input)
33	39	NC	$\overline{TAS}$ (TURBO ACCESS STROBE)
34	40	NC	$\overline{HWE}$ (WRITE ENABLE Input)
35	41	NC	$\overline{LWE}$ (WRITE ENABLE Input)
36	42	$\overline{OE}$ (OUTPUT ENABLE Input)	$\overline{OE}$ (OUTPUT ENABLE Input)
37	43	NC	ASTB (ADRS LATCH ENABLE Input)
38	44	0V	$\overline{RESET}$ (reset Input)
39	45	V_{DD} (DC 5V, 6V)	V_{DD} (DC 5V)
40	46	NC	CLK (Clock Input)

64-Pin LCC	64-Pin QUIP	EPROM Program Mode	Operating Mode
41	47	V_{PP} (DC 5V, 12.5V)	V_{PP} (DC Input 5V, 12.5V)
42	48	NC	AD15 (ADDRESS/DATA MPX BUS)
43	49	NC	AD14 (ADDRESS/DATA MPX BUS)
44	50	NC	AD13 (ADDRESS/DATA MPX BUS)
45	51	NC	AD12 (ADDRESS/DATA MPX BUS)
46	52	NC	AD11 (ADDRESS/DATA MPX BUS)
47	53	NC	AD10 (ADDRESS/DATA MPX BUS)
48	54	NC	AD9 (ADDRESS/DATA MPX BUS)
49	55	NC	AD8 (ADDRESS/DATA MPX BUS)
50	56	D7 (DATA Input/Output)	AD7 (ADDRESS/DATA MPX BUS)
51	57	D6 (DATA Input/Output)	AD6 (ADDRESS/DATA MPX BUS)
52	58	D5 (DATA Input/Output)	AD5 (ADDRESS/DATA MPX BUS)
53	59	D4 (DATA Input/Output)	AD4 (ADDRESS/DATA MPX BUS)
54	60	D3 (DATA Input/Output)	AD3 (ADDRESS/DATA MPX BUS)
55	61	D2 (DATA Input/Output)	AD2 (ADDRESS/DATA MPX BUS)
56	62	D1 (DATA Input/Output)	AD1 (ADDRESS/DATA MPX BUS)
57	63	D0 (DATA Input/Output)	AD0 (ADDRESS/DATA MPX BUS)
58	64	V_{DD} (DC 5V, 6V)	V_{DD} (DC 5V

Pin Functions

Pin name	Input/Output	Function
$\overline{RESET}$	Input	– System reset signal input (active low)
$\overline{CE}$	Input	– Chip enable input pin (active low) 0: enable operation 1: disable operation and standby state (disable read/write operation but work other functions)
ASTB	Input	– Address strobe signal input pin. – ASTB latch input address (AD0 to AD15 & AD16 to AD19), TAS and TDM to on-chip pointers at its falling edge.
$\overline{OE}$	Input	– Output enable input pin (active low)
$\overline{LWE}$	Input	– Lower write enable signal input pin (active low) At 8-bit access: Low/high-byte write enable signal At 16 bit access: Low byte write enable signal
$\overline{TAS}$	Input	– Turbo acces strobe signal input pin – $\overline{TAS}$ specify the operating mode when ASTB is high. – Enable/disable access operations by input level, after ASTB.
TMD	Input	– Turbo mode signal input pin. – TMD specify the operation mode when ASTB is high.
AD0-AD15	Input/Output	– Address/Data multiplexed bus
P00-P07	Input/Output	– 8 bit programmable input/output port
A16-A19	Input	– Address input by mode control
CS0-CS3	Output	– 4 bit chip select output by mode control
P10-P17	Input/Output	– 8 bit bit programmable input/output port

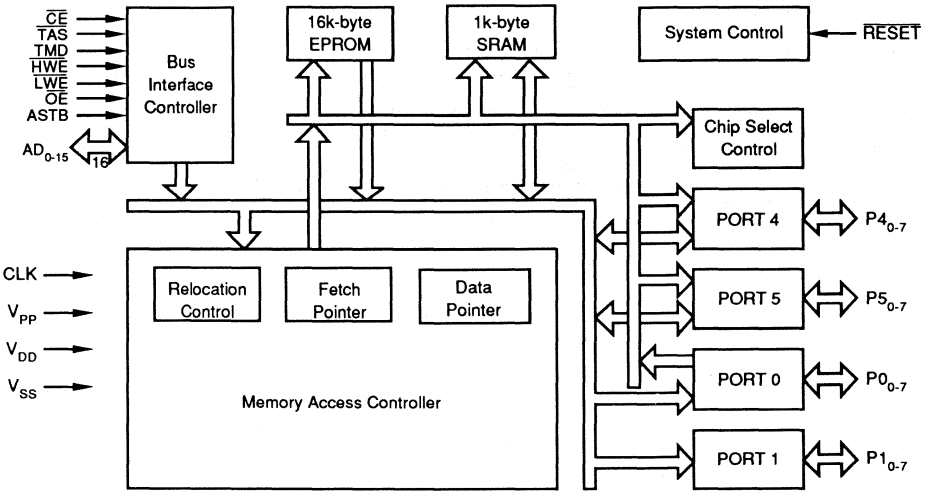
Pin Functions (cont'd)

Pin name	Input/Output	Function
P40-P47	Input/Output	– 8 bit byte programmable input/output port – Output lower-byte address held on the chip by mode control
P50-P57	Input/Output	– 8 bit bit programmable Input/Output port – Output higher-byte address held on the chip by mode control
CLK	Input	– System clock input pin – In the operating mode not used CLK fixed to high level
V_{DD}	—	– Power supply pin (positive)
V_{PP}	—	– Power supply pin (positive)
V_{SS}	—	– Ground potential pin

PROM Programming Mode

Pin name	Input/Output	Function
$\overline{RESET}$	Input	PROM mode setting pin. $\overline{RESET}$=0
A0 to A14	Input	Address input pins
D0 to D7	Input/Output	Data input/output pins
$\overline{CE}$	Input	Chip Enable signal input pin
$\overline{OE}$	Input	Output Enable signal input pin
V_{PP}	Input	High-voltage application pin for program writing/verifying
V_{DD}	—	Positive power supply pin
V_{SS}	—	Ground potential pin
Others	—	Forced to "0" via a resistor

Block Diagram



Absolute Maximum Ratings

Ta = 25°C

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5 to +7.0	V
	V_{PP}		-0.5 to +13.5	V
Input Voltage	V_{I1}	Except TMD/A9 pin	-0.5 to V_{DD}+0.5	V
	V_{I2}	TMD/A9 pin	-0.5 to +13.5	V
Output Voltage	V_O		-0.5 to V_{DD}+0.5	V
Output Current Low	I_{OL}	All output pins	4.0	mA
		Total for all output pins	100	mA
Output Current High	I_{OH}	All output pins	-2.0	mA
		Total for all output pins	-50	mA
Operating Temperature	T_{opt}		-10 to +70	°C
Storage Temperature	T_{stg}		-65 to +150	°C

Capacitance (Ta=25°C,V_{DD}=V_{SS}=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f=1MHz pins not used for measurement are at 0V.			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	C_{IO}				20	pF

DC Characteristics
Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL1}	Except $\overline{RESET}$, CLK, $\overline{TAS}$	0		0.8	V
	V_{IL2}	$\overline{RESET}$	0		0.2 V_{DD}	V
	V_{IL3}	CLK, $\overline{TAS}$	0		0.25 V_{DD}	V
Input Voltage high	V_{IH1}	Except $\overline{RESET}$, CLK, $\overline{TAS}$	2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$	0.8 V_{DD}		V_{DD}	V
	V_{IH3}	CLK, $\overline{TAS}$	0.75 V_{DD}		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL}= 2.0 mA			0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -1.0 mA	V_{DD} -1			V
	V_{OH2}	I_{OH} = -100 mA	V_{DD} -0.5			V
Input Leakage Current	I_{LI}	$0V \le V_I \le V_{DD}$			±10	μA
Output Leakage Current	I_{LO}	$0V \le V_O \le V_{DD}$			±10	μA
V_{DD} supply current	I_{DD1}	Operation Mode		40		mA
	I_{DD2}	Standby Mode		1		μA
V_{PP} supply current	I_{PP}	Operating Mode		1		μA

AC Characteristics
Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
CLK Cycle time	t_{CYK1}	1 CLK MODE (14MHz)	71			ns
	t_{CYK2}	2 CLK MODE (16MHz)	61			ns
CLK low-level width	t_{WKL}		22			ns
CLK high-level width	t_{WKH}		22			ns
CLK rise time	t_{KR}				10	ns
CLK fall time	t_{KF}				10	ns
ASTB high-level width	t_{WASH}		13			ns
CLK ↑ → ASTB	t_{DKAS}		3			ns
ASTB ↓ → ↑ CLK	t_{SASK1}	1 CLK MODE	20			ns
	t_{SASK2}	2 CLK MODE	5			ns
Address set-up time (from ASTB ↓)	t_{SIAAS}		7			ns
Address set-up time (to CLK ↑)	t_{SIAK1}	1 CLK MODE	35			ns
	t_{SIAK2}	2 CLK MODE	20			ns
Address hold time (from ASTB ↓)	t_{HASIA}		15			ns
Data output delay time (from CLK ↓)	t_{DKOD}	C_L = 100pF	35			ns

AC Characteristics (cont'd)
Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Data output delay time (from $\overline{OE}$ ↓)	t_{DOEOD}	CL = 100pF	35			ns
$\overline{OE}$ set-up time (from CLK ↑)	t_{SOEK}		5			ns
Data hold time (from CLK ↓)	t_{HKOD}	CL = 100pF	5			ns
Data hold time (from $\overline{OE}$ ↑)	t_{HOEOD}	CL = 100pF	5			ns
$\overline{OE}$ ↑ → ASTB ↑	t_{DOEAS}		10			ns
$\overline{TAS}$ set-up time (to ASTB ↓)	t_{STSAS}		10			ns
$\overline{TAS}$ hold time (from CLK ↓)	t_{HKTS}		8			ns
$\overline{TAS}$ set-up time (to CLK ↓)	t_{STSK}		30			ns
$\overline{OE}$ ↑ → $\overline{TAS}$ ↓	t_{DOETS}		10			ns
TMD set-up time (to ASTB ↓)	t_{STMAS}		10			ns
TMD hold time (to CLK ↑)	t_{HKTM}		8			ns
TMD set-up time (to CLK ↑)	t_{STMK}		30			ns
$\overline{CE}$ set-up time (to CLK ↑)	t_{SCEK}		50			ns
$\overline{CE}$ hold time (to CLK ↓)	t_{HKCE1}		20			ns
	t_{HKCE2}		20			ns
Port data hold time (from address input)	t_{HIAOA}	Address output C_L= 100pF	5			ns
Port data output time (from address input)	t_{DIAOA}	Address output C_L= 100pF	50			ns
Port data hold time (from CLK ↓)	t_{HKOA}	Address output C_L= 100pF	5			ns
Port data output time (from CLK ↓)	t_{DKOA}	Address output	40			ns
Port data hold time (from address input)	t_{HIACS}	Chip select output	5			ns
Port data hold time (from address input)	t_{DIACS}	Chip select output C_L= 50pF	70			ns
Port data hold time (to CLK ↓)	t_{HKCS}	Chip select output C_L= 50pF	5			ns
Port data output time (to CLK ↓)	t_{DKCS}	Chip select output C_L=50pF	35			ns
ASTB ↓ → $\overline{HWE}$/$\overline{LWE}$ ↓	t_{DASWE}		20			ns
$\overline{HWE}$/$\overline{LWE}$ set-up time (to CLK ↑)	t_{SWEK1}		5			ns
	t_{SWEK2}		30			ns
$\overline{HWE}$/$\overline{LWE}$ hold time (from CLK ↓)	t_{HKWE}		5			ns
Write data set-up time (to CLK ↓)	t_{SIDK}		40			ns
Write data hold time (from CLK ↓)	t_{HKID}		5			ns
$\overline{HWE}$/$\overline{LWE}$ ↑ → ASTB ↑	t_{DWEAS}		10			ns
$\overline{HWE}$/$\overline{LWE}$ ↑ → $\overline{TAS}$ ↓	t_{DWETS}		10			ns
Address input → data output	t_{DIAOD}	C_L= 100pF	140			ns

AC Characteristics (cont'd)
Ta=-10°C to +70°C, V_{DD}=5.0V±10%, V_{ss}=0V

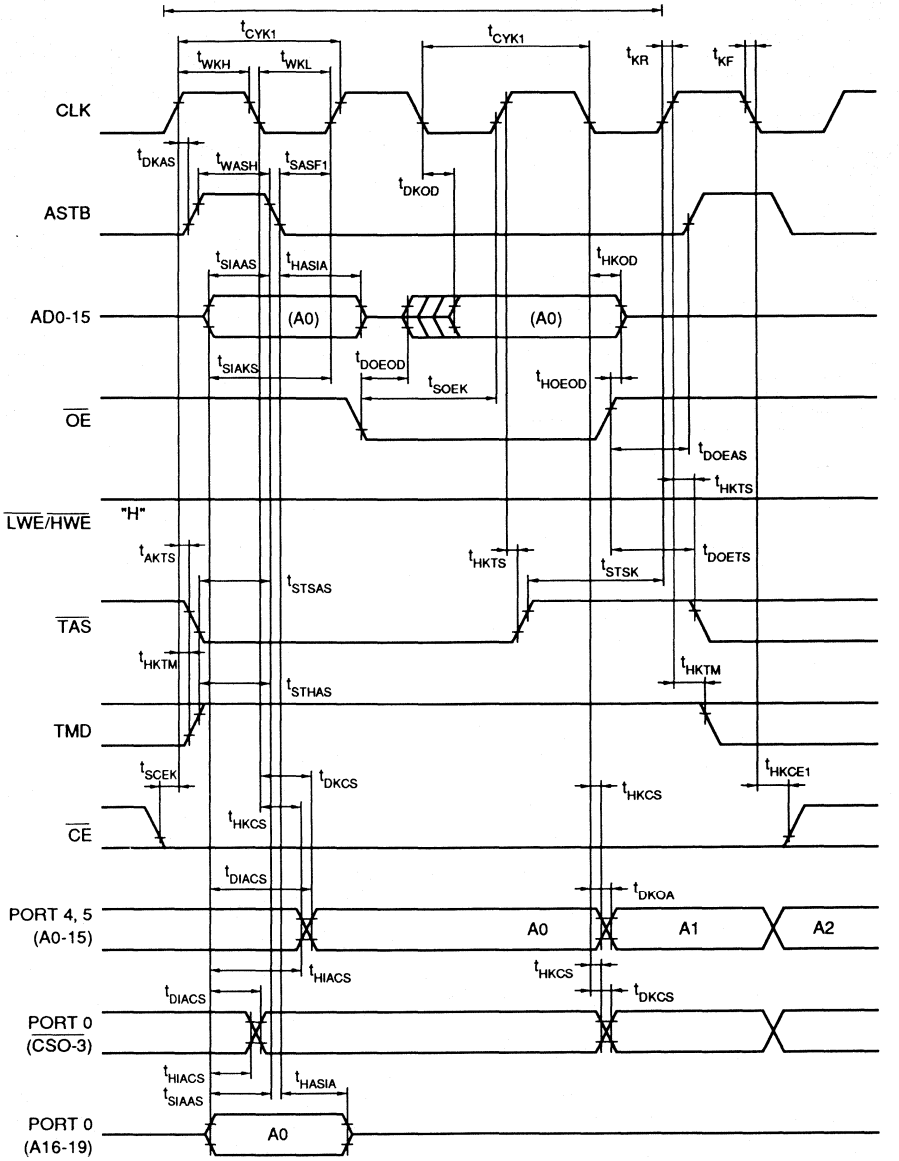
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
$\overline{OE}$ low-level width	t_{WOEL}		40			ns
$\overline{CE}$ set-up time (to ASTB ↓)	t_{SCEAS}		100			ns
$\overline{CE}$ hold time (from $\overline{OE}$ ↑)	t_{HOECE}		20			ns
HWE/LWE low-level width	t_{WWEL}		40			ns
Write data set-up time (to HWE/LWE ↑)	t_{SIDWE}		40			ns
Write data hold time (to HWE/LWE ↑)	t_{HWEID}		10			ns
$\overline{CE}$ hold time (from $\overline{HWE}$/$\overline{LWE}$ ↑)	t_{HWECE}		20			ns
TMD hold time (from $\overline{HWE}$/$\overline{LWE}$ ↑)	t_{HWETM1}		20			ns
	t_{HWETM2}		20			ns
$\overline{RESET}$ low-level width	t_{WRESL}		500			ns
$\overline{RESET}$ high-level width	t_{WRESH}		500			ns

2

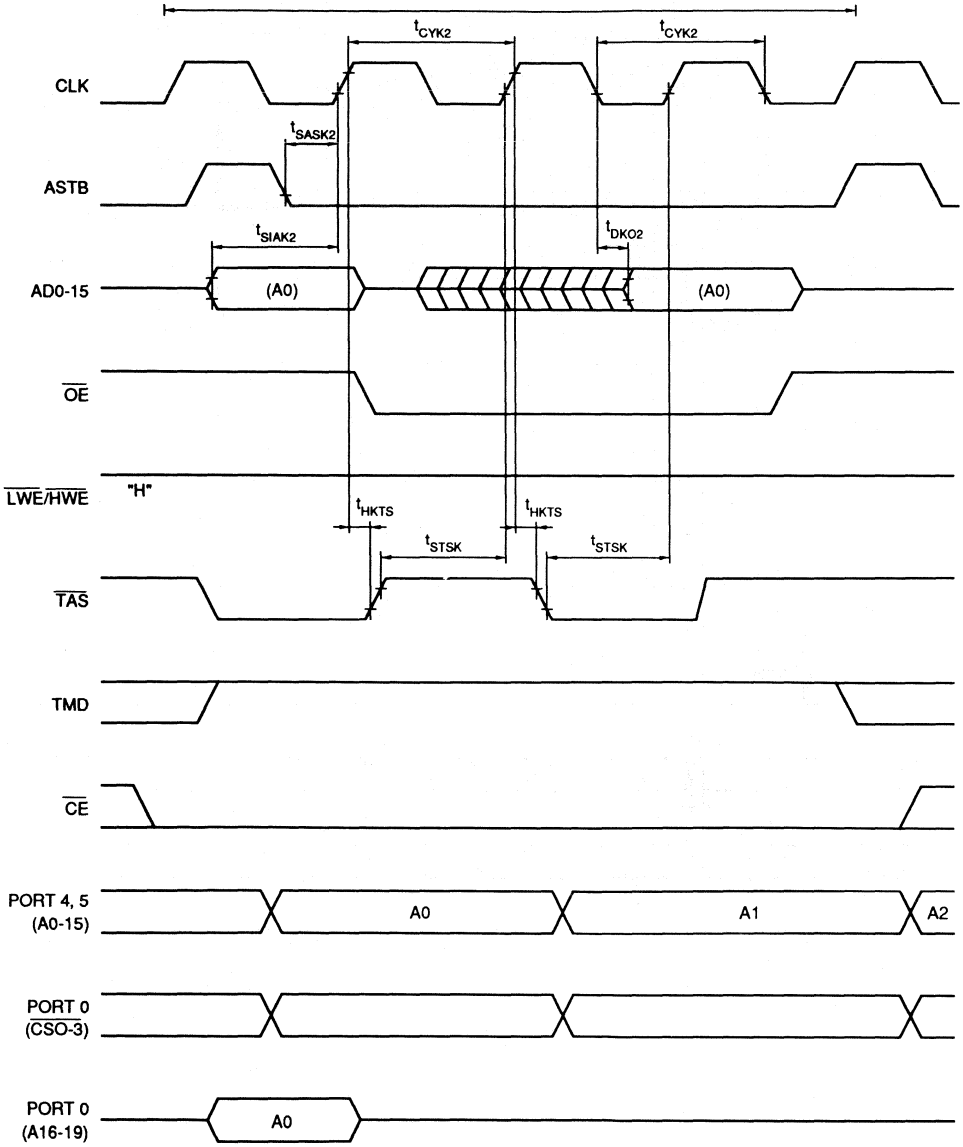
Timing Waveforms

Normal Opcode Fetch Timing

(1-clock mode, no-wait)

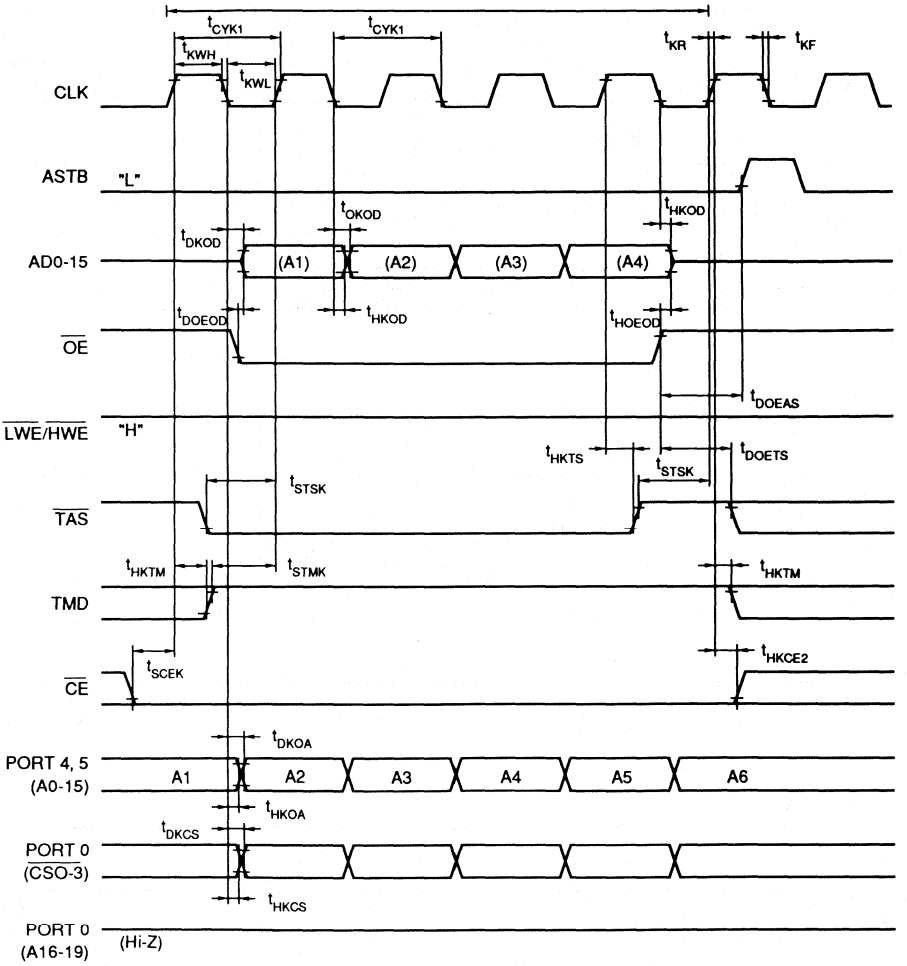


Normal Opcode Fetch Timing
(2-clock mode, 1-wait)

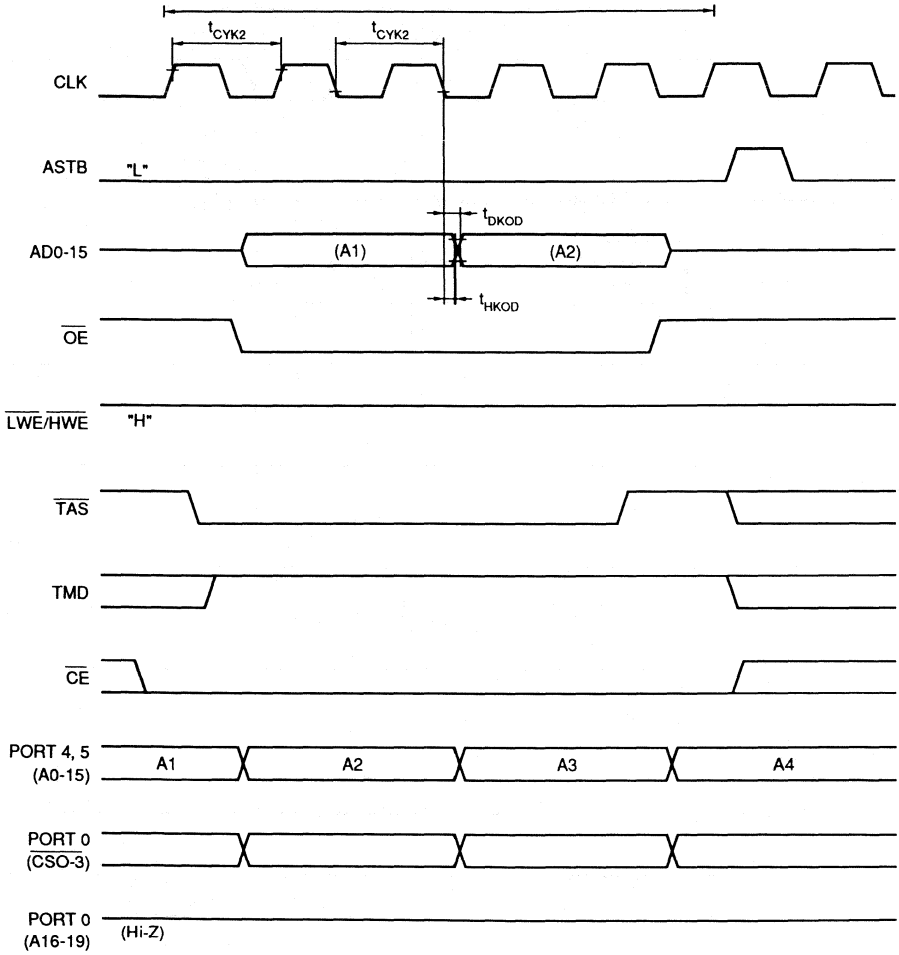


The specification except above ones is referred to the normal opcode fetch mode (1-clock mode).

High-Speed Opcode Fetch Mode Timing
(1-clock mode)

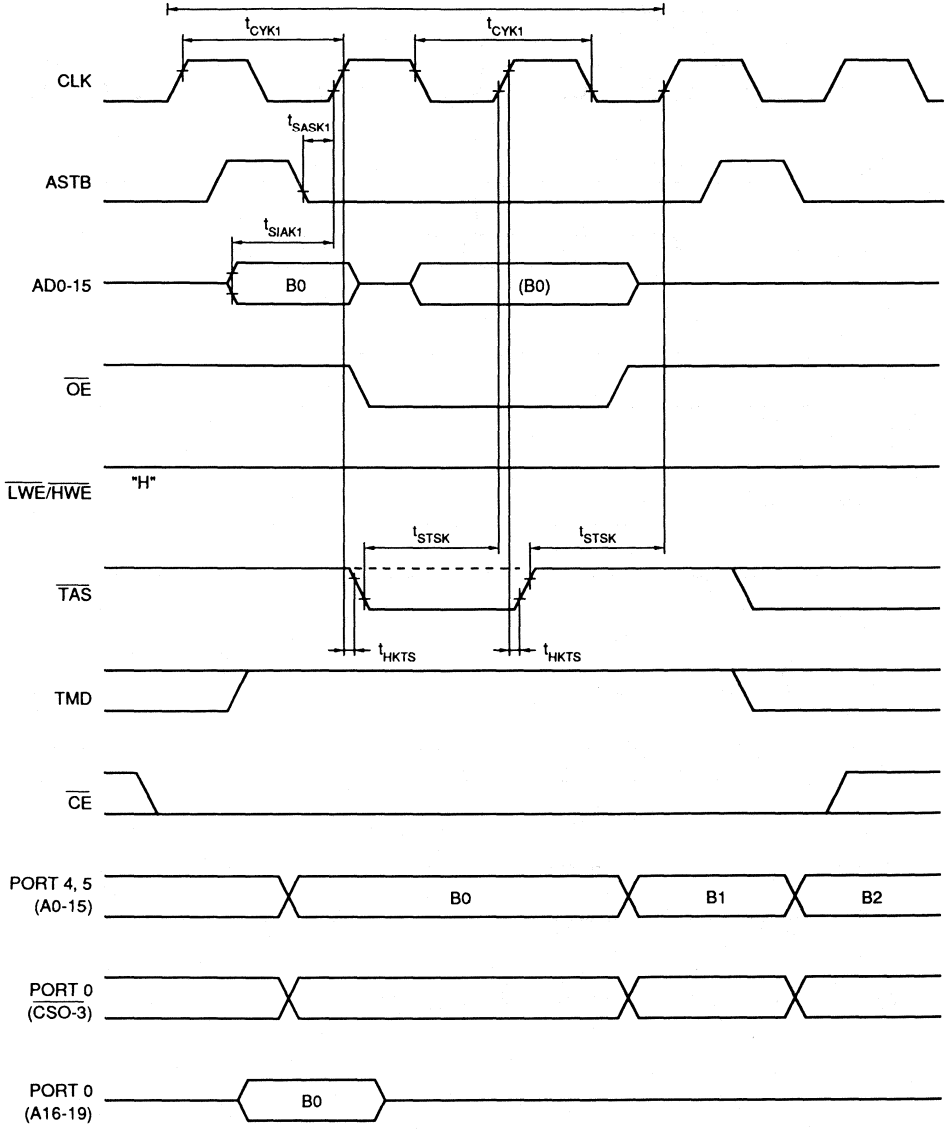


High-Speed Opcode Fetch Mode Timing
(2-clock mode)



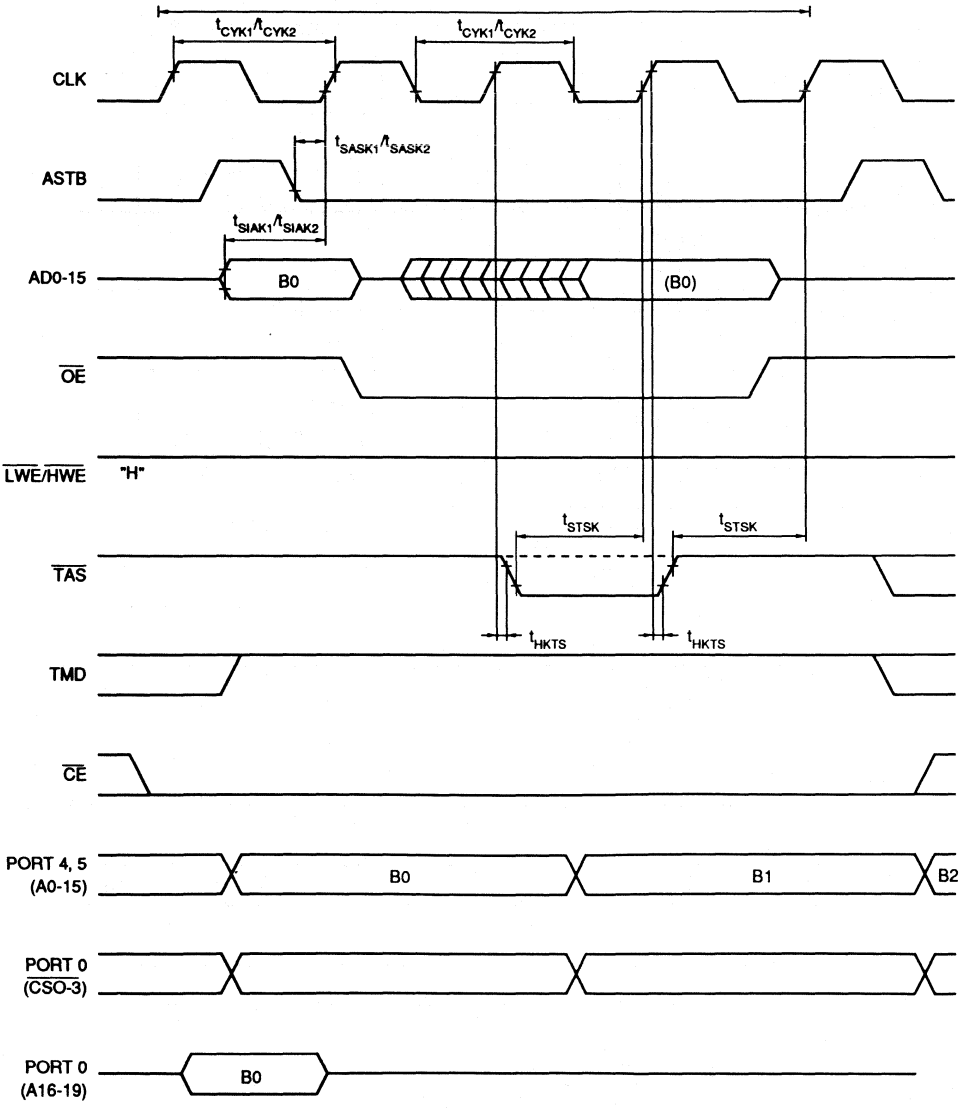
The specification except above ones is referred to the high-speed opcode fetch mode (1-clock mode).

Normal Data Read Mode Timing
(1-clock mode, no-wait)



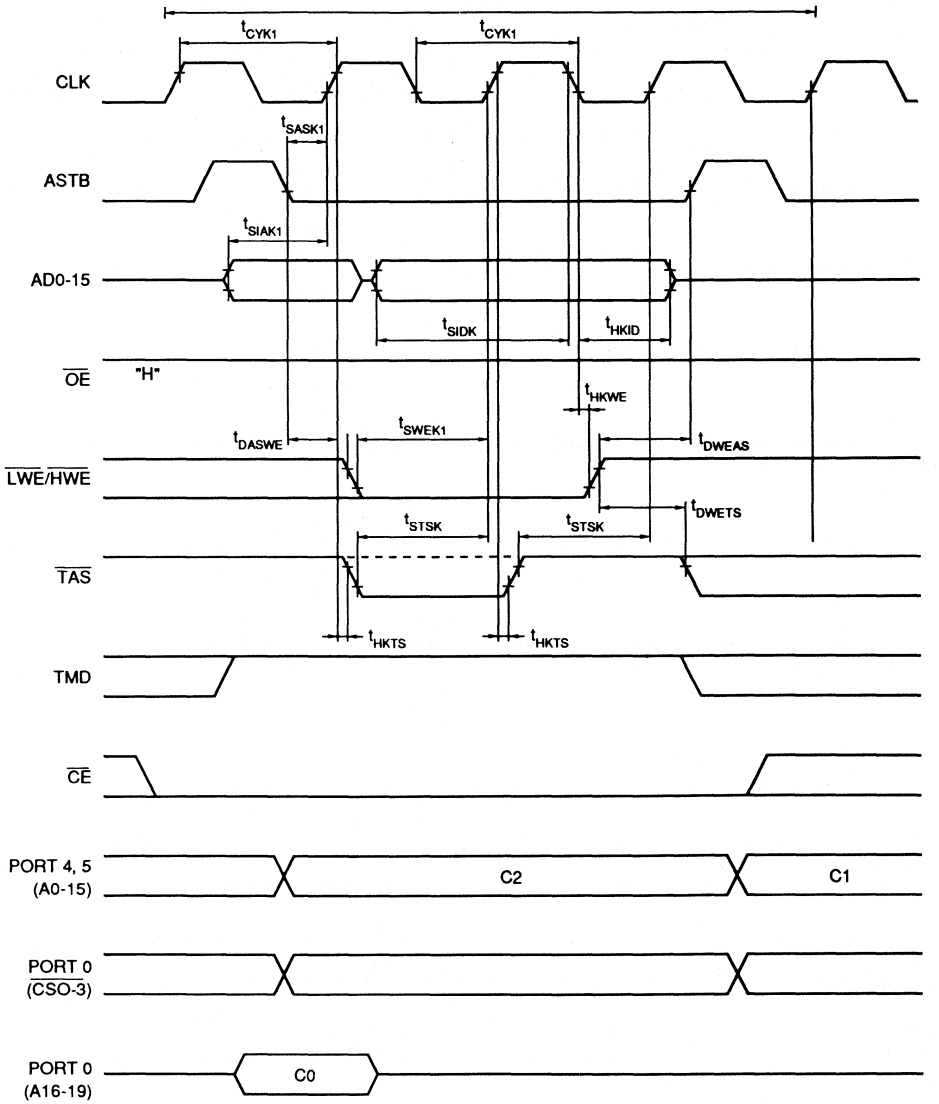
The specification except above ones is referred to the normal opcode fetch mode

Normal Data Read Mode Timing
(1-clock mode, 1-wait / 2-clock mode, 1-wait)



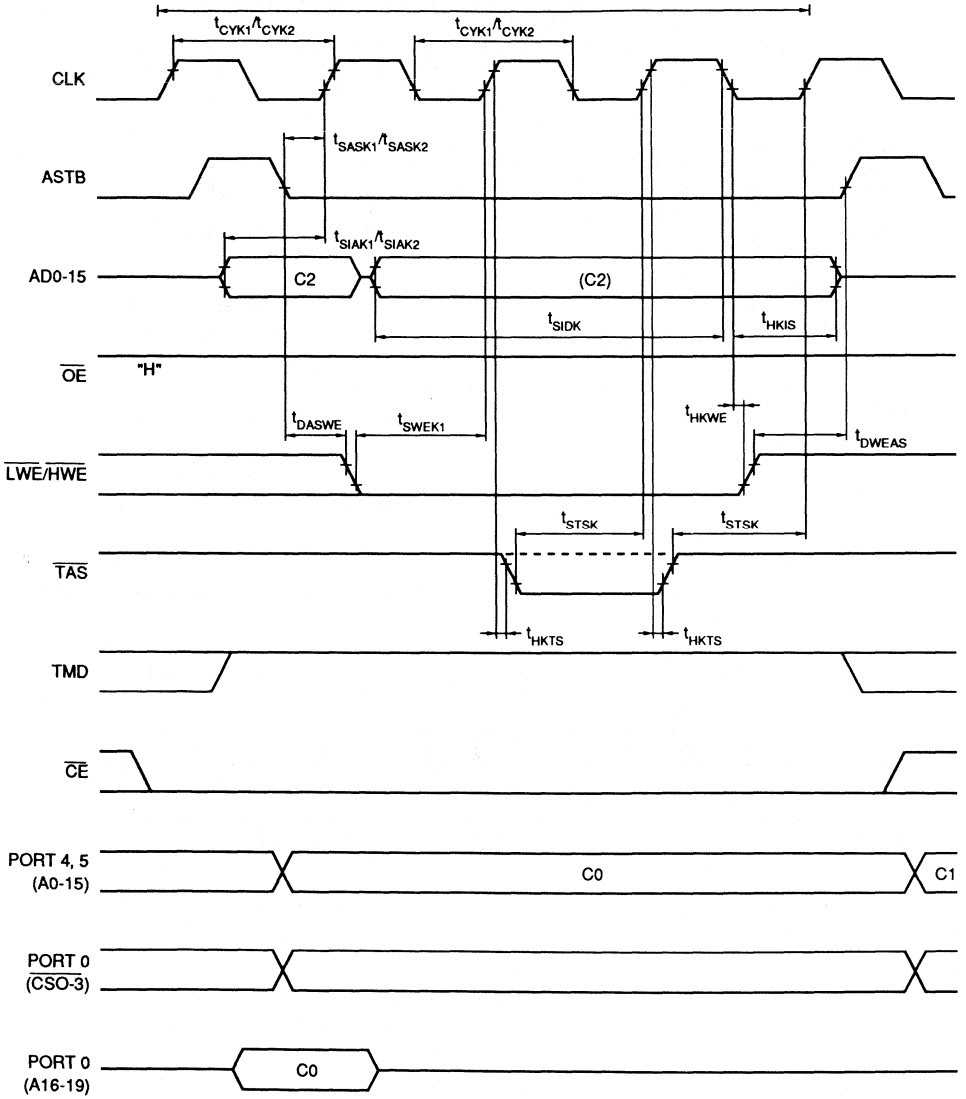
The specification except above ones is referred to the normal opcode fetch mode

Normal Data Write Mode Timing
(1-clock mode, no-wait)



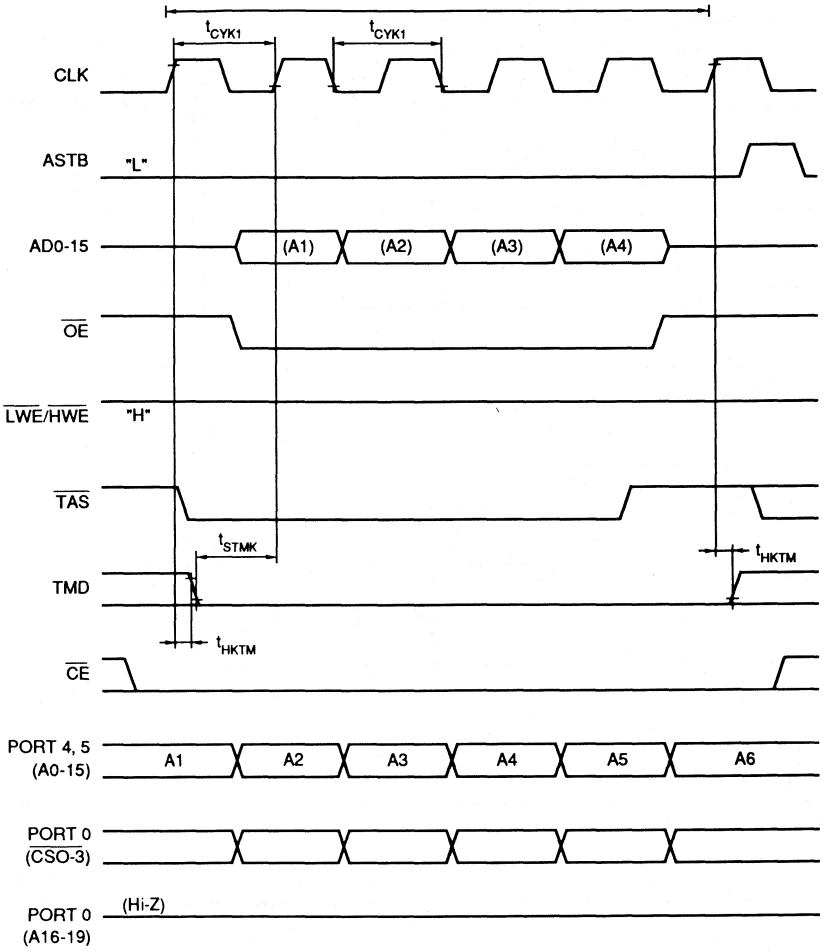
The specification except above ones is referred to the normal opcode fetch mode.

Normal Data Write Mode Timing
(1-clock mode, 1-wait / 2-clock mode, 1-wait)



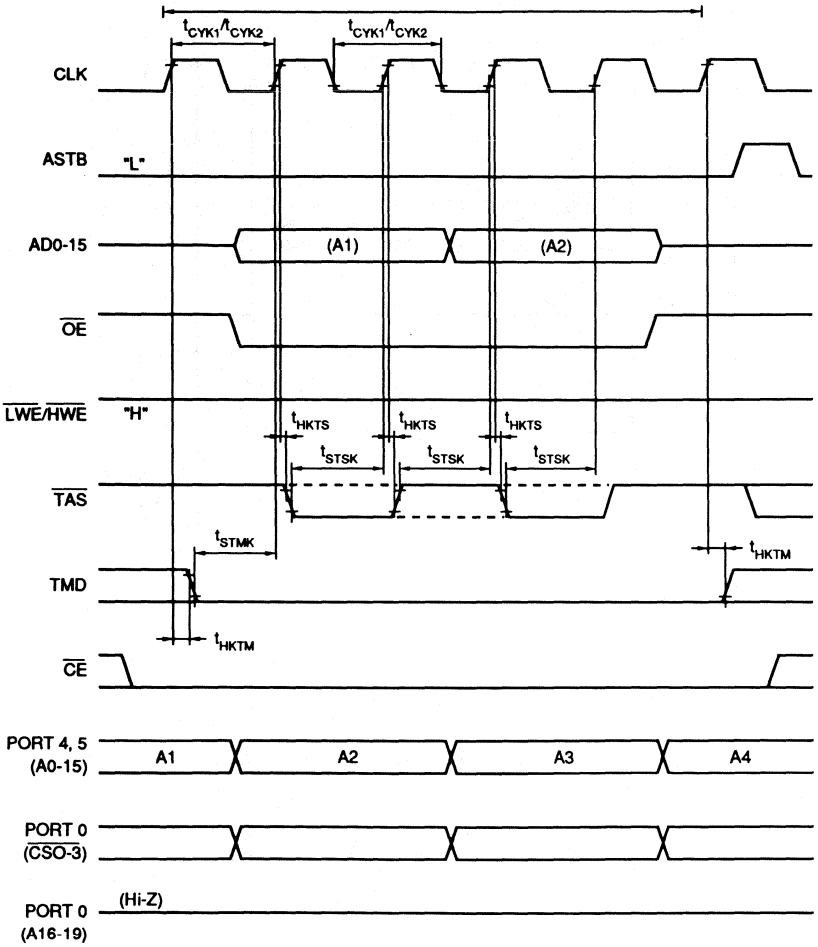
The specification except above ones is referred to the normal opcode fetch mode.

High-Speed Data Read Mode Timing
(1-clock mode, no-wait)



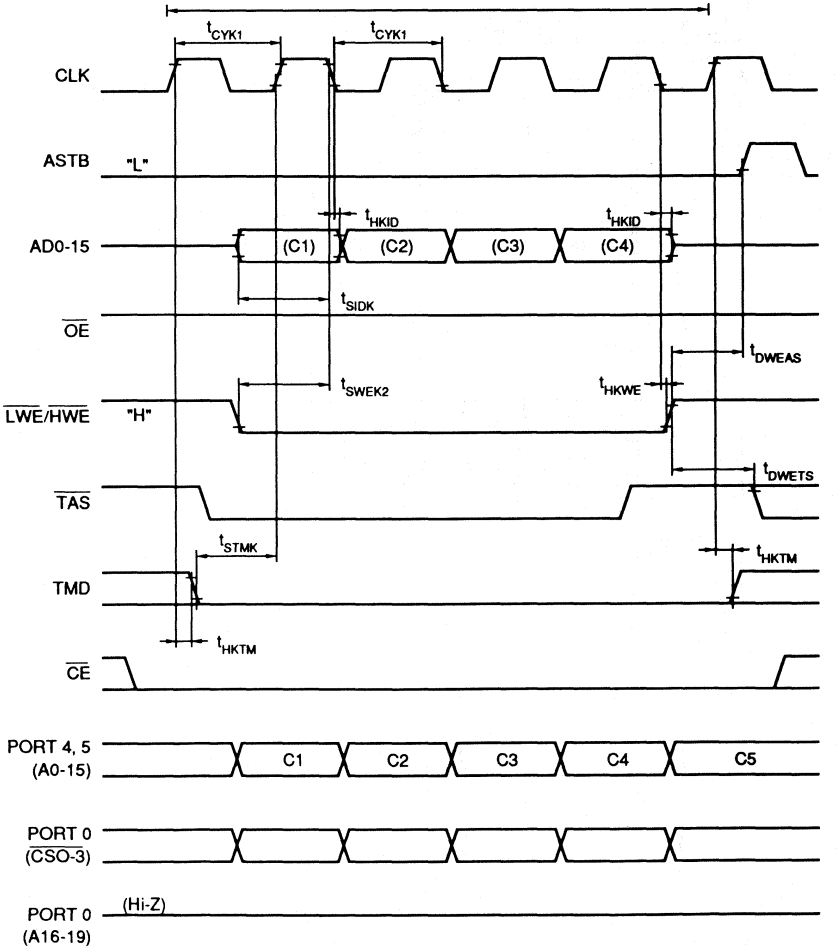
The specification except above ones is referred to the high-speed opcode fetch mode.

High-Speed Data Read Mode Timing
(1-clock mode, 1-wait / 2-clock mode, 1-wait)



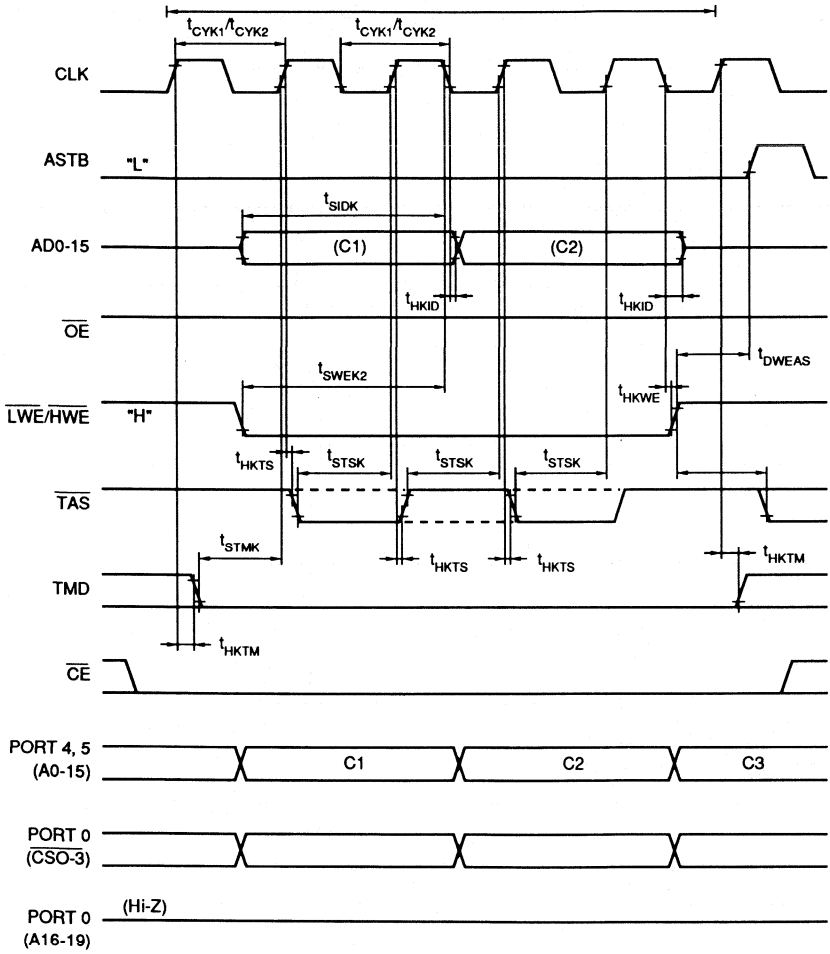
The specification except above ones is referred to the high-speed opcode fetch mode.

High-Speed Data Write Mode Timing
(1-clock mode, no-wait)



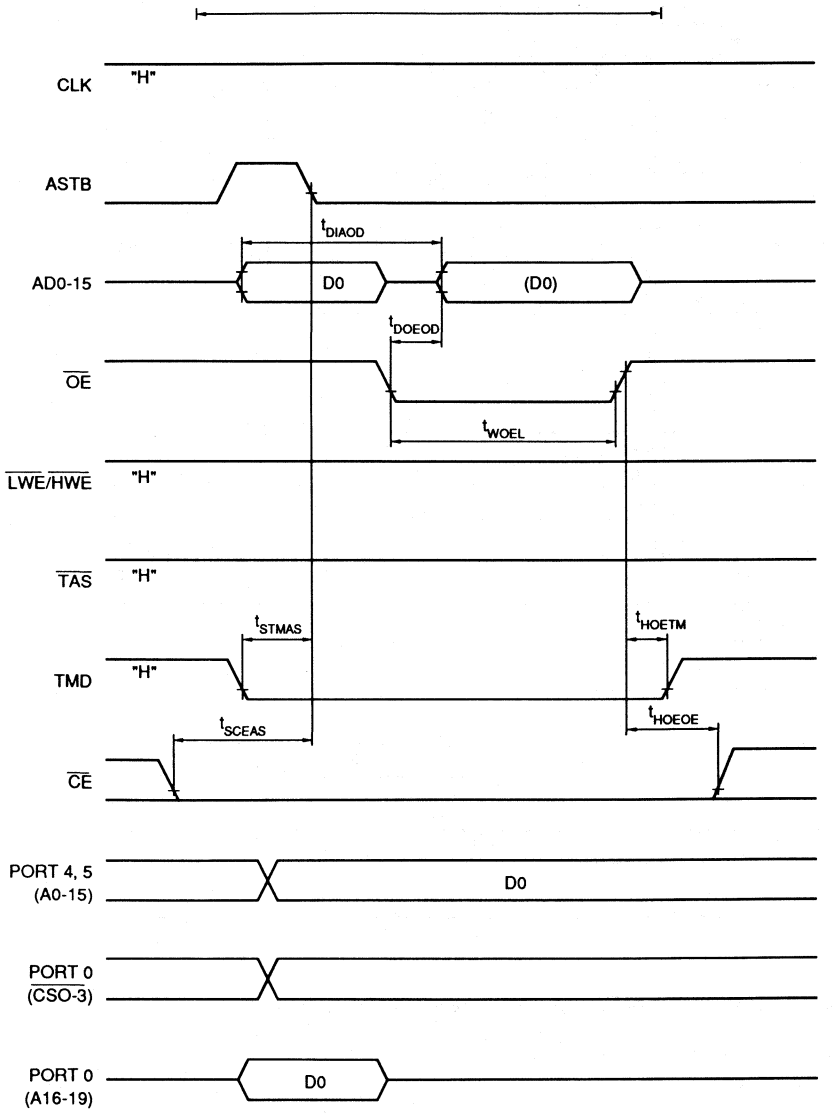
The specification except above ones is referred to the high-speed opcode fetch mode.

High-Speed Data Write Mode Timing
(1-clock mode, 1-wait / 2-clock mode, 1-wait)



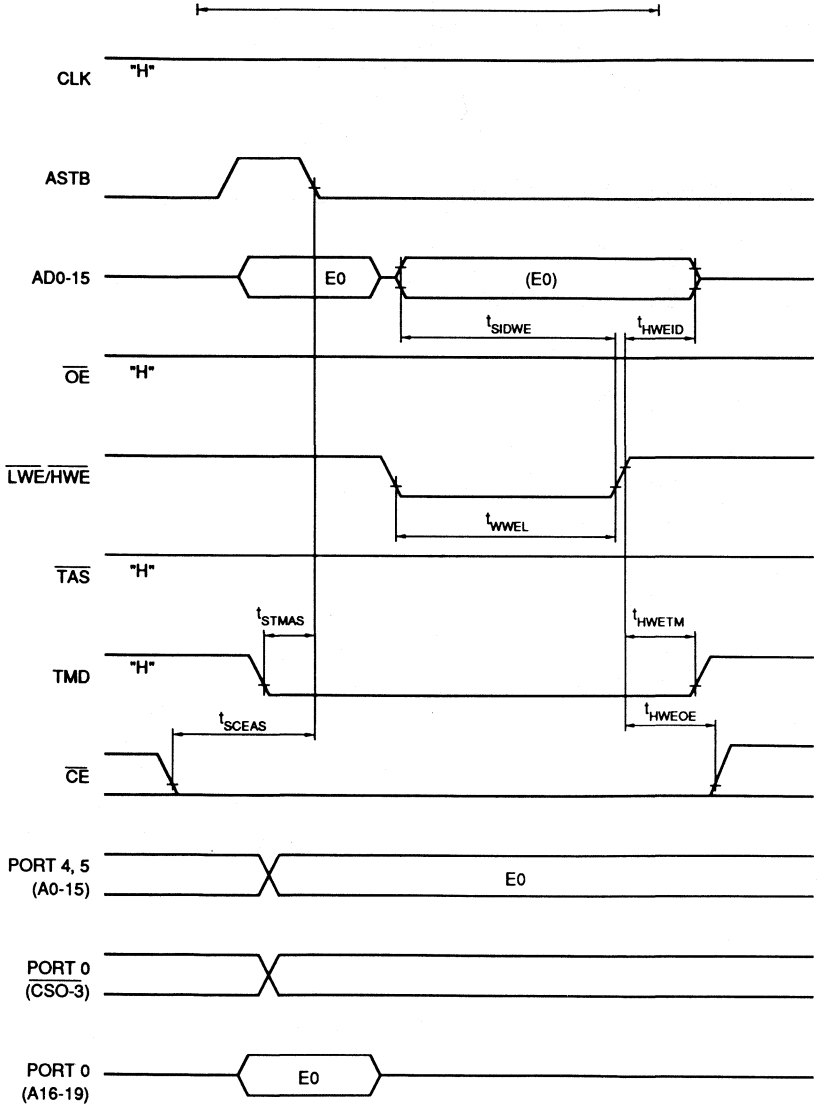
The specification except above ones is referred to the high-speed opcode fetch mode.

Non-Clock Normal Data Read Timing



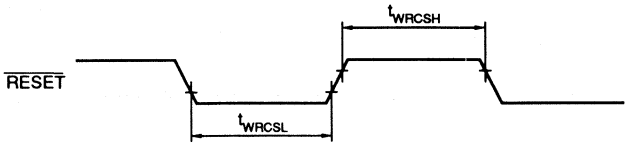
The specification except above ones is referred to the normal opcode fetch mode.

Non-Clock Normal Data Write Timing

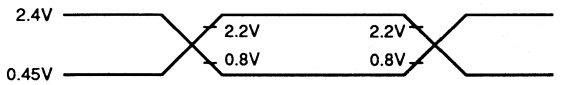


The specification except above ones is referred to the normal opcode fetch mode.

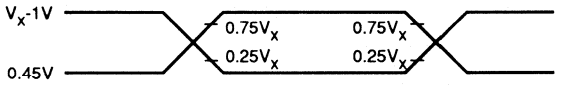
Others



AC Test Input/Output Wave-Forms (Except CLK, $\overline{RESET}$, $\overline{TAS}$)



AC Test Input/Output Wave-Forms (CLK, $\overline{TAS}$)



DC Programming Characteristics
($Ta = 25°C \pm 5°C$, $V_{IP} = 12.0V \pm 0.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Symbol*	Test Conditions	Min.	Typ.	Max.	Unit
Input Voltage High	V_{IH}	V_{IH}		2.2		$V_{DDP}+0.3$	V
Input Voltage Low	V_{IL}	V_{IL}		-0.3		0.8	V
Input Leakage Current	I_{LIP}	I_{LI}	$0 \le V_I \le V_{DDP}$			10	μA
Output Voltage High	V_{OH}	V_{OH}	$I_{OH} = -400$ μA	2.4			V
Output Voltage Low	V_{OL}	V_{OL}	$I_{OL} = 2.0$ mA			0.45	V
Input current	V_{A9}		TMD/A9 pin			±10	μA
Output Leakage Current	I_{LO}		$0 \le V_O \le V_{DDP}$, $\overline{OE} = V_{IH}$			10	μA
PROG Pin High-Voltage Input Current	I_{IP}					±10	μA
V_{DDP} Supply Voltage	V_{DDP}	V_{DD}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	$V_{PP} = V_{DDP}$			V
I_{DDP} Supply Current	I_{DD}	I_{DD}	Program memory write mode		10	30	mA
			Program memory read mode $\overline{CE} = V_{IL}$, $V_I = V_{IH}$		10	30	mA
I_{PP} Supply Current	I_{PP}	I_{PP}	Program memory write mode $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		10	30	mA
			Program memory read mode		1	100	μA

* Symbol of the corresponding μPD27C256A

2

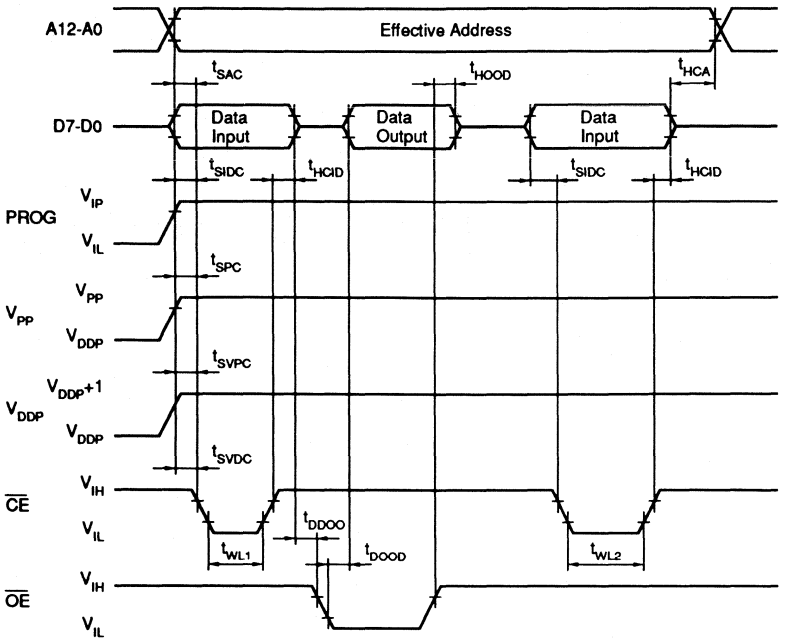
AC Programming Characteristics

(Ta = 25°C ±5°C, V_{IP} = 12.0V ±0.5V, V_{SS} = 0V)

Parameter	Symbol	Symbol*	Test Conditions	Min.	Typ.	Max.	Unit
Address Setup Time (to $\overline{CE}\downarrow$)	t_{SAC}	t_{AS}		2			μs
$\overline{OE}\downarrow$ Delay Time from Data	t_{DDOO}	t_{OES}		2			μs
Input Data Setup Time (to $\overline{CE}\downarrow$)	t_{SIDC}	t_{DS}		2			μs
Address Hold Time (from $\overline{CE}\uparrow$)	t_{HCA}	t_{AH}		2			μs
Input Data Hold Time (from $\overline{CE}\uparrow$)	t_{HCID}	t_{DH}		2			μs
Output Data Hold Time (from $\overline{OE}\uparrow$)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} Setup Time (to $\overline{CE}\downarrow$)	t_{SVPC}	t_{VPS}		2			μs
V_{DDP} Setup Time (to $\overline{CE}\downarrow$)	t_{SVDC}	t_{VDS}		2			μs
Initial Program Pulse Width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Additional Program Pulse Width	t_{WL2}	t_{OPW}		2.85		78.75	ms
PROG High-Voltage Input Setup Time (to $\overline{CE}\downarrow$)	t_{SPC}			2			μs
Data Output Time from Address	t_{DAOD}	t_{ACC}	$\overline{OE} = V_{IL}$			2	μs
Data Output Time from $\overline{OE}\downarrow$	t_{DOOD}	t_{OE}				1	μs
Data Hold Time (from $\overline{OE}\uparrow$)	t_{HCOD}	t_{DF}		0		130	ns
Data Hold Time (from Address)	t_{HAOD}	t_{OH}	$\overline{OE} = V_{IL}$	0			ns

* Symbol of the corresponding μPD27C256A

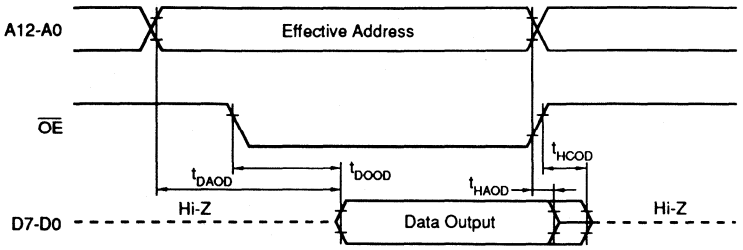
PROM Write Mode Timing



Note: 1: Ensure that V_{DDP} is applied before V_{PP} and is cut off after V_{PP}.

2: Ensure that V_{PP} does not reach +13 V or above, including overshoot.

PROM Read Mode Timing



Section 3: The μCOM87 Family

Section 3 – The μCOM87 Family

SINGLE CHIP 8-BIT MICROCOMPUTER ROM-LESS DEVELOPMENT DEVICE IN CMOS TECHNOLOGY

DESCRIPTION

The μPD78C05A is a high-performance 8-bit microcomputer fabricated with CMOS technology. The μPD78C05A contains an 8-bit ALU, a 128 x 8 RAM, two 8-bit I/O ports, a 6-bit I/O port, an 8-bit timer/event counter with 4-bit prescaler, a serial I/O port, and three (two external and one internal) source vectored interrupt structure. It also contains a 16-bit Address bus and an 8-bit data bus for external memory (program memory, data memory, or memory mapped I/O) up to 64K bytes.

The μPD78C05A has stand-by capability (STOP/HALT) for its power-down.

The μPD78C05A is applicable for hand-held computer, etc. requiring low power consumption.

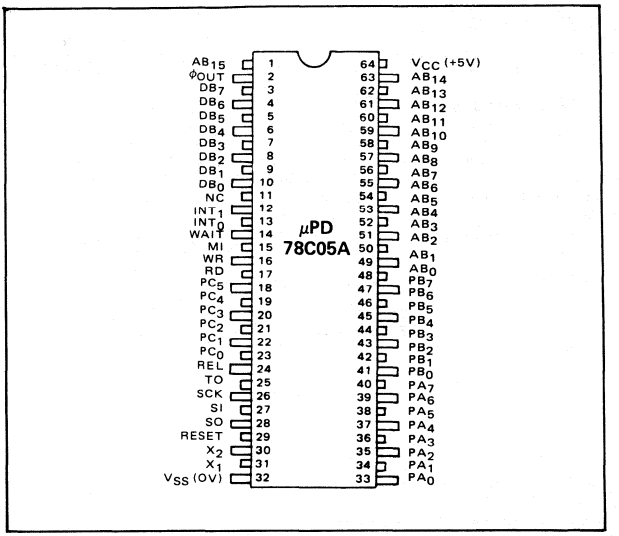
The μPD78C05A is compatible with the μPD78C06A (μCOM-87LC-family) and used as evaluation chip for μCOM-87LC-series.

FEATURES

- Powerful 101 Instructions
- Instruction Cycle Time: 2,6 μs for 78C05A,
- Data Memory: 128W x 8
- Direct Addressing Capability up to 64kB External Memory
- Powerful Addressing Modes Capability
- Multi-level Stack
- Vectored Interrupts (External: 2, Internal: 1)
- On-chip 8-bit Timer with 4-bit Prescaler
- 30 I/O Ports
- Serial I/O Ports
- Stand-by Capability (STOP/HALT mode)
- Fully Bus Compatible with 8080A
- On-chip Clock Generator with 6 MHz crystal
- Single Supply, CMOS Technology
- Low Power Consumption
- 64 pin QUIP
- μPD78C06A Evaluation chip

3

PIN CONFIGURATION



ORDERING INFORMATION

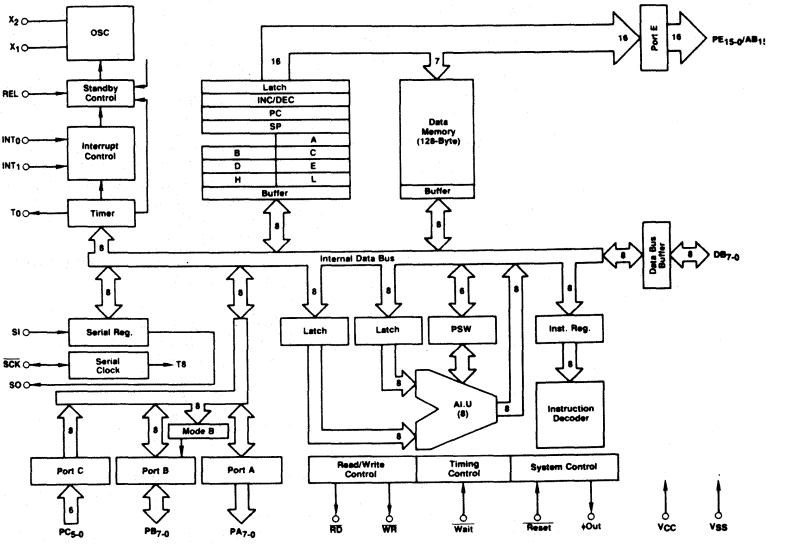
PART NUMBER	PACKAGE TYPE	ROM
μPD78C05AG-36	64-PIN QUIP	ROM-Less

NOTE: QUIP = QUAD IN LINE, SDIP = SHRINKED DUAL IN LINE,
FLAT = FLAT PACKAGE (SMD)

PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
1, 49-63	AB_0-AB_{15}	(Output), 16 bit address bus and output port.
2	ϕOUT	(Output) The clock of system clock frequency (1/4 of crystal frequency or X_1 external clock frequency) is placed out from this line. It is still placed out in HALT mode, but it is fixed to high in STOP mode.
3-10	DB_7-DB_0	(Tri-State Input/Output) This is an 8-bit bi-directional data bus. The data move between an external memory or I/O STOP, and accumulator is done through this data bus. During an input, HALT, and RESET, the output of the data bus goes a high impedance state. Input/Output level are TTL compatible.
12	INT_0	(Input) It is a level-sensitive interrupt input line which is high level active.
13	INT_1	(Input) It is a rising-edge sensitive interrupt line, and it becomes valid when INT_1 input goes low to high. Subsequently, if users want to perform another interrupt on this line after an interrupt on this line is accepted, they must take it into consideration that INT_1 input should be maintained at low state a little while, and then it should go high. Unless, it does not enable another interrupt.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state T_W and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-23	PC_0-PC_5	(Input) This is a 6-bit input port with pull-up resistors. Input data to this port can be test by test instruction, and also moved to least significant 6-bit of accumulator. Input level is CMOS compatible. This port is fit for key-input port.
24	REL	(Input) This is an input to release the STOP mode of stand-by function. STOP mode is released by raising the REL input high, then clock generator which has been stopped will restart. During REL input is high, the bit 3 of Stand-by Control Register (SC3) is set to one, and it is reset to zero after REL signal returns low. Pull-down resistor is built in.
25	TO	(Output) The square wave is output from this line. Its cycle time is half of a count time of the internal timer. It goes on low level after reset.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD78C05A
30	X_2	(Output) Oscillator output.
31	X_1	(Input) Clock Input
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

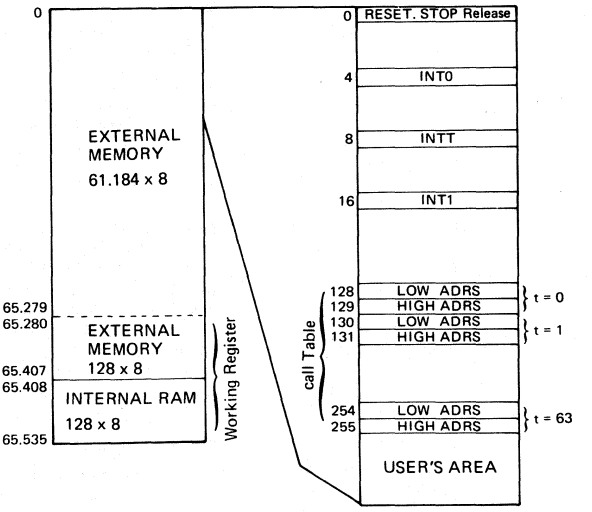
BLOCK DIAGRAM



Memory Map

The μPD78C05A can directly address the memory up to 64k bytes. Except on-chip RAM (65.408-65.535) any memory location can be used as either of RAM or ROM, freely. The memory map of the μPD78C05A is shown on the next page. In the specific memory area, the Reset/Stop mode Restart Address, Interrupt Start Address, Call Table etc. are involved. External memory (ROM), and/or working registers, freely.

FUNCTIONAL DESCRIPTION



HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH 4K ROM IN CMOS TECHNOLOGY

DESCRIPTION

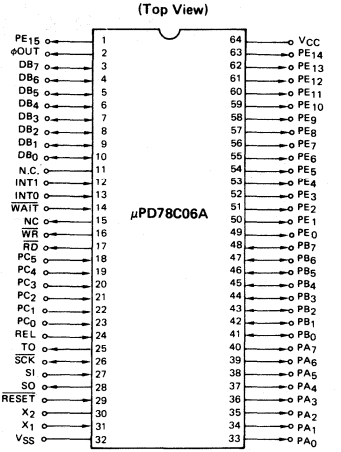
The NEC μPD78C06A is a general purpose single-chip microcomputer. The μPD78C06A is fabricated with CMOS technology.

This contains the functional blocks of program memory, data memory, ALU, I/O ports, on-chip timer, serial I/O and internal clock generator. It can extend external memory capacity (ROM, RAM) up to 60k bytes.

FEATURES

- Single-chip Microcomputer (μCOM-87LC)
- Powerful 101 Instructions
- Instruction Cycle Time: 4 μs (on-chip ROM); 2,6 μs (external memory & on-chip RAM) } for 78C06A
- Program Memory (ROM): 4096W x 8
- Data Memory (RAM): 128W x 8
- Direct Addressing Capability up to 60kB External Memory
- Powerful Addressing Modes Capability
- Multi-level Stack
- Vectored Interrupts (External: 2, Internal: 1)
- On-chip 8-bit Timer with 4-bit Prescaler
- 46 I/O Ports
- Serial I/O Ports
- Stand-by Capability (STOP/HALT mode)
- Fully Bus Compatible with 8080A
- On-chip Clock Generator
- Single Supply, CMOS Technology
- Low Power Consumption
- 64 pin Plastic Flat Package
- 64 pin QUIP

PIN CONFIGURATION



NC: Non-connection

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	ROM
μPD78C06AG-XXX-36	64-PIN QUIP	4-MASK ROM

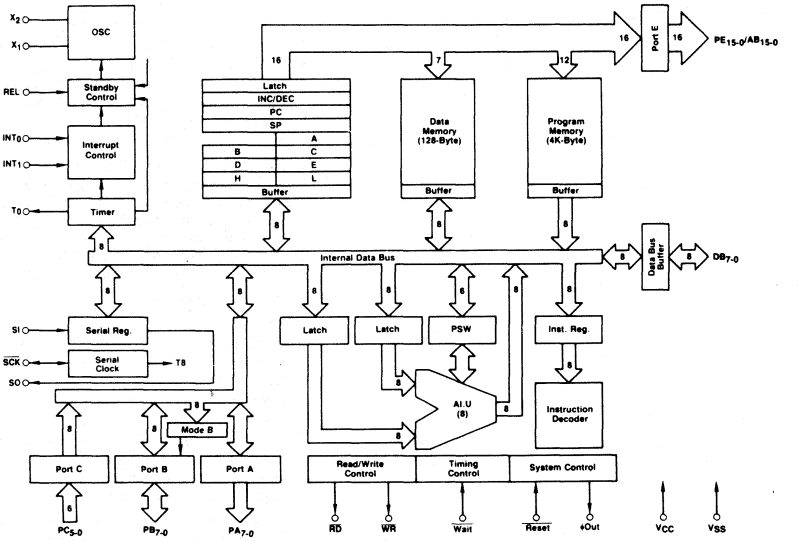
NOTE: QUIP = QUAD IN LINE, SDIP = SCHRINKED DUAL IN LINE,
FLAT = FLAT PACKAGE (SMD)

PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
2-5 61-64	DB_0-DB_7	(Input/Output) This is an 8-bit bi-directional data bus. The data move between an external memory or I/O, and accumulator is done through this data bus. During an input, HALT, STOP mode, and RESET, the output of the data bus goes a high impedance state. Input/Output level are TTL compatible.
6	INT_1	(Input) It is a rising-edge sensitive interrupt line, and it becomes valid when INT_1 input goes low to high. Subsequently, if users want to perform another interrupt on this line after an interrupt on this line is accepted, they must take it into consideration that INT_1 input should be maintained at low state a little while, and then it should go high. Unless, it does not enable another interrupt.
7	INT_0	(Input) It is a level-sensitive interrupt input line which is high level active.
8	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state T_W and remains in that state as long as $\overline{WAIT}$ is active.
9	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
10	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
11-16	PC_0-PC_5	(Input) This is a 6-bit input port with pull-up resistors. Input data to this port can be test by test instruction, and also moved to least significant 6-bit of accumulator and higher 2-bit of accumulator is lodaded with "0". Input level is CMOS compatible. This port is fit for key-input port.
17	REL	(Input) This is an input to release the STOP mode of stand-by function. STOP mode is released by raising the REL input high, then clock generator which has been stopped will restart. During REL input is high, the bit 3 of Stand-by Control Register (SC3) is set to one, and it is reset to zero after REL signal returns low. Pull-down resistor is built in.
18	TO	(Output) The square wave is output from this line. Its cycle time is half of a count time of the internal timer. It goes on low level after reset.
19	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
20	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
22	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
22	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD78C06A.
23	X_2	(Output) Oscillator output.
24	X_1	(Input) Clock Input
27-34	PA_0-PA_7	(Output) 8-bit output port with latch capability.
35-42	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.
43-57,59	PE_0-PE_{15}	(Output) 16-bit address bus and output port.
64	ϕOUT	(Output) The Clock of system clock frequency (1/8 of crystal frequency or X_1 external clock frequency) is placed out from this line. It is still placed out in HALT mode, but it is fixed to high in STOP mode.

3

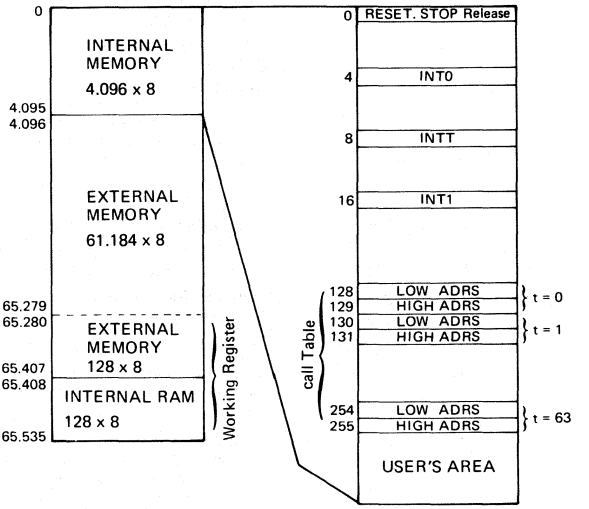
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Memory Map

The μPD78C06A can directly address the memory up to 64k bytes. Except on-chip ROM (0-4095) and RAM (65.408-65.535), and memory location can be used as either of RAM or ROM, freely. In the internal ROM area, the Reset/Stop mode Restart Address, Interrupt Start Address, Call Table etc. are involved. External memory and on-chip RAM area can be used as data memory (RAM), program memory (ROM), and/or working registers, freely.



FUNCTIONAL DESCRIPTION

I/O PORTS

PORT	FUNCTIONS
Port A	8-bit output port with latch
Port B	8-bit programmable Input/Output port w/latch
Port C	6-bit input port with pull up resistors
Port E	16-bit Address bus/Output Port

Port A

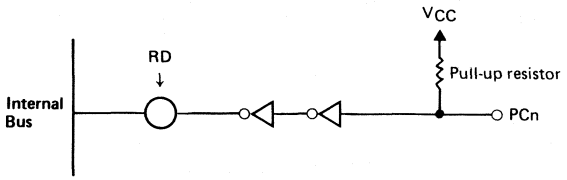
Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using Arithmetic and Logic instructions. Data remains latched at Port A unless acted on by another Port A instruction or a RESET is issued.

Port B

Port B is an 8-bit I/O port. Data is latched at Port B in both the Input or Output modes. Each bit of Port B can be independently set to either Input or Output mode. The Mode B register programs the individual lines of Port B to be either an Input (Mode $B_n = 1$) or an Output (Mode $B_n = 0$).

Port C

This is a 6-bit input port with pull-up resistors. Input data to this port can be test by instruction, and also moved to least significant 6-bit of accumulator and higher 2-bit of accumulator is loaded with "0". Input level is CMOS compatible. This port is fit for key-input port.



Port E (μPD78C06A)

Port E is a 16-bit address bus/output port. There are two ways to use these lines:

a) 16-Bit Address Bus – the PER instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).

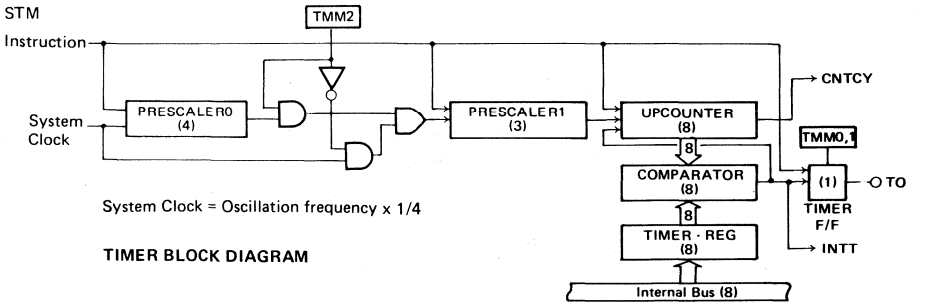
b) 16-Bit Output Port – the PEX instruction sets Port E to a 16-bit output port. The contents of B and C registers appear on PE_{8-15} and PE_{0-7}, respectively.

Address bus AB_{15}–AB_0 (μPD78C05A)

These lines are the 16 bit-to-bit address bus to the main memory. The μPD78C05A, having no internal ROM, must address the area from 0 to 4096 as external ROM.

The μPD78C05A AB lines are unlike the μPD78C06A PE lines; they have no internal latches. When the Port E output instruction PEX is executed in a μPD78C05A, the register pair BC is output to the AB lines for only one clock cycle during the third machine cycle. This is provided to allow external hardware to emulate the Port E operation of the μPD78C06A.

TIMER OPERATION



System Clock = Oscillation frequency x 1/4

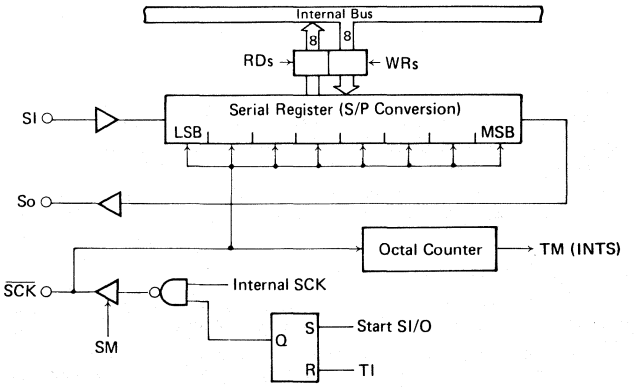
TIMER BLOCK DIAGRAM

This is a programmable 8-bit interval timer with prescaler. It consists of TIMER·REG (8-bit), PRESCALER0 (4-bit), PRESCALER1 (3-bit), UPCOUNTER (8-bit), COMPARATOR (8-bit), and TIMER F/F.

Count time and TO output are controlled by Timer Mode Register (TMM). It can count 5,3 μsec to 1,3 msec with resolution of 5,3 μsec (TMM2 = 0), or 85,3 μsec to 21,3 msec with resolution of 85,3 μsec (TMM2 = 1).

At first set the count value to the TIMER REG by MOV TM, A instruction, then initialize the PRESCALER0, 1, TIMER F/F, UPCOUNTER and start timer by STM instruction. UPCOUNTER is incremented at every 5,3 μs (TMM2 = 0) or 85,3 μs (TMM2 = 1(. COMPARATOR always compares the contents of UPCOUNTER with TIMER·REG, and it generates match signal (internal interrupt; INTT) when they are matched. The match signal clears the content of UPCOUNTER, and restarts the countup. Accordingly, this timer operates as the interval timer which generates repetitive interrupts with the interval of count time specified by count value of TIMER·REG. When a timer interrupt is generated in HALT mode, the HALT mode is released.

SERIAL PORT OPERATION



The Block Diagram of Serial Ports

FUNCTIONAL DESCRIPTION (CONT.)

Serial interface section consists of Serial Input (SI) line, Serial Output (SO) Line, Serial Clock ($\overline{SCK}$) input/output line, an 8-bit Serial Register (S/P), an octal counter, a R-S flip-flop used for transfer control, and some gates. When the bit 6 of Serial Mode Register (SM6) is 0, $\overline{SCK}$ becomes internal clock mode fixed to 1/8 of oscillator frequency (if fosc = 6MHz, then $\overline{SCK}$ is fixed to 780KHz), however, when the SM6 is 1, it becomes external clock mode, and operates with DC to 780KHz external clock. Accordingly, the transfer operation in internal clock mode is performed synchronously with constant frequency, and in external clock mode it performed synchronously with variable frequency.

A transmitting data is set to serial register by MOV S, A instruction, then the octal counter is reset and serial transfer is triggered by SIO instruction. At every falling edge of $\overline{SCK}$, the contents of serial register are shift, and shift-out data are placed to SO line with MSB as starting bit.

While the $\overline{SCK}$ is low the data on SI line is loaded in continuously, and then latched to serial register at the rising edge of the $\overline{SCK}$. Like this both the input and output of serial data are performed by same $\overline{SCK}$.

After occuring eight $\overline{SCK}$ pulses and completing 8-bit serial data transfer, the carry T8 is generated from the octal counter and it sets the interrupt request flag (INTFS). But μPD78C05A/06A has no serial interrupt, then INTFS is checked by only test instruction (SKNIT FS).

In internal $\overline{SCK}$ mode, as T8 signal resets the control flip-flop, the following transfer after completing 8-bit transfer are disabled until next SIO instruction will be given.

Accordingly, the data transfer should be restarted by SIO instruction with the next conditions. In case of data reception, after receiving the data from serial register by MOV A,S instruction, and in case of data transmission, after setting the data to serial register by MOV S,A instruction, data transmittion must be done by SIO instructions.

INTERRUPT STRUCTURE

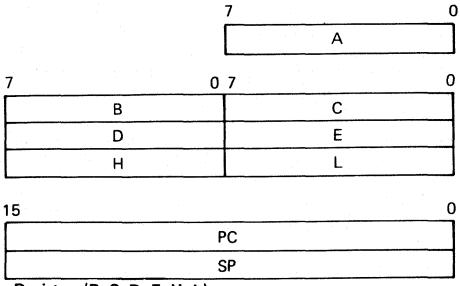
The μPD78C05A/06A provides a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from 3 different sources; two external interrupts and one internal interrupt. Each interrupt when activated branches to a designated memory vector location.

INT	VECTORED MEMORY LOCATION	PRIORITY	TYPE
INT_0	4	1	External, level sensitive
INT_1	16	3	External, rising edge sensitive
INTT	8	2	Internal, match on timer comparator

FUNCTIONAL DESCRIPTION (CONT.)

REGISTERS

This mainly consists of the seven 8-bit registers and two 16-bit registers as below.



General Purpose Registers (B, C, D, E, H, L)

They can function as auxilliary registers to the accumulator (A) or in pairs as data pointers (BC, DE, HL). Auto increment and decrement addressing mode capabilities extend the uses for the DE and HL register pairs.

Accumulator (A)

All data transfers between the μPD78C05A/06A and external memory or I/O are done through the accumulator. The contents of the Accumulator and Vector Registers can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A Reset sets the PC to 0000_H.

Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

STAND-BY OPERATION

Stand-by function is used to lower the power consumption in stand-by condition, and there are two types of it: HALT mode and STOP mode.

In HALT mode the masking functions are active, so that programmer can chose an interrupt source, $\overline{\text{RESET}}$ or T8-signal for release use.

STOP mode can be released by REL or RESET signal. In both cases, program will start at location 0 again.

HALT AND STOP MODE

FUNCTION	HALT MODE	STOP MODE
Oscillator	Run	Stop
Internal System Clock	Stop	
Timer	Run	
Timer Register	Hold	Set
Upcounter, Prescaler 0, 1	Run	Cleared
Serial Interface		Run ①
Serial Clock	Hold	Hold
Interrupt Control Circuit	Run	Stop
Interrupt Enable Flag	Hold	Reset
INT_0, INT_1 Input	Active	Inactive
INT_T		–
T_8 (INTFS)		–
Mask Register	Hold	Set
Pending Interrupts (INTFX)		Reset
REL Input	Inactive	Active
$\overline{\text{RESET}}$ Input	Active	

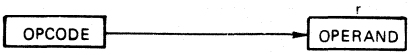
FUNCTION	HALT MODE	STOP MODE
On-chip RAM	Hold	Hold
Output Latch in Ports A, B, E		
Address Bus AB0 . . . 15		Low
Program Counter (PC)		Cleared
Stack Pointer (SP)		Unknown
General Registers (A, B, C, D, E, F, L)		
Program Status Word (PSW)		Reset
Mode B Register		Hold
Standby Control Register (SC_0–SC_3)		
Standby Control Register (SC_4)		Set
Timer Mode Register (TMM_0–TMM_1)		Hold
Timer Mode Register (TMM_1)		Set
Serial Mode Register (SM)		Hold
Data Bus (DB_0–DB_7)	High-Z	High-Z
$\overline{\text{RD}}$, $\overline{\text{WR}}$ Output	High	High

Note: ① Serial clock counter is running and T_8 is generated; however, there are no effects from it.

ADDRESS MODES

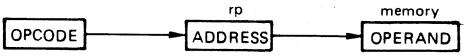
Register Addressing
Register Indirect Addressing
Auto-Increment Addressing
Auto-Decrement Addressing
Working Register Addressing
Direct Addressing
Immediate Addressing
Immediate Extended Addressing

Register Addressing



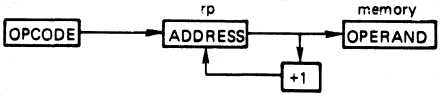
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



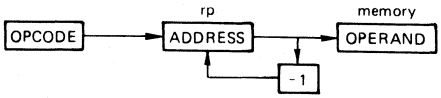
The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

Auto-Increment Addressing

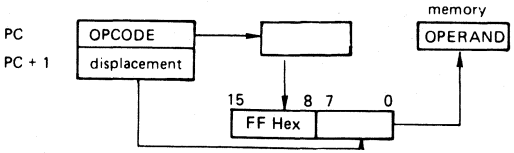


The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

Auto Decrement Addressing



Working Register Addressing

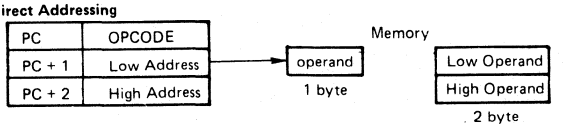


The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix ending this address mode.

3

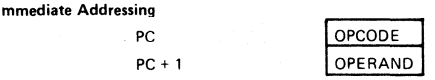
ADDRESS MODES (CONT.)

Direct Addressing



The two bytes following the opcode specify an address of a location containing the operand.

Immediate Addressing



Immediate Extended Addressing

PROGRAM STATUS WORD (PSW) OPERATION

OPERATION					D6	D5	D4	D3	D2	D0
REG. MEMORY		IMMEDIATE		SKIP	Z	SK	HC	L1	I0	CY
ADD ADC SUB SBB	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			‡	0	‡	0	0	‡
ANA ORA XRA	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		‡	0	•	0	0	•
ADDNC SUBNB GTA LTA	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	LTIW		‡	‡	‡	0	0	‡
	ONAX OFFAX	ONI OFFI	ONIW OFFIW		‡	‡	•	0	0	•
NEA EQA	NEAX EQAX	NEI EQI	NEIW EQIW		‡	‡	‡	0	0	‡
INR DCR	INRW DCRW				‡	‡	‡	0	0	•
DAA					‡	0	‡	0	0	‡
RLL, RLR					•	0	•	0	0	‡
RLD – RRD					•	0	•	0	0	•
STC					•	0	•	0	0	1
CLC					•	0	•	0	0	0
		MVI A, byte			•	0	•	1	0	•
		MVI L, byte LXI H, word			•	0	•	0	1	•
				SKNC SKNZ SKNIT	•	‡	•	0	0	•
				RETS	•	1	•	0	0	•
All other instructions					•	0	•	0	0	•

Notes: ‡ Flag affected according to result op operation.
1 Flag set.
0 Flag reset.
• Flag not affected.

μCOM87LC INSTRUCTION SET

Symbols/Description on Operand

SYMBOLS	DESCRIPTIONS
r r1 r2	A, B, C, D, E, H, L B, C, D, E, H, L A, B, C
sr sr1 sr2	PA PB MK MB TM S TMM SM SC PA PB PC MK S TMM SC PA PB PC MK
rp rp1	SP, B, D, H V, B, D, H
rpa wa	B, D, H, D+, H+, D−, H− 8-bit immediate data
word byte bit	16-bit immediate data 8-bit immediate data 3-bit immediata data
if	F0, F1, FT, FS
f	CY, Z

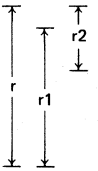
Notes:

1. At sr ~ sr2, the symbols of 'PA', 'PB', etc. stand for the following, respectively:
   PA = PORTA, PB = PORTB, PC = PORTC, MK = MASK·reg, MB = MODE·B, TM = TIMER·REG, S = SERIAL I/O, TMM = TIMER MODE REG, SM = SERIAL MODE REG, SC = STANDBY CONTROL REG
2. At rp ~ rp1, the 'SP', 'B', etc stand for the following, respectively;
   SP = STACK POINTER, B = BC, D = DE, H = HL, V = FFH·A
3. At rpa, the 'B', 'D', etc. stand for the following respectively:
   B = (BC), D = (DE), H = (HL), D+ = $(DE)^+$, H+ = $(HL)^+$, D− = $(DE)^-$, H− = $(HL)^-$
4. At if, the 'F0', 'F1', etc. stand for the following, respectively:
   F0 = INTF0, F1 = INTF1, FT = INTFT, FS = INTFS
5. At f, the 'CY', 'Z', stand for the following, respectively:
   CY = CARRY, Z = ZERO

The description of the symbols on Operation Codes is as follows:

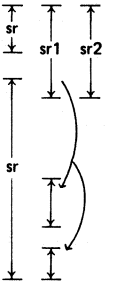
r

R_2	R_1	R_0	reg
0	0	0	
0	0	1	A
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L



sr

S_3	S_2	S_1	S_0	special reg
0	0	0	0	PORT A
0	0	0	1	PORT B
0	0	1	0	PORT C
0	0	1	1	MASK
0	1	0	0	MODE·B
0	1	0	1	–
0	1	1	0	TIMER·REG
0	1	1	1	–
1	0	0	0	SERIAL·I/O
1	0	0	1	TIMER MODE REG
1	0	1	0	SERIAL MODE REG
1	0	1	1	STANDBY CONTROL REG

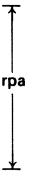


rp

P_1	P_0	reg·pair
0	0	SP
0	1	BC
1	0	DE
1	1	HL

rpa

A_2	A_1	A_0	addressing
0	0	0	–
0	0	1	(BC)
0	1	0	(DE)
0	1	1	(HL)
1	0	0	$(DE)^+$
1	0	1	$(HL)^+$
1	1	0	$(DE)^-$
1	1	1	$(HL)^-$



rp1

Q_1	Q_0	reg·pair
0	0	FFH.A
0	1	BC
1	0	DE
1	1	HL

if

I_2	I_1	I_0	INTF
0	0	0	INTF0
0	0	1	INTFT
0	1	0	INTF1
0	1	1	–
1	0	0	INTFS

f

F_2	F_1	F_0	flag
0	1	0	CY
1	0	0	Z

INSTRUCTION GROUPS

8-BIT DATA TRANSFER

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
MOV	r1, A	6	r1 ← A	
MOV	A, r1	6	A ← r1	
MOV	sr, A	14	sr ← A	
MOV	A, sr1	14	A ← sr1	
MOV	r, word	25	r ← (word)	
MOV	word, r	25	(word) ← r	
MVI	r, byte	11	r ← byte	
STAW	wa	14	(FFH, wa) ← A	
LDAW	wa	14	A ← (FFH, wa)	
STAX	rpa	9	(rpa) ← A	
LDAX	rpa	9	A ← (rpa)	
SBCD	word	28	(word) ← C, (word+1) ← B	
SDED	word	28	(word) ← E, (word+1) ← D	
SHLD	word	28	(word) ← L, (word+1) ← H	
SSPD	word	28	(word) ← SP_L, (word+1) ← SP_H	

3

16-BIT DATA TRANSFER

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
LBCD	word	28	C ← (word), B ← (word+1)	
LDED	word	28	E ← (word), D ← (word+1)	
LHLD	word	28	L ← (word), H ← (word+1)	
LSPD	word	28	SP_L ← (word), SP_H ← (word+1)	
PUSH	rp1	21	(SP−1) ← $rp1_H$, (SP−2) ← $rp1_L$	
POP	rp1	18	$rp1_L$ ← (SP), $rp1_H$ ← (SP+1) SP ← SP+2	
LXI	rp, word	16	rp ← word	

ARITHMETIC INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
ADD	A, r	12	A ← A+r	
ADDX	rpa	15	A ← A+(rpa)	
ADC	A, r	12	A ← A+r+CY	
ADCX	rpa	15	A ← A+(rpa)+CY	
SUB	A, r	12	A ← A−r	
SUBX	rpa	15	A ← A−(rpa)	
SBB	A, r	12	A ← A−r− CY	
SBBX	rpa	15	A ← A−(rpa)−CY	
ADDNC	A, r	12	A ← A+r	No Carry
ADDNCX	rpa	15	A ← A+(rpa)	No Carry
SUBNB	A, r	12	A ← A−r	No Borrow
SUBNBX	rpa	15	A ← A−(rpa)	No Borrow

LOGIC INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
ANA	A, r	12	A ← A∧r	
ANAX	rpa	15	A ← A∧(rpa)	
ORA	A, r	12	A ← A∨r	
ORAX	rpa	15	A ← A∨(rpa)	
XRA	A, r	12	A ← A∨r	
XRAX	rpa	15	A ← A∨(rpa)	
GTA	A, r	12	A−r−1	No Borrow
GTAX	rpa	15	A−(rpa)−1	No Borrow
LTA	A, r	12	A−r	Borrow
LTAX	rpa	15	A−(rpa)	Borrow
ONAX	rpa	15	A∧(rpa)	No Zero
OFFAX	rpa	15	A∧(rpa)	Zero
NEA	A, r	12	A−r	No Zero
NEAX	rpa	15	A−(rpa)	No Zero
EQA	A, r	12	A−r	Zero
EQAX	rpa	15	A−(rpa)	Zero

IMMEDIATE OPERATION INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
XRI	A, byte	11	A ← AVbyte	
DINC	A, byte	11	A ← A + byte	No Carry
SUINB	A, byte	11	A ← A–byte	No Borrow
ADI	A, byte	11	A ← A+byte	
ACI	A, byte	11	A ← A+byte+CY	
SUI	A, byte	11	A ← A–byte	
SBI	A, byte	11	A ← A–byte –CY	
ANI	A, byte	11	A ← A∧byte	
ORI	A, byte	11	A ← AVbyte	
GTI	A, byte	11	A–byte–1	No Borrow
LTI	A, byte	11	A–byte	Borrow
ONI	A, byte	11	A∧byte	No Zero
OFFI	A, byte	11	A∧byte	Zero
NEI	A, byte	11	A–byte	No Zero
EQI	A, byte	11	A–byte	Zero

3

SPECIAL REGISTER

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
ANI	sr2, byte	23	sr2 ← sr2∧byte	
ORI	sr2, byte	23	sr2 ← sr2Vbyte	
ONI	sr2, byte	20	sr2∧byte	No Zero
OFFI	sr2, byte	20	sr2∧byte	Zero

WORKING REGISTER OPERATIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
ANIW	wa, byte	22	(FFH.wa) ← (FFH.wa)∧byte	
ORIW	wa, byte	22	(FFH.wa) ← (FFH.wa)Vbyte	
GTIW	wa, byte	19	(FFH.wa)–byte–1 No Borrow	No Borrow
LTIW	wa, byte	19	(FFH.wa)–byte	Borrow
ONIW	wa, byte	19	(FFH.wa)∧byte	No Zero
OFFIW	wa, byte	19	(FFH.wa)∧byte	Zero
NEIW	wa, byte	19	(FFH.wa)–byte	No Zero
EQIW	wa, byte	19	(FFH.wa)–byte	Zero

INCREMENT/DECREMENT INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
INR	r2	6	r2 ← r2+1	Carry
INRW	wa	17	(FFH.wa) ← (FFH.wa)+1	Carry
DCR	r2	6	r2 ← r2–1	Borrow
DCRW	wa	17	(FFH.wa) ← (FFH.wa)–1	Borrow
INX	rp	9	rp ← rp+1	
DCX	rp	9	rp ← rp–1	

OTHER OPERATIONAL INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
DAA		6	Decimal Adjust Accumulator	
STC		12	CY ← 1	
CLC		12	CY ← 0	

ROTATION INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
RLD		21	Rotate Left Digit	
RRD		21	Rotate Right Digit	
RLL	A	12	Am+1 ← Am, A_0 ← CY, CY ← A_7	
RLR	A	12	Am–1 ← Am, A_7 ← CY, CY ← A_0	

JUMP INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
JMP	word	16	PC ← word	
JB		6	PC_H ← B PC_L ← C	
JR	word	12	PC ← PC+1+jdisp1	
JRE	word	17	PC ← PC+2+jdisp	

CALL INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
CALL	word	22	(SP–1) ← $(PC+3)_H$, (SP–2) ← $(PC+3)_L$, PC ← word	
CALF	word	17	(SP–1) ← $(PS+2)_H$, (SP–2) ← $(PC+2)_L$ PC15~11 ← 00001, PC10~ 0 ← 1a	
CALT	word	21	(SP–1) ← $(PC+1)_H$, (SP–2) → $PC+1)_L$ PC_L ← (128+21a), PC_H ← (129+21a)	

RETURN INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
RET		12	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1)$ $SP \leftarrow SP+2$	
RETS		12+n	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1), SP \leftarrow SP+2$ $PC \leftarrow PC+n$	Uncon-ditional Skip
RETI		15	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1)$ $PSW \leftarrow (SP+2), SI' \leftarrow SP+3$	

SKIP INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
SKN	CY	12	Skip if No Carry	CY = 0
SKN	Z	12	Skip if No Zero	Z = 0
SKNIT	if	12	Skip if No INTX Reset INTX if INTX = 1	f = 0

CPU CONTROL INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
NOP		6	No Operation	
EI		12	Enable Interrupt	
DI		12	Disable Interrupt	

REGISTER CONTROL INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
SIO		6	Start (Trigger) Serial I/O	
STM		6	Start Timer	

INPUT/OUTPUT INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
PEX		15	$PE_{15-8} \leftarrow B, PE_{7-0} \leftarrow C$	
PER		12	Port E AB Mode	

(Note)

The clock cycles shown here are indicated about in care of that the program are located in the on-chip ROM, and the other data are located in the on-chip RAM or external memory requiring no wait. If the programs were located in the on-chip RAM or external memory, then the clock cycles are shortened by two clock cycles per one-byte fetch.

Ex. PER instruction (2-byte instruction)

In case of the on-chip ROM access: 12 clock cycles

In case of the on-chip RAM or external memory access: 12– (2x2) = 8 clock cycles

1 clock cycle = 4/fosz

Differences between μPD78C06A and μPD78C05A

Parameter		μPD78C06A	μPD78C05A
4K-byte built-in ROM		Yes	No
Internal WAIT of built-in ROM		2 WAIT cycle	No
Port E (Address bus)	After reset	Port mode	Address bus mode
	Latch function	Yes	No
	PEX instruction	PE15 – 8⇦B and PE7 – 0⇦C are executed and latched at M3T1 timing. Output is unchanged until the next PEX or PER instruction is executed.	AB15 – 8⇦B and AB7 – 0⇦C are executed only at M3T1 timing and the contents of the internal address bus are output at the other timing.
$\overline{RD}/\overline{WR}$ signal		Output against the address space of 1000H – FF7FH (4096 – 65407).	Output against the address space of 000H – FF7FH (0 – 65407).
M1 output		No	Yes
Pin connection		Difference	
Package		64 pin Flat 64 pin QUIP	64 pin QUIP

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Supply Voltage	V_{CC}		−0.3 to +7.0	V
Input Voltage	V_I		−0.3 to V_{CC} + 0.3	V
Output Voltage	V_O		−0.3 to V_{CC} + 0.3	V
Output High Current	I_{OH}	Device Total	−5	mA
Output Low Current	I_{OL}	Device Total	43.5	mA
Operating Temperature	T_{opt}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

DC CHARACTERISTICS

(T_a = −40 to +85°C, V_{CC} = +5.0V ± 10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH1}	INT_{0-1}, $\overline{WAIT}$, PB_{0-7}, PC_{0-5}	0.7 V_{CC}		V_{CC}	V
	V_{IH2}	$\overline{RESET}$, $\overline{SCK}$, REL, SI	0.75 V_{CC}		V_{CC}	V
	V_{IH3}	DB_{0-7}	V_{CC} −2.0		V_{CC}	V
	V_{IH4}	X1	V_{CC} −0.5		V_{CC}	V
Input Low Voltage	V_{IL1}	INT_{0-1}, $\overline{WAIT}$, PB_{0-7}, PC_{0-5}	0		0.3 V_{CC}	V
	V_{IL2}	$\overline{RESET}$, $\overline{SCK}$, REL, SI	0		0.25 V_{CC}	V
	V_{IL3}	DB_{0-7}	0		0.8	V
	V_{IL4}	X1	0		0.5	V
Output High Voltage	V_{OH1}	I_{OH} = −100 μA	2.4			V
	V_{OH2}	I_{OH} = −50 μA	V_{CC} −0.5			V
Output Low Voltage	V_{OL}	I_{OL} = 1.8 mA			0.45	V
Input High Current	I_{IH1}	V_{IN} = V_{CC} (REL)	7		100	μA
	I_{IH2}	V_{IN} = V_{CC} (X1)			45	μA
Input Low Current	I_{IL1}	V_{IN} = 0V ($\overline{WAIT}$, PC_{0-5})	−7		−100	μA
	I_{IL2}	V_{IN} = 0V (X1)			−45	μA
Input High Leakage Current	I_{LIH}	V_{IN} = V_{CC} (Except REL, X1)			3.2	μA
Input Low Leakage Current	I_{LIL1}	V_{IN} = OV (Except $\overline{WAIT}$, PC_{0-5}, X1)			−3.2	μA
	I_{LIL2}	V_{IN} = 0V (STOP Mode, X1)			−3.2	μA
Output High Leakage Current	I_{LOH}	V_{OUT} = V_{CC}			3.2	μA
Output Low Leakage Current	I_{LOL}	V_{OUT} = 0V			−3.2	μA
V_{CC} Supply Current	I_{CC1}	Operation Mode		4.0	7.5	mA
	I_{CC2}	HALT Mode		1.2	2.7	mA
	I_{CC3}	STOP Mode (X1 = OV, X2 = Open)		1	20	μA

CAPACITANCE

(T_a = 25°C, V_{CC} = GND = OV)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_C = 1MHz			15	pF
Output Capacitance	C_O	Unmeasured Pins returned to OV			15	pF
I/O Capacitance	$C_{I/O}$				15	pF

AC CHARACTERISTICS CLOCK TIMING

(T_a = −40 to +85°C, V_{CC} = +5.0V ± 10 %)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
X1 Input Cycle Time	t_{CYX}		160		10000	ns
X1 Input Low Time	t_{XXL}		75			ns
X1 Input High Time	t_{XXH}		75			ns
ϕ_{OUT} Cycle Time	$t_{CY\phi}$		640		40000	ns
ϕ_{OUT} Low Time	$t_{\phi\phi L}$		195			ns
ϕ_{OUT} High Time	$t_{\phi\phi H}$		195			ns
ϕ_{OUT} Rise/Fall Time	t_r, t_f				120	ns

READ/WRITE OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RD}$ L. E. to ϕ_{OUT} L. E.	$t_{R\phi}$	$t_{CY\phi}$ = 660 ns	180			ns
Address (PE_{0-15}) to Data Input	t_{AD1}				790 +660xN	ns
$\overline{RD}$ T. E. to Address	t_{RA}		180(T3) 840(T4)			ns
$\overline{RD}$ L. E. to Data Input	t_{RD}				460 +660xN	ns
$\overline{RD}$ T. E. to Data Hold Time	t_{RDH}		0			ns
$\overline{RD}$ Low Time	t_{RR}		1070 +660xN			ns
$\overline{RD}$ L. E. to $\overline{WAIT}$ L. E.	t_{RWT}				460	ns
Address (PE_{0-15}) to $\overline{WAIT}$ L. E.	t_{AWT1}				790	ns
$\overline{WAIT}$ Set Up Time to ϕ_{OUT} L. E.	t_{WTS}		370			ns
$\overline{WAIT}$ Hold Time after ϕ_{OUT} L. E.	t_{WTH}		0			ns
M1 to RD L. E.	t_{MR}		108			ns
RD T. E. to M1	t_{RM}		130			ns
ϕ_{OUT} L. E. to $\overline{WR}$ L. E.	$t_{\phi W}$				175	ns
Address (PE_{0-15}) to ϕ_{OUT} T. E.	$t_{A\phi}$		90			ns
Address (PE_{0-15}) to Data Output	t_{AD2}		510			ns
Data Output to $\overline{WR}$ T. E.	t_{DW}		740 +660xN			ns
$\overline{WR}$ T. E. to Data Stable Time	t_{WD}		130			ns
Address (PE_{0-15}) to $\overline{WR}$ L. E.	t_{AW}		460			ns
$\overline{WR}$ T. E. to Address Stable Time	t_{WA}		180			ns
$\overline{WR}$ Low Time	t_{WW}		690 +660xN			ns
$\overline{WR}$ L. E. to $\overline{WAIT}$ L. E.	t_{WWT}				110	ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	1270			ns
		$\overline{SCK}$ Output	1280		80000	ns
$\overline{SCK}$ Low Time	t_{KKL}	$\overline{SCK}$ Input	515			ns
		$\overline{SCK}$ Output	520			ns
$\overline{SCK}$ High Time	t_{KKH}	$\overline{SCK}$ Input	515			ns
		$\overline{SCK}$ Output	520			ns
SI Set Up Time to $\overline{SCK}$ T. E.	t_{SIS}		200			ns
SI Hold Time after $\overline{SCK}$ T. E.	t_{SIH}		250			ns
$\overline{SCK}$ L. E. to SO Delay Time	t_{KO}				300	ns

Note: 1) Input timings are measured at V_{IHMIN} and V_{ILMAX}.
2) Output timings are measured at V_{OH} = 2.4 V and V_{OL} = 0.45 V with 1TTL + 200 pF load.
3) L. E. = Leading Edge, T. E. = Trailing Edge
4) N is number of T_{WAIT}.

BUS TIMING DEPENDING ON t_{CYC}

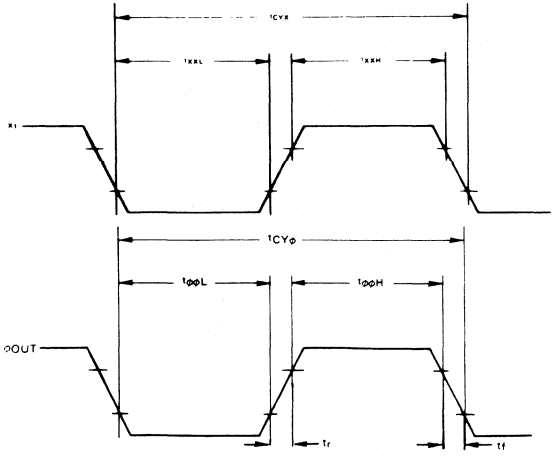
(T_a = −40 to + 85°C)

SYMBOL	CALCULATING EXPRESSION	MIN/MAX	UNITS
$t_{R\phi}$	(1/2)T − 150	MIN	ns
t_{AD1}	(3/2+N)T − 200	MAX	ns
$t_{RA(T3)}$	(1/2)T − 150	MIN	ns
$t_{RA(T4)}$	(3/2)T − 150	MIN	ns
t_{RD}	(1+N)T − 200	MAX	ns
t_{RR}	(2+N)T − 250	MIN	ns
t_{RWT}	T − 200	MAX	ns
t_{AWT1}	(3/2)T − 200	MAX	ns
t_{WTS}	(1/3)T + 150	MIN	ns
t_{MR}	(3/8)T − 140	MIN	ns
t_{RM}	(1/2)T − 200	MIN	ns
$t_{A\phi}$	(1/2)T − 240	MIN	ns
t_{AD2}	T − 150	MIN	ns
t_{DW}	(3/2+N)T − 250	MIN	ns
t_{WD}	(1/2)T − 200	MIN	ns
t_{AW}	T − 200	MIN	ns
t_{WA}	(1/2)T − 150	MIN	ns
t_{WW}	(3/2+N)T − 300	MIN	ns
t_{WWT}	(1/2)T − 220	MAX	ns
t_{CYK}	2T	MIN	ns
t_{KKL}	T − 120	MIN	ns
t_{KKH}	T − 120	MIN	ns

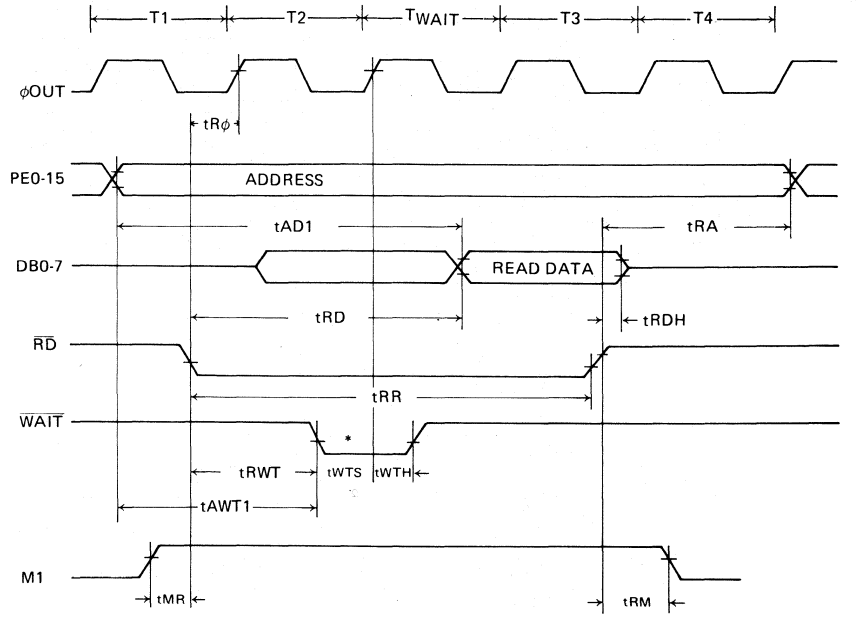
Note: 1) N = Number of T_{WAIT}.
2) T = $T_{CY\phi}$.
3) t_{CY} assumes 50 % duty cycle on X1.
4) The items out of this table are not dependent on t_{CY}.

TIMING WAVEFORMS

CLOCK TIMING

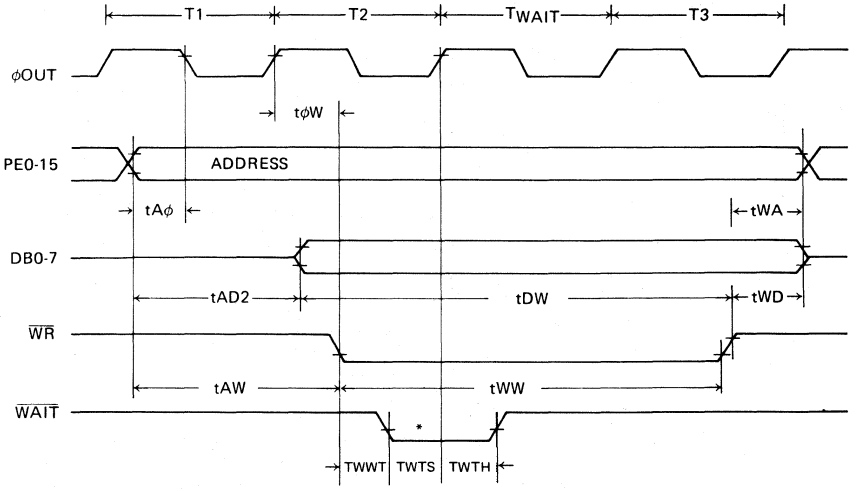


READ OPERATION



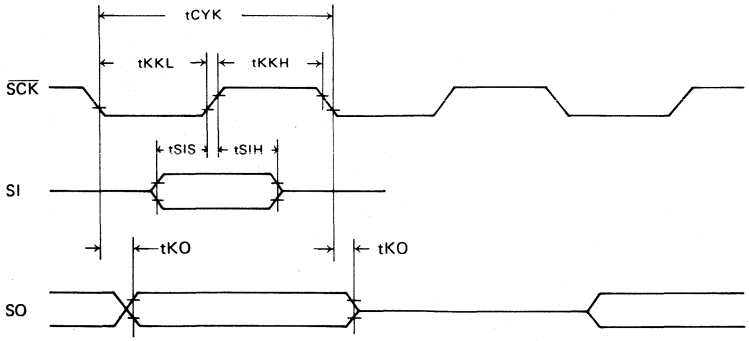
* WAIT signal must be remained stable during t_{WTS} and t_{WTH}.
If it is unstable, misoperation may occur.

WRITE OPERATION



* WAIT signal must be remained stable during t_{WTS} and t_{WTH}.
If it is unstable, misoperation may occur.

SERIAL OPERATION



Low Power Data Memory Retention Characteristics for STOP Mode Operation

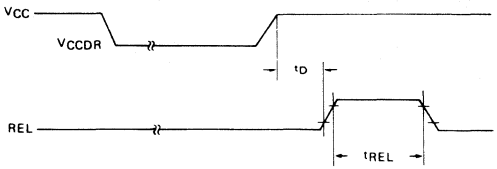
3

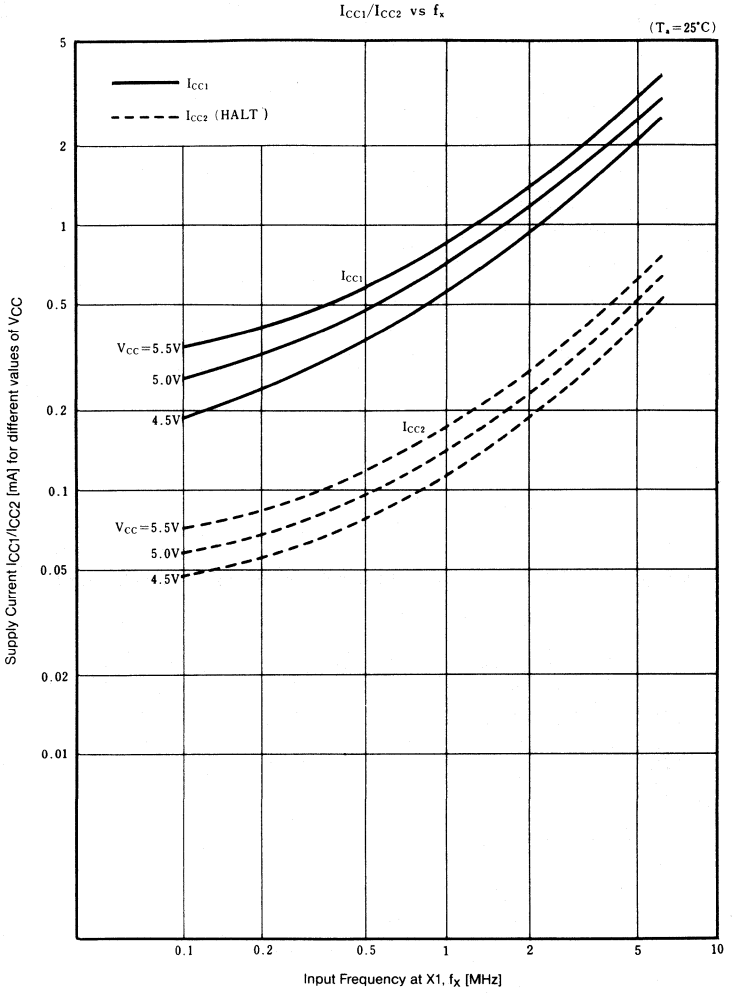
(T_a = −40 to +85°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{CCDR}		2.0			V
Data Retention Supply Current	I_{CCDR}	V_{CCDR} = 2.0V, X1 = 0V, X2 = Open		0.8	20	μA
Data Retention Input Low REL Voltage	V_{ILDR}		0		0.2 V_{CCDR}	V
Data Retention Input High $\overline{RESET}$ Voltage	V_{IHDR}		0.8 V_{CCDR}		V_{CCDR}	V
REL Input Delay Time	t_D		500			μs
REL Input High Time	t_{REL}		10			μs

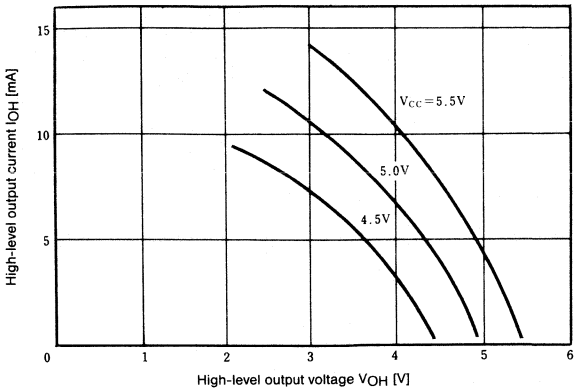
Note: In data retention mode,

1) Input voltages to $\overline{WAIT}$ and PC_{0-5} pins (with pull-up resisters) should be maintained same as V_{CCDR} level,
2) Other input voltages should be kept less than V_{CCDR} level.

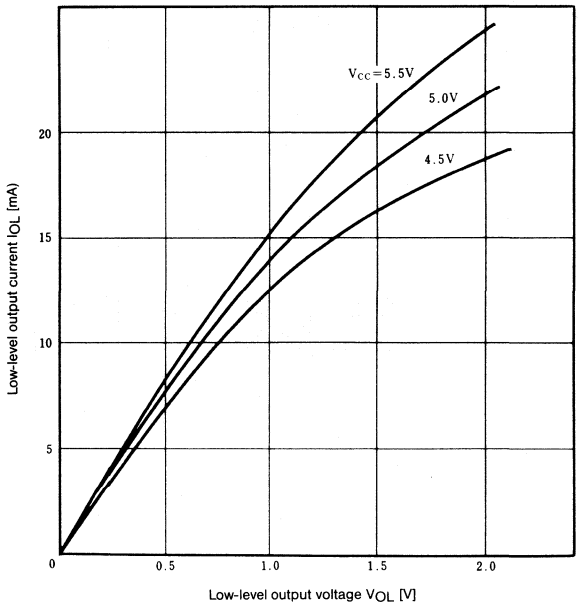



I_{CC1}/I_{CC2} vs f_x
(T_a=25°C)
I_{CC1}
I_{CC2} (HALT)
I_{CC1}
V_{CC}=5.5V
5.0V
4.5V
I_{CC2}
V_{CC}=5.5V
5.0V
4.5V
Supply Current I_{CC1}/I_{CC2} [mA] for different values of V_{CC}
5
2
1
0.5
0.2
0.1
0.05
0.02
0.01
0.1
0.2
0.5
1
2
5
10
Input Frequency at X1, f_X [MHz]

I_{OH} vs V_{OH} (T_a=25°C)



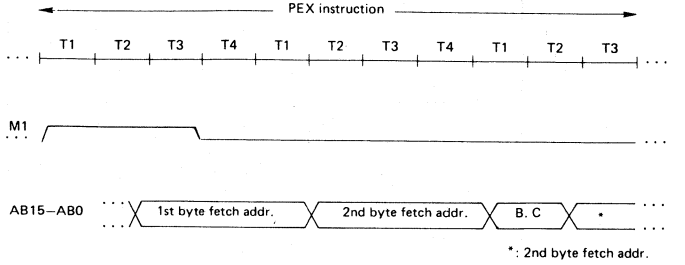
I_{OL} vs V_{OL} (T_a=25°C)



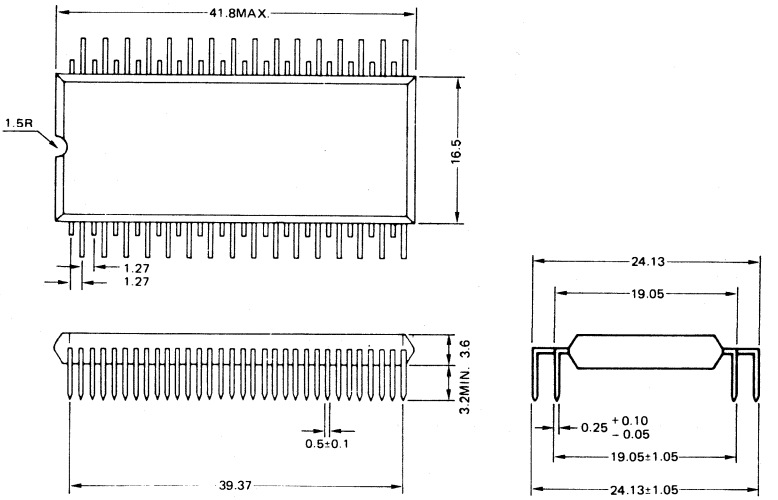
3

PORT E OPERATION μPD78C05A

The following diagram is the timing at PEX instruction execution.



64 PIN PLASTIC QUIP OUTLINE (Unit : mm) for μPD78C05AG



ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Supply Voltage	V_{CC}		−0.3 to +7.0	V
Input Voltage	V_I		−0.3 to V_{CC} + 0.3	V
Output Voltage	V_O		−0.3 to V_{CC} + 0.3	V
Output High Current	I_{OH}	Device Total	−5	mA
Output Low Current	I_{OL}	Device Total	45	mA
Operating Temperature	T_{opt}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

DC CHARACTERISTICS

(T_a = −40 to +85°C, V_{CC} = +5.0V ± 10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH1}	INT_{0-1}, $\overline{WAIT}$, PB_{0-7}, PC_{0-5}	0.7 V_{CC}		V_{CC}	V
	V_{IH2}	$\overline{RESET}$, $\overline{SCK}$, REL, SI	0.75 V_{CC}		V_{CC}	V
	V_{IH3}	DB_{0-7}	V_{CC} −2.0		V_{CC}	V
	V_{IH4}	X1	V_{CC} −0.5		V_{CC}	V
Input Low Voltage	V_{IL1}	INT_{0-1}, $\overline{WAIT}$, PB_{0-7}, PC_{0-5}	0		0.3 V_{CC}	V
	V_{IL2}	$\overline{RESET}$, $\overline{SCK}$, REL, SI			0.25 V_{CC}	V
	V_{IL3}	DB_{0-7}	0		0.8	V
	V_{IL4}	X1	0		0.5	V
Output High Voltage	V_{OH1}	I_{OH} = −100 μA	2.4			V
	V_{OH2}	I_{OH} = −50 μA	V_{CC} −0.5			V
Output Low Voltage	V_{OL}	I_{OL} = 1.8 mA			0.45	V
Input High Current	I_{IH1}	V_{IN} = V_{CC} (REL)	7		100	μA
	I_{IH2}	V_{IN} = V_{CC} (X1)			45	μA
Input Low Current	I_{IL1}	V_{IN} = 0V ($\overline{WAIT}$, PC_{0-5})	−7		−100	μA
	I_{IL2}	V_{IN} = 0V (X1)			−45	μA
Input High Leakage Current	I_{LIH}	V_{IN} = V_{CC} (Except REL, X1)			3.2	μA
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0V (Except $\overline{WAIT}$, PC_{0-5}, X1)			−3.2	μA
	I_{LIL2}	V_{IN} = 0V (STOP Mode, X1)			−3.2	μA
Output High Leakage Current	I_{LOH}	V_{OUT} = V_{CC}			3.2	μA
Output Low Leakage Current	I_{LOL}	V_{OUT} = 0V			−3.2	μA
V_{CC} Supply Current	I_{CC1}	Operation Mode		4.0	7.5	mA
	I_{CC2}	HALT Mode		1.2	2.7	mA
	I_{CC3}	STOP Mode (X1 = OV, X2 = Open)		1	20	μA

DC CHARACTERISTICS

(T_a = −40 to +85°C, V_{CC} = +2.5V to +6.0V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage High	V_{IH1}	Except DB_{0-7}, X1		0.8 V_{CC}		V_{CC}	V
	V_{IH2}	DB_{0-7}		0.7 V_{CC}		V_{CC}	V
	V_{IH3}	X1	(1)	0.9 V_{CC}		V_{CC}	V
			(2)	V_{CC} −0.5		V_{CC}	V
Input Voltage Low	V_{IL1}	Except DB_{0-7}, X1		0		0.2 V_{CC}	V
	V_{IL2}	DB_{0-7}	(1)	0		0.18 V_{CC}	V
			(2)	0		0.8	V
	V_{IL3}	X1	(1)	0		0.1 V_{CC}	V
			(2)	0		0.5	V
Output Voltage	V_{OH}	I_{OH} = −50μA		V_{CC} −0.5			V
Output Voltage Low	V_{OL}	I_{OL} = 400μA				0.45	V
Input Current High	I_{IH1}	V_{IN} = V_{CC} (REL)		2.5		110	μA
	I_{IH2}	V_{IN} = V_{CC} (X1)				50	μA
Input Current Low	I_{IL1}	V_{IN} = 0V ($\overline{WAIT}$, PC_{0-5})		−2.5		−110	μA
	I_{IL2}	V_{IN} = 0V (X1)				−50	μA
Input Leakage Current High	I_{LIH}	V_{IN} = V_{CC} (Except REL, X1)				3.5	μA
Input Leakage Current Low	I_{LIL1}	V_{IN} = 0V (Except $\overline{WAIT}$, PC_{0-5}, X1)				−3.5	μA
	I_{LIL2}	V_{IN} = 0V (STOP Mode, X1)				−3.5	μA
Output Leakage Current High	I_{LOH}	V_{OUT} = V_{CC}				3.5	μA
Output Leakage Current Low	I_{LOL}	V_{OUT} = 0V				−3.5	μA
V_{CC} Supply Current	I_{CC1}	Operation Mode	V_{CC} = 3V, $t_{CY\phi}$ = 8μs		0.7	1.5	mA
			V_{CC} = 6V, $t_{CY\phi}$ = 1.32μs		5.0	9.0	mA
	I_{CC2}	HALT Mode	V_{CC} = 3V, $t_{CY\phi}$ = 8μs		0.2	0.5	mA
			V_{CC} = 6V, $t_{CY\phi}$ = 1.32μs		1.5	3.0	mA
	I_{CC3}	STOP Mode	(X1 = 0V, X2 = Open)		1	20	μA

Notes 1: 2.5V ≦ V_{CC} ≦ 4.5V
2: 4.5V ≦ V_{CC} ≦ 6.0V

3

CAPACITANCE

(T_a = 25°C, V_{CC} = GND = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_C = 1MHz			15	pF
Output Capacitance	C_O	Unmeasured Pins returned to 0V			15	pF
I/O Capacitance	$C_{I/O}$				15	pF

AC CHARACTERISTICS CLOCK TIMING:

(T_a = −40°C to +85°C)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} = 5.0V ±10% MIN	MAX	UNIT	V_{CC} = 2.5V to +6.0V MIN	MAX	UNIT
X1 Input Cycle Time	t_{CYX}			160	10000	ns	1.65	10	μs
X1 Input Low Level Width	t_{XXL}			75		ns	0.78		μs
X1 Input High Level Width	t_{XXH}			75		ns	0.78		μs
$Ø_{OUT}$ Cycle Time	$t_{CYØ}$			1280	80000	ns	13.2	80	μs
$Ø_{OUT}$ Low Level Width	$t_{ØØL}$			515		ns	6.35		μs
$Ø_{OUT}$ High Level Width	$t_{ØØH}$			515		ns	6.35		μs
$Ø_{OUT}$ Rise/Fall Time	t_r, t_f				120	ns		250	ns
Clock Oscillation Frequency (X1, X2)	f_{OSC}	Crystal oscillation	4.5V≦V_{CC}≦6.0V				3.5	6.25	MHz
		Ceramic oscillation	4.5V≦V_{CC}≦6.0V				0.1	6.25	MHz
			V_{CC} = 3.5V				0.1	4.0	MHz
			V_{CC} = 2.7V				0.1	0.6	MHz

READ/WRITE OPERATION

(T_a = −40°C to +85°C)

PARAMETER	SYMBOL	V_{CC} = +5.0V ±10% TEST CONDITIONS	MIN	MAX	UNIT	V_{CC} = 2.5V to +6.0V TEST CONDITIONS	MIN	MAX	UNIT
$\overline{RD}$ L.E. to $Ø_{OUT}$ L.E.	$t_{RØ}$		180		ns		3.1		μs
Address (PE_{0-15}) to Data Input	t_{AD1}			790 +660xN	ns			9.7 +6.6xN	μs
$\overline{RD}$ T.E. to Address	t_{RA}		180(T3) 840(T4)		ns		3.05(T3) 9.65(T4)		μs
$\overline{RD}$ L.E. to Data Input	t_{RD}			460 +660xN	ns			6.4 +6.6xN	μs
$\overline{RD}$ T.E. to Data Hold Time	t_{RDH}		0		ns		0		μs
$\overline{RD}$ Low Level Width	t_{RR}		1070 +660xN		ns		12.93 +6.6xN		μs
$\overline{RD}$ L.E. to $\overline{WAIT}$ L.E.	t_{RWT}			460	ns			6.4	μs
Address (PE_{0-15}) to $\overline{WAIT}$ L.E.	t_{AWT1}			790	ns			9.7	μs
$\overline{WAIT}$ Set Up Time to $Ø_{OUT}$ L.E.	t_{WTS}		370		ns		2.35		μs
$\overline{WAIT}$ Hold Time after $Ø_{OUT}$ L.E.	t_{WTH}	$t_{CYØ}$=1320ns	0		ns	$t_{cyø}$=13.2μs	0		μs
$Ø_{OUT}$ L.E. to $\overline{WR}$ L.E.	$t_{ØW}$			175	ns			0.25	μs
Address (PE_{0-15}) to $Ø_{OUT}$ T.E.	$t_{AØ}$		420		ns		6.1		μs
Address (PE_{0-15}) to Data Output	t_{AD2}		510		ns		6.4		μs
Data Output to $\overline{WR}$ T.E.	t_{DW}		740 +660xN		ns		9.35 +6.6xN		μs
$\overline{WR}$ T.E. to Data Stable Time	t_{WD}		130		ns		3.05		μs
Address (PE_{0-15}) to $\overline{WR}$ L.E.	t_{AW}		460		ns		6.35		μs
$\overline{WR}$ T.E. to Address Stable Time	t_{WA}		180		ns		3.05		μs
$\overline{WR}$ Low Level Width	t_{WW}		690 +660xN		ns		9.5 +6.6xN		μs
$\overline{WR}$ L.E. to $\overline{WAIT}$ L.E.	t_{WWT}			110	ns			3.08	μs

N: Number of T_{WAIT}

SERIAL OPERATION

(T_a = −40°C to +85°C)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} = +5.0V ± 10% MIN	MAX	UNIT	V_{CC} = +2.5V to + 6.0V MIN	MAX	UNIT
$\overline{SCK}$ Cycle Time	t_{KYK}	$\overline{SCK}$ Input	1270		ns	13.2		μs
		$\overline{SCK}$ Output	1280	80000	ns	13.2	80	μs
$\overline{SCK}$ Low Level Width	t_{KKL}	$\overline{SCK}$ Input	515		ns	6.35		μs
		$\overline{SCK}$ Output	520		ns	6.35		μs
$\overline{SCK}$ High Level Width	t_{KKH}	$\overline{SCK}$ Input	515		ns	6.35		μs
		$\overline{SCK}$ Output	520		ns	6.35		μs
SI Set Up Time to $\overline{SCK}$ T.E.	t_{SIS}		200		ns	0.3		μs
SI Hold Time after $\overline{SCK}$ T.E.	t_{SIH}		250		ns	0.5		μs
$\overline{SCK}$ L.E. to SO Delay Time	t_{KO}			300	ns		0.8	μs

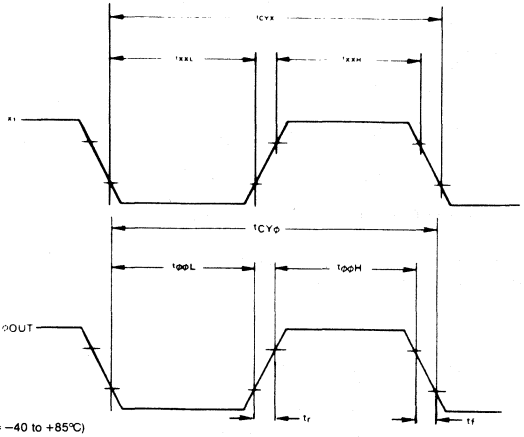
Notes 1: Input timings are measured at V_{IHMIN} and V_{ILMAX}

2: Output timings are measured at V_{OH} = 2.4V and V_{OL} = 0.45V (V_{CC} = 5.0V ± 10%) with 1TTL + 200pF load. V_{OH} = 0.7V_{CC} and V_{OL} = 0.3V_{CC} (V_{CC} = 2.5V to +6.0V)

3: L.E. = Leading Edge, T.E. = Trailing Edge

4: Use the following table (on same page) to calculate AC parameters in $t_{CY\Phi}$ 1320ns (V_{CC} = 5.0V ± 10%) resp. $t_{CY\Phi}$ 13.2 μs (V_{CC} = 2.5V to + 6.0V)

TIMING WAVEFORMS CLOCK TIMING



BUS TIMING DEPENDING ON $t_{CY\Phi}$

(T_a = −40 to +85°C)

SYMBOL	V_{CC} = +5.0V ± 10% CALCULATING EXPRESSION	MIN/MAX	UNIT	V_{CC} = +2.5V to +6.0V CALCULATING EXPRESSION	MIN/MAX	UNIT
$t_{R\Phi}$	(1/2)T − 150	MIN	ns	(1/2)T − 200	MIN	ns
t_{AD1}	(3/2+N)T − 200	MAX	ns	(3/2+N)T − 200	MAX	ns
$t_{RA(T3)}$	(1/2)T − 150	MIN	ns	(1/2)T − 250	MIN	ns
$t_{RA(T4)}$	(3/2)T − 150	MIN	ns	(3/2)T − 250	MIN	ns
t_{RD}	(1+N)T − 200	MAX	ns	(1+N)T − 200	MAX	ns
t_{RR}	(2+N)T − 250	MIN	ns	(2+N)T − 270	MIN	ns
t_{RWT}	T − 200	MAX	ns	T − 200	MAX	ns
t_{AWT1}	(3/2)T + 200	MAX	ns	(3/2)T − 200	MAX	ns
t_{WTS}	(1/3)T + 150	MIN	ns	(1/3)T + 150	MIN	ns
$t_{A\Phi}$	T − 240	MIN	ns	T − 500	MIN	ns
t_{AD2}	T − 150	MIN	ns	T − 200	MIN	ns
t_{DW}	(3/2+N)T − 250	MIN	ns	(3/2+N)T − 550	MIN	ns
t_{WD}	(1/2)T − 200	MIN	ns	(1/2)T − 250	MIN	ns
t_{AW}	T − 200	MIN	ns	T − 250	MIN	ns
t_{WA}	(1/2)T − 150	MIN	ns	(1/2)T − 250	MIN	ns
t_{WW}	(3/2+N)T − 300	MIN	ns	(3/2+N)T − 400	MIN	ns
t_{WWT}	(1/2)T − 220	MAX	ns	(1/2)T − 220	MAX	ns
t_{CYK}	2T	MIN	ns	2T	MIN	ns
t_{KKL}	T − 120	MIN	ns	T − 250	MIN	ns
t_{KKH}	T − 120	MIN	ns	T − 250	MIN	ns

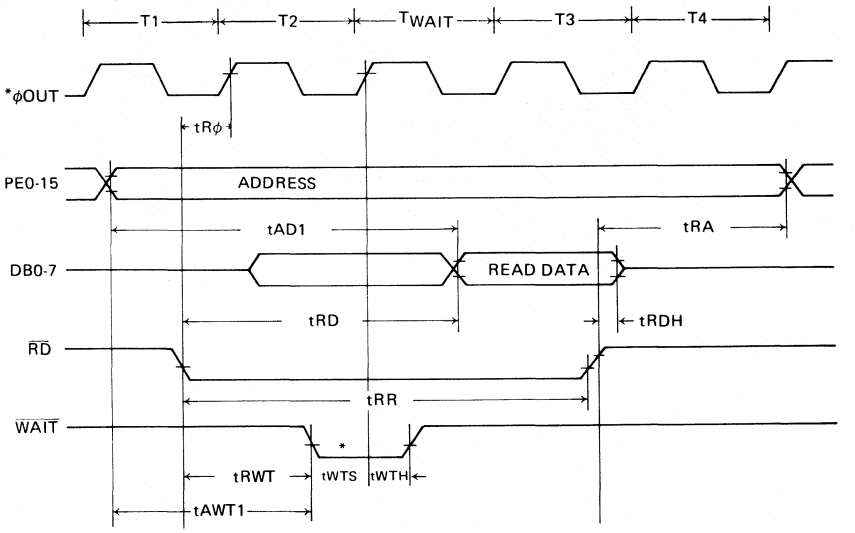
Notes 1. N = Number of T_{WAIT}

2. T = $t_{CY\Phi}$/2

3. For external clock, 50% duty cycle on X1 is assumed.

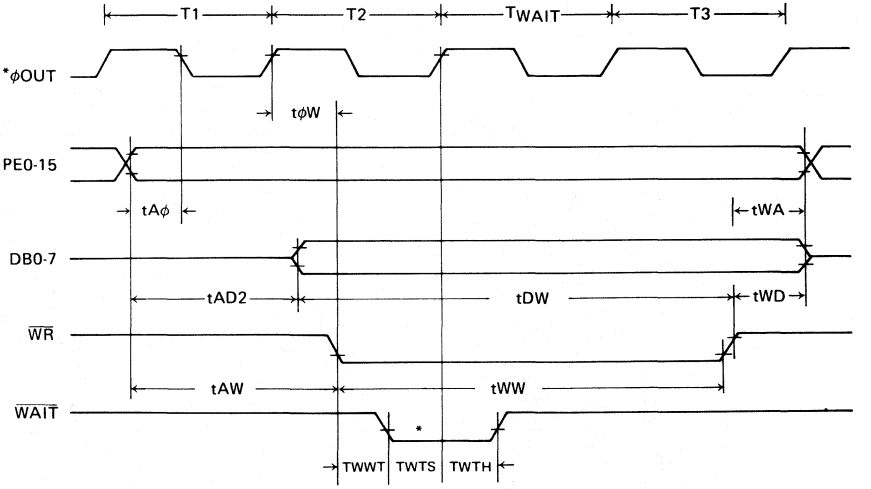
4. The items not included in this table are not dependent on $t_{CY\Phi}$.

READ OPERATION



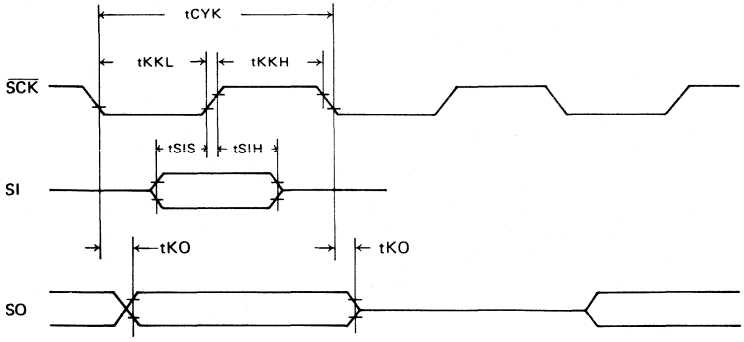
* WAIT signal must be remained stable during t_{WTS} and t_{WTH}.
If it is unstable, misoperation may occur.

WRITE OPERATION



* WAIT signal must be remained stable during t_{WTS} and t_{WTH}.
If it is unstable, misoperation may occur.

SERIAL OPERATION



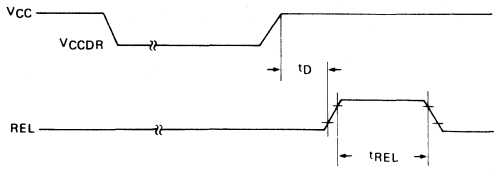
Low Power Data Memory Retention Characteristics for STOP Mode Operation

(T_a = −40 to +85°C)

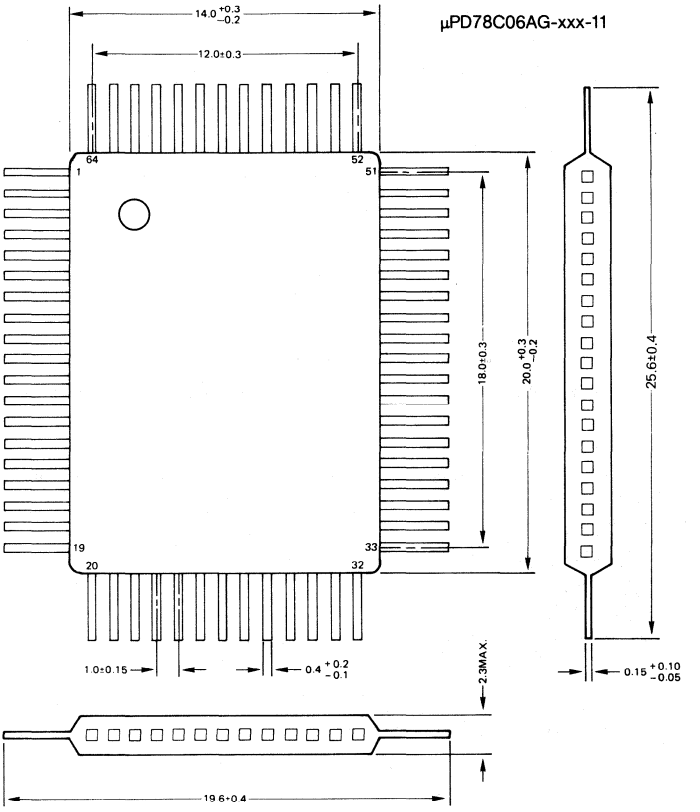
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{CCDR}		2.0			V
Data Retention Supply Current	I_{CCDR}	V_{CCDR} = 2.0V, X1 = 0V, X2 = Open		0.8	20	μA
Data Retention Input Low RES Voltage	V_{ILDR}		0		0.2 V_{CCDR}	V
Data Retention Input High $\overline{RESET}$ Voltage	V_{IHDR}		0.8 V_{CCDR}		V_{CCDR}	V
REL Input Delay Time	t_D		500			μs
REL Input High Time	t_{REL}		10			μs

Note: In data retention mode,

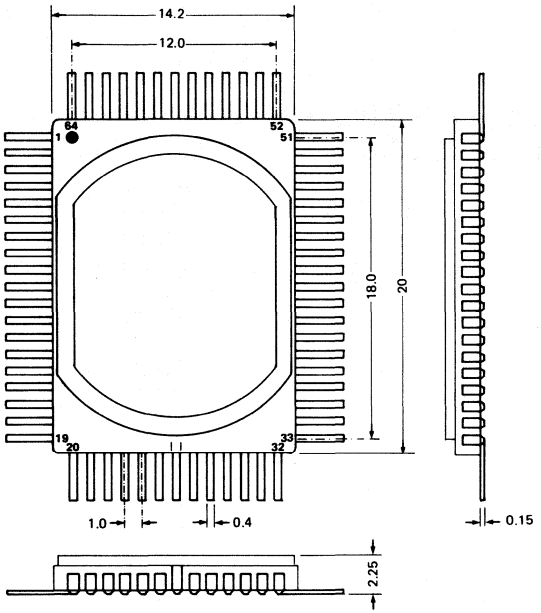
1) Input voltages to $\overline{WAIT}$ and PC_{0-5} pins (with pull-up resistors) should be maintained same as V_{CCDR} level,
2) Other input voltages should be kept less than V_{CCDR} level.

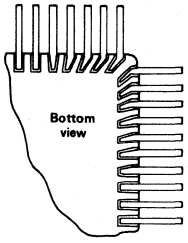


64-PIN PLASTIC FLAT PACKAGE OUTLINE, STRAIGHT LEADS (Unit : mm)
for μPD78C06AG



64-PIN CERAMIC FLAT PACKAGE OUTLINE FOR ES – REFERENCE – (Unit : mm)
for μPD78C06AG





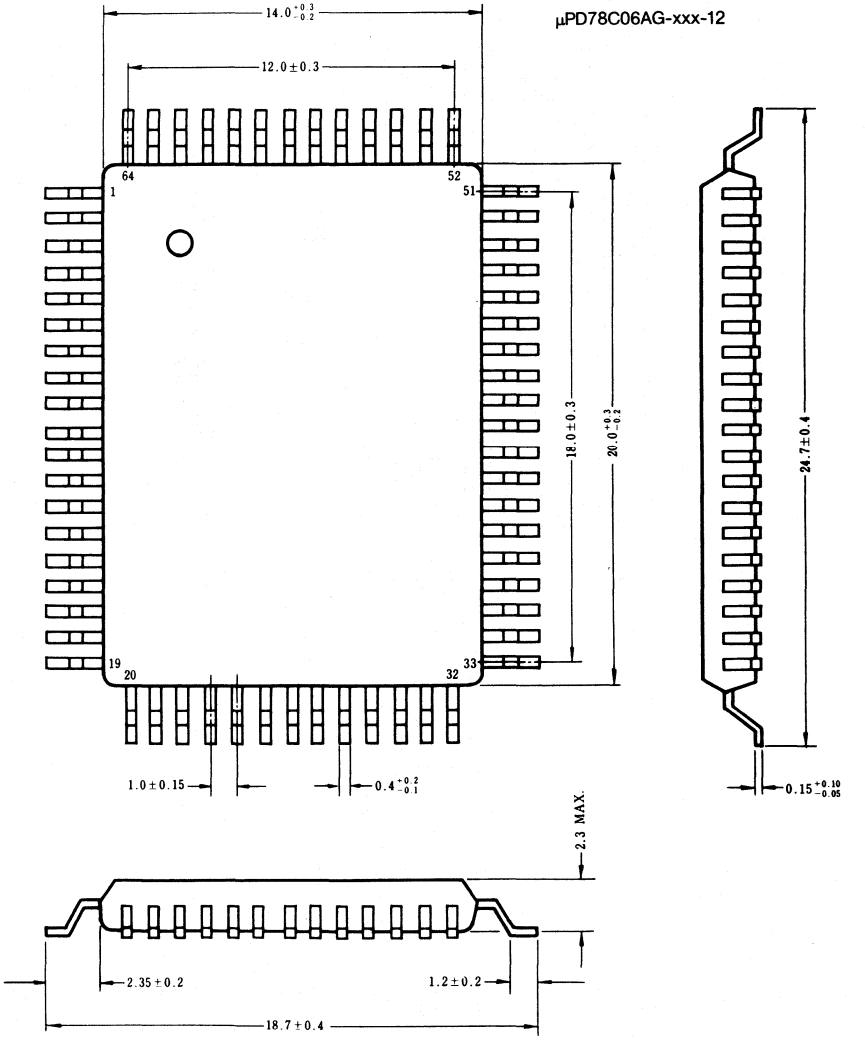
Note:

The metal cap of the device has V_{DD} (positive power supply) level because the metal cap is connected to pin No. 26 (i. e. V_{DD} pin).

The leads of the welding part at bottom of this device are formed in slant and have a chance of shorting the other lines of printed wiring board.

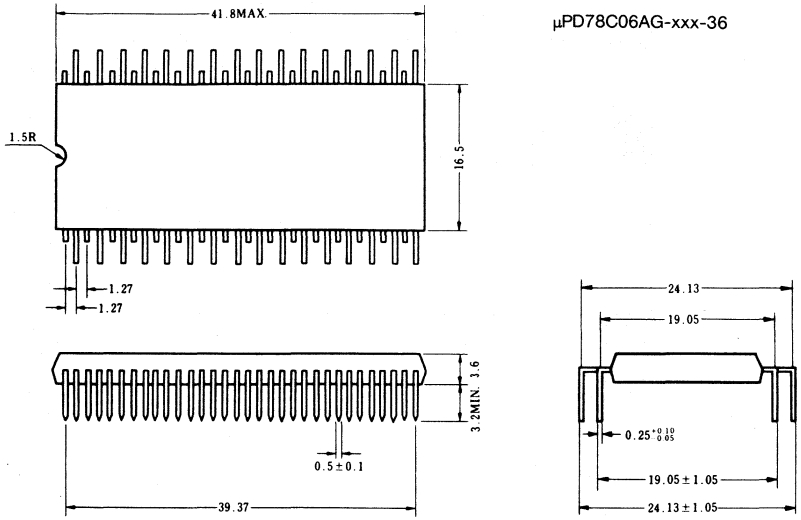
64-PIN PLASTIC FLAT PACKAGE, BENT LEADS (Unit : mm)
for μPD78C06A

μPD78C06AG-xxx-12



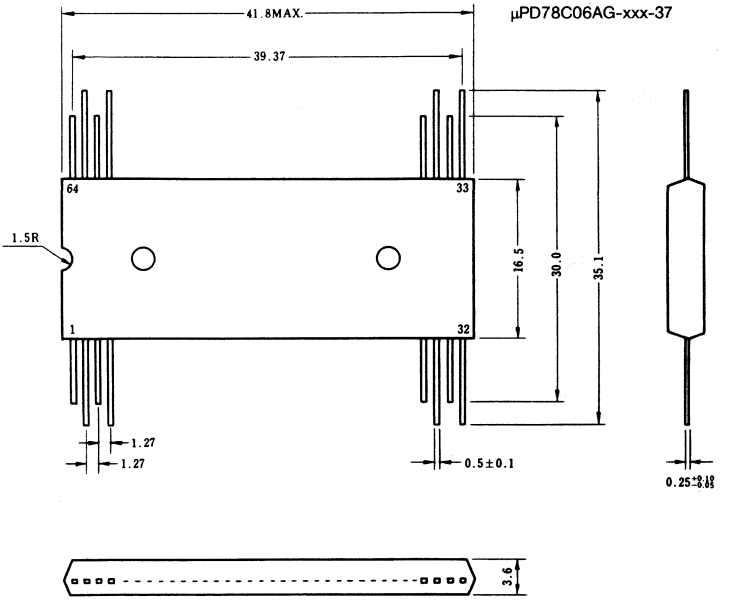
64-PIN PLASTIC QUAD-IN-LINE PACKAGE (QUIP), BENT LEADS
for μPD78C06A (Unit : mm)

μPD78C06AG-xxx-36



3

64-PIN PLASTIC QUAD-IN-LINE PACKAGE (QUIP), BENT LEADS (Unit : mm)
for μPD78C06AG



SINGLE CHIP 8-BIT MICROCOMPUTER WITH COMPARATOR INPUTS, 8K ROM

DESCRIPTION

The μPD7809/7808/7807/78P09 single chip microcomputer augments the high-end in NEC's family of 8-bit microcomputers with sophisticated on-chip peripheral functionality. Like its nearest relative in the family, the μPD7811, this device has a fast internal 16-bit ALU and data paths, 256 bytes of RAM, multifunction 16-bit timer/event counter, two 8-bit timers, a USART, and two zero-cross detect inputs. Features that distinguish this device in the NEC 8-bit family are: 8K ROM, programmable threshold comparator (8 inputs), programmable WAIT function, watchdog timer, hold and hold acknowledge for DMA interface, and bit test/write instructions for both RAM and I/O.

The μPD7809 is the 8K Byte ROM version with the customers program on chip. The μPD7808 is a 4K Byte ROM version. The μPD7807 is the ROM-less version for prototyping and small volume applications. The μPD78P09 is an EPROM version of the 8K ROM μPD7809.

FEATURES

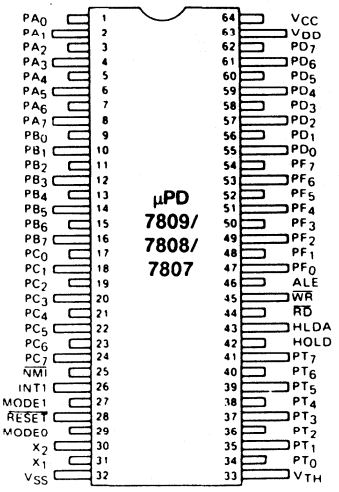
- NMOS silicon gate technology requiring + 5V supply
- Complete single chip microcomputer
  - 16-bit ALU
  - 8K ROM
  - 256 bytes RAM
- Large I/O capability
  - 40 I/O port lines (μPD7809/7808)
  - 24 I/O port lines (μPD7807)
  - 8 input lines
- Two zero-cross detect inputs
- Expansion capability (total of 64K memory access)
  - 8085A bus compatible
  - 56K bytes external memory address range
- Programmable threshold comparator
  - 8 inputs, 1 of 16 software selectable levels
- Full duplex USART
  - Synchronous, asynchronous and I/O mode
- 165 powerful instructions
  - 16-bit arithmetic, multiply and divide
- 1 μs instruction cycle time
- Prioritized interrupt structure
  - 3 external
  - 8 internal
- Hold, hold acknowledge for DMA interface
- Programmable WAIT function
- Watchdog timer
- Standby function
- On-chip clock generator
- 64-pin QUIL package/SDIP package

ORDERING INFORMATION

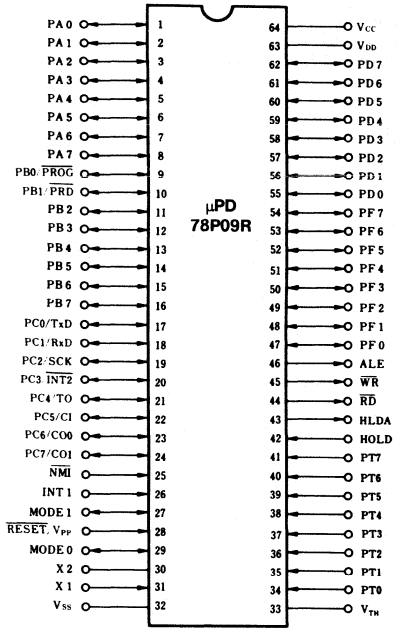
PART NUMBER	PACKAGE TYPE	ROM
μPD7807G-36	64-PIN QUIP (Bent leads)	ROM-Less
μPD7807CW-36	64-PIN SDIP	
μPD7808G-XXX-36	64-PIN QUIP (Bent leads)	4K-MASK ROM
μPD7808CW-XXX-36	64-PIN SDIP	
μPD7809G-36	64-PIN QUIP (Bent leads)	8K-MASK ROM
μPD7809CW-36	64-PIN SDIP	
μPD78P09R	64-PIN CERAMIC QUIP	8K-UV PROM
μPD78P09DW	64-PIN CERAMIC QUIP	

NOTE: QUIP = QUAD IN LINE, SDIP = SCHRINKED DUAL IN LINE,
FLAT = FLAT PACKAGE (SMD)

PIN CONFIGURATION



PIN CONFIGURATION μPD78P09R



3

PIN DESCRIPTION
μPD7809/08/07

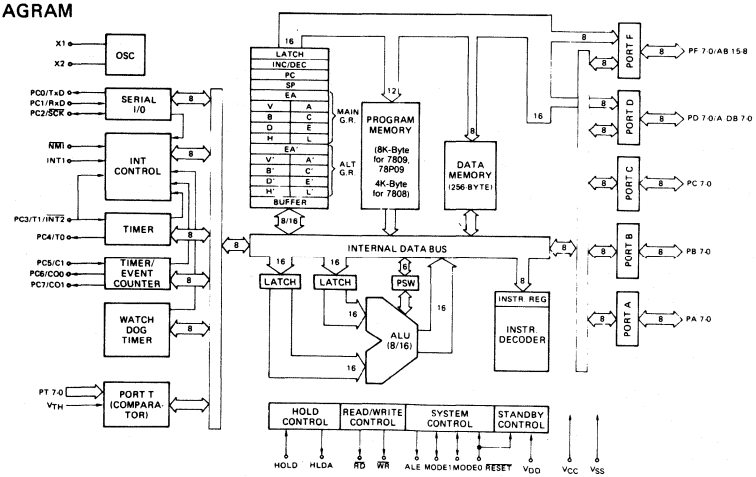
PIN NO.	PIN SYMBOL	FUNCTION	
1–8	PA_0–PA_7	Port A: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port A in input mode.	
9–16	PB_0–PB_7	Port B: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port B in input mode.	
17	PC_0	Port C: (Three-state input/output) 8-bit programmable I/O port. Each line independently pro-programmable as an input or output. Alternatively, Port C may be used as control lines for USART and timer counter and interrupt. Reset puts Port C in Port mode and all lines in input mode.	Transmit Data (TxD): Serial data output terminal.
18	PC_1		Receive Data (RxD): Serial data input terminal.
19	PC_2		Serial Clock (SCK): Serial clock input/output terminal. When internal clock is used, the output can be selected; when an external clock is used, the input can be selected.
20	PC_3		Timer Input ((TI)/interrupt request input (INT_2): Timer clock input terminal; can also be used as falling edge, maskable-interrupt input terminal and AC input zero-cross detection terminal.
21	PC_4		Timer Output (TO): This output signal is a square wave whose frequency is determined by the timer/counter.
22	PC_5		Counter Input (CI): External pulse input terminal to the timer/event counter.
23–24	PC_6, PC_7		Counter Outputs 0, 1 (CO_0–CO_1): Programmable rectangular wave output terminal based on timer/event counter.
25	NMI	Falling-edge, nonmaskable interrupt (NMI) input.	
26	INT_1	This signal is a rising-edge, maskable interrupt input. This input is also used to make the zero-cross detection AC input.	
27	MODE1	Used as input in conjunction with MODE0 to select appropriate memory expansion mode. Also outputs M1 Signal during each opcode fetch.	
28	RESET	(Input, active low), RESET initializes the μPD7809.	
29	MODE0	Used as input in conjunction with MODE1 to select appropriate memory expansion mode. Also used to output IO/M.	
30–31	X_2, X_1 (crystal)	This is a crystal connection terminal for system clock oscillation. When an external clock is supplied X_1 is the input.	
32	V_{SS}	Power supply ground potential.	
33	V_{TH}	V_{TH} threshold voltage input. Reference voltage for variable threshold input, Port T. Threshold voltage to each Port T input is software programmable to 16 different levels.	

PIN DESCRIPTION (cont.)

PIN NO.	PIN SYMBOL	FUNCTION
34–41	PT_1–PT_7	Eight variable threshold input ports. Ports T_0–T_7 inputs are each connected internally to comparators where the other input is the threshold voltage.
42	HOLD	HOLD request input. When high, CPU is in a HOLD state until HOLD goes low.
43	HLDA	HOLD Acknowledge output by CPU when HOLD state is accepted; goes low when HOLD is released.
44	RD	(Three-state output, active low) RD is used as a strobe to gate data from external devices onto the data bus. RD goes high during Reset.
45	WR	(Three-state output, active low) WR, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. WR goes high during Reset.
46	ALE	The strobe signal is for latching the address signal to the output from PD_7–PD_0 when accessing external expansion memory.
47–54	PF_0–PF_7	Port F: (Three-state input/output) 8-bit programmable I/O port. Each line configurable independently as an input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
55–62	PD_0–PD_7	Port D: 8-bit programmable I/O port. This byte can be designated as either input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
63	V_{DD}	This is a backup power terminal for on-chip RAM.
64	V_{CC}	+5V power supply.

Notes: 1 clock cycle = 1 CL = 3/f.
1 machine cycle = 3 or 4 clock cycles.
1 instruction cycle = 1 to 19 machine cycles.
f: System clock frequency (MHz).

BLOCK DIAGRAM



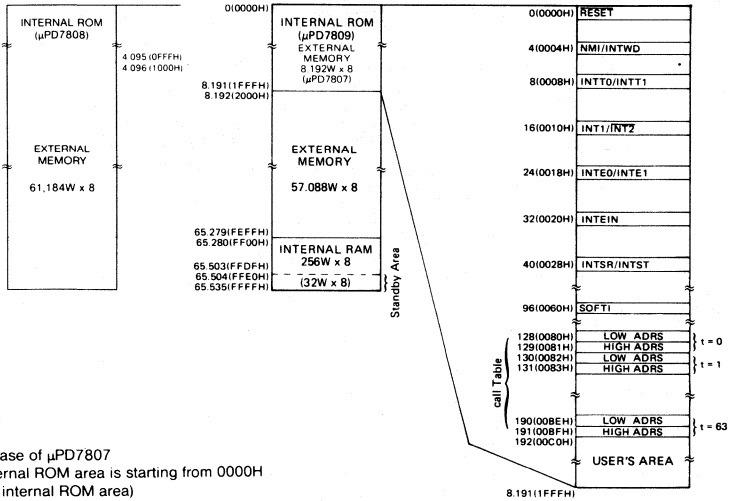
Note: The μPD7807 has no on chip ROM

INSTRUCTION SET

In addition to the basic 7800 family instruction set, the following instructions are incorporated in the μPD7809/7808/7807

- 16-bit data transfer between memory, registers, and extended accumulator
- 16-bit addition and subtraction
- 16-bit comparison and skip
- 16-bit and, or, ex-or operation
- 16-bit data shift and rotation
- Multiply
  8-bit by 8-bit, 16-bit product
  Less than 8 μs execution-time
- Divide
  16-bit by 8-bit, 16-bit quotient, 8-bit remainder
  Less than 14 μs execution-time
- Working register instructions for efficient RAM addressing, testing and manipulating
- Direct bit addressing for code-efficient addressing, testing and manipulating bits in RAM, port lines and mode registers

MEMORY MAP



In case of μPD7807
external ROM area is starting from 0000H
(no internal ROM area)

FUNCTIONAL DESCRIPTION

Please refer to the section of μPD7811 for description of the following functions which are the same as on this device:

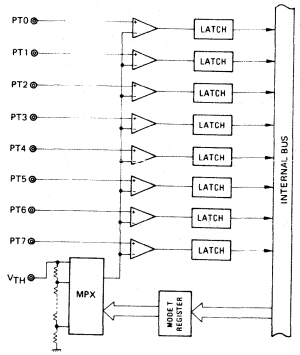
1. Memory expansion (except 56K bytes maximum for μPD7809)
2. USART
3. Reset
4. External memory access and timing

Variable Threshold Input Port (Port T)

- 8 input lines
- 16 levels – from 1/16 of reference voltage (V_{TH}) to 16/16 V_{TH}
- Level selected by software write to Mode T register
- Input at Port bit reads 0 until voltage at pin exceeds selected level
- Comparison execution time: 12 μs

FUNCTIONAL DESCRIPTION (CONT.)

Block Diagram of Threshold Variable Input Port



Format of MODE T Register

7	6	5	4	3	2	1	0
–	–	–	–	MT3	MT2	MT1	MT0

Specification of 16 Threshold Levels

0	0	0	0	V_{TH} x 16/16
0	0	0	1	V_{TH} x 1/16
0	0	1	0	V_{TH} x 2/16
0	0	1	1	V_{TH} x 3/16
0	1	0	0	V_{TH} x 4/16
0	1	0	1	V_{TH} x 5/16
0	1	1	0	V_{TH} x 6/16
0	1	1	1	V_{TH} x 7/16
1	0	0	0	V_{TH} x 8/16
1	0	0	1	V_{TH} x 9/16
1	0	1	0	V_{TH} x 10/16
1	0	1	1	V_{TH} x 11/16
1	1	0	0	V_{TH} x 12/16
1	1	0	1	V_{TH} x 13/16
1	1	1	0	V_{TH} x 14/16
1	1	1	1	V_{TH} x 15/16

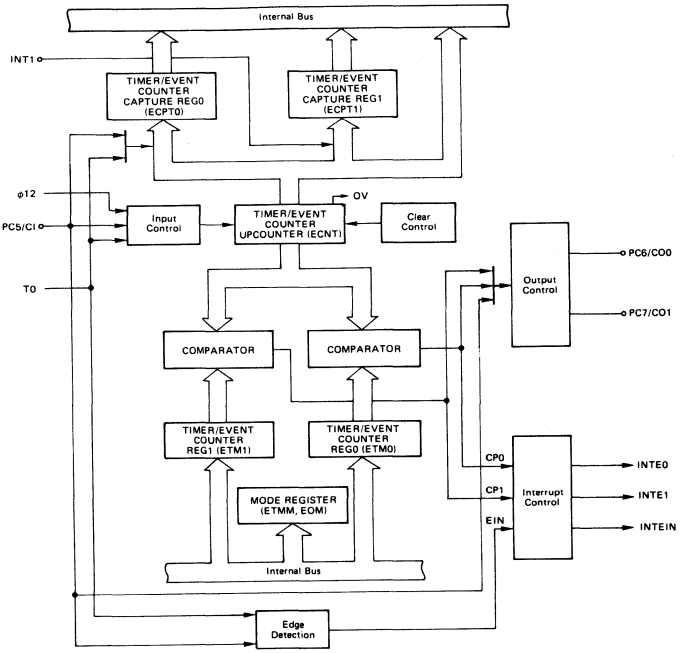
3

Input/Output

- 40 digital I/O lines – Five 8-bit ports (Port A, Port B, Port C, Port D, Port F)
- Port operation for Ports A, B, C and F: Each line of these ports can be individually programmed as an input or as an output
- Port D can be programmed as a byte input or a byte output
- Control lines: Under software control, each line of Port C can be configured individually to provide control lines for serial interface timer and timer/counter and interrupt.

FUNCTIONAL DESCRIPTION (CONT.)

TIMER / EVENT COUNTER – BLOCK DIAGRAM



Note: $\phi 12 = f_{XTAL} \times 1/12$,

f_{XTAL} : oscillation frequency

Input Clock of TIMER/EVENT COUNTER: Internal ($\phi 12$)
External (CI)
Timer out (TO)

Operations:

a) Interval Timer:
Counter repeats interruptions due to a present count time.

b) Event Count Mode:
CI inputs are synchr. by the internal clock. 250ns noise detection.

c) Frequency Measurement Mode:
CI inputs while TO is kept at high level.

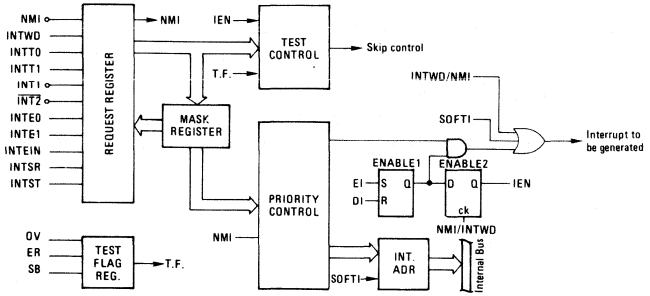
d) Puls with Meaurement Mode:
Counting up the upcounter during CI is high or low.

e) Programmable Square Wave:
Comperator 0 signal sets $CO_{0/1}$. Comperator 1 signal reset $CO_{0/1}$.

f) Single Pulse Generation:
CI is trigger input 16 bit counter free running output Flip-Flop toggled two times.

FUNCTIONAL DESCRIPTION (CONT.)

INTERRUPT CONTROL CIRCUITRY – BLOCK DIAGRAM



Mask register: Masking the interrupts

Priority control: Accepts only the interrupt with the highest priority if more than one request at the same time.

Test Flag register: 3 kinds of test flags which doesn't bring any interrupt request:

OV: set to 1 by overflow of the timer/event counter
ER: set to 1 by priority error
SB: set to 1 by rise input of V_{DD} terminal

3

INTERRUPT

11 Interrupt Sources

3 External Interrupts – Including non maskable interrupt
8 Internal Interrupts

6 Priority Levels and 6 Interrupt Vectors

11 Interrupt sources are divided into 6 priority levels.

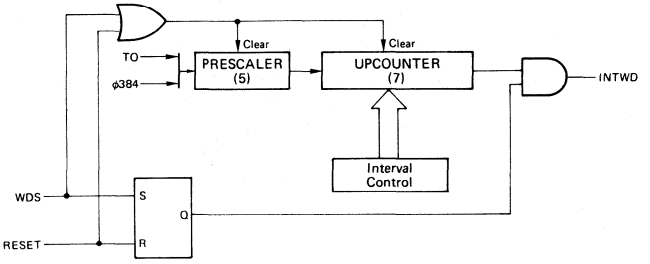
PRIORITY	INTERRUPT ADDRESS	INTERRUPT SOURCE		INTERNAL/ EXTERNAL
1	4 (0004H)	$\overline{NMI}$	falling edge	external
		INTWD	output signal of watchdog timer	internal
2	8 (0008H)	INTT0	coincidence signal from TIMER0	internal
		INTT1	coincidence signal from TIMER1	
3	16 (0010H)	INT1	rising edge	external
		$\overline{INT2}$	falling edge	
4	24 (0018H)	INTE0	coincidence signal from timer/ event counter	internal
		INTE1	coincidence signal from timer/ event counter	
5	32 (0020H)	INTEIN	falling edge of CI or TO	internal
6	40 (0028H)	INTSR	serial receive interrupt	internal
		INTST	serial transmit interrupt	

FUNCTIONAL DESCRIPTION (CONT.)

WATCHDOG TIMER

Used for software safety check or overall performance safety check. Watchdog, if enabled, must be cleared at regular intervals in program execution to avoid watchdog interrupt or by Reset. Intervals are software selectable.

BLOCK DIAGRAM OF WATCHDOG TIMER



Note: $\phi 384 = f_{XTAL} \times 1/384$

HOLD/HLDA

To perform all sorts of DMA-applications a Hold-request signal can be applied to the μPD7809; it puts Address- and Databus and RD/WR signal lines to the high impedance state. Then HLDA goes high as a response to the hold request.

MODE0/MODE1-TERMINALS

The logic level applied to M0/M1-Terminals determines the memory map of μPD7807/08/09 and the use of Port D/F as multiplexed Address/Data Bus.

M0	M1	MEMORY	ADDRESSES	LOCATION
0	1	4K/ 8K	0 . . . . . 0FFFH/1FFFH	internal*
0	0	4K	0 . . . . . ,OFFFH	external
0	1	16K	0 . . . . . 3FFFH	external
1	0	64K	0 . . . . . FEFFH	external

* M0, M1 = 0,1 realizes the ROM version (access of internal ROM), all others represent access of external memory only. In case external memory is used in addition to internal, memory mapping register has to be programmed then (see below).

MEMORY EXPANDES MODES	MEMORY MAPPING REGISTER MM2	MM1	MM0	NUMBER OF I/O LINES
Port Mode	0	0	X	44
256 Expanded	0	1	0	36
4K Expanded	1	0	0	32
16K Expanded	1	1	0	30
56K/60K* Expanded	1	1	1	28

*56K for 7809, 60K for 7808

FUNCTIONAL DESCRIPTIONS (CONT.)

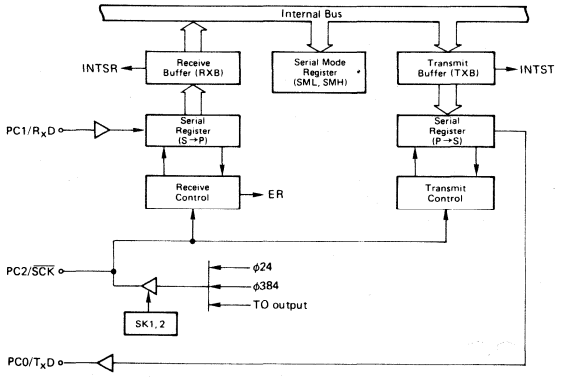
STANDBY FUNCTION

The μPD7809/08/07/P09 offers a standby function that allows the user to save up to 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On powerup the μPD7809 checks whether recovery was made from standby mode or from cold start.

UNIVERSAL SERIAL INTERFACE

The serial interface can operate in any of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first for ease of communication with certain peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception. In the search mode, data is transferred one bit at a time from serial register to receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from serial register to transmit buffer occurs 8 bits at a time.

UNIVERSAL SERIAL INTERFACE BLOCK DIAGRAM



Note: $\phi 24 = f_{XTAL} \times 1/24$

$\phi 384 = f_{XTAL} \times 1/384$ f_{XTAL}: oscillation frequency (MHz)

- Asynchronous Mode
  - Full-Duplex, Double Buffering
  - 7, 8-Bit/Character
  - Start/Stop Bit
  - Even/Odd Parity
  - Programmable Clock Rate X1, X16, X64
- Synchronous Mode
  - Search/Receive Mode
- I/O Interface Mode (μPD7801 Serial Mode)
- Programmable Communication Rate
  - 2μsec, 32μsec, Timer and External

3

FUNCTIONAL DESCRIPTION (CONT.)

ZERO-CROSSING DETECTOR

The INT1 and INT2 terminals (used common to TI and PC_3) can be used to detect the zero-crossing point of slow moving AC signals. When driven directly, these pins respond as a normal digital input.

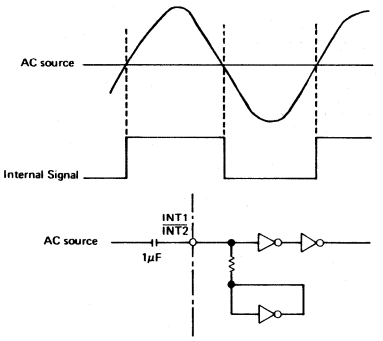
To utilize the zero-cross detection mode, an AC signal of approximately 1–3V AC peak-to-peak magnitude and a maximum frequency of 1kHz is coupled through an external capacitor to these pins.

For the INT1 pin, the internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one and INT1 interrupt is generated.

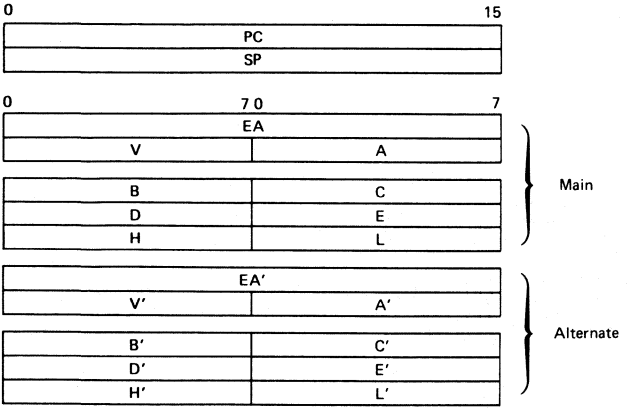
For the INT2 pin, the state is sensed as a one until the falling edge crosses the DC average level, when it becomes a zero and INT2 interrupt is generated.

The zero-cross detection capability allows the user to make the 50–60Hz power signal the basis for system timing and to control voltage phase sensitive devices.

ZERO-CROSSING DETECTION CIRCUIT



REGISTERS



FUNCTIONAL DESCRIPTION (CONT.)

General Purpose Registers (B, C, D, E, H. L)

There are two sets of general purpose registers (Main: B, C, D, E, H, L: Alternate: B', C', D', H', L'). They can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL, B'C', D'E', H'L'). Auto Increment and Decrement addressing mode capabilities extend the uses for the DE, HL, D'E', and H'L' register-pairs. The contents of the BC, DE, and HL register-pairs can be exchanged with their Alternate Register counterparts using the EXX instruction.

Vector Register (V)

When defining a scratch pad area in the memory space, the upper 8-bit memory address is defined in the V-register and the lower 8-bits is defined by the immediate data of an instruction. Also the scratch pad indicated by the V-register can be used as 256 x 8-bit working registers for storing software flags, parameters and counters.

Accumulator (A)

All data transfers between the μPD7809 and external memory of I/O are done through the accumulator. The contents of the Accumulator and Vector Registers can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A reset sets the PC to 0000_H.

Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

3

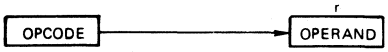
Extended Accumulator (EA)

The data processings of 16-bit arithmetic and logical operation instructions are mainly handled in the extended accumulator.

ADDRESS MODES

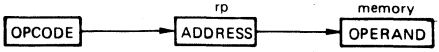
Register Addressing	Working Register Addressing
Register Indirect Addressing	Direct Addressing
Auto-Increment Addressing	Immediate Addressing
Auto-Decrement Addressing	Immediate Extended Addressing
Double Auto-Increment Addressing	Base Addressing
Relative Addressing	Base-Index-Addressing

Register Addressing



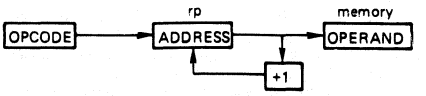
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



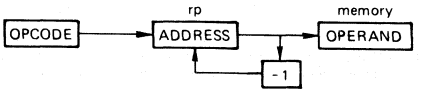
The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

Auto-Increment Addressing

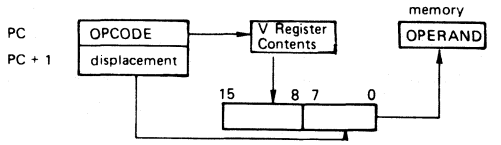


The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

Auto Decrement Addressing

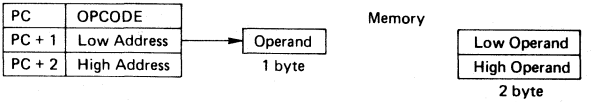


Working Register Addressing



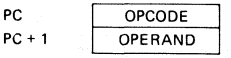
The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix ending this address mode.

Direct Addressing

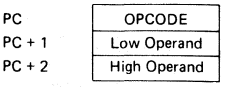


The two bytes following the opcode specify an address of a location containing the operand.

Immediate Addressing

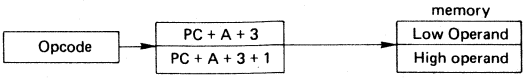


Immediate Extended Addressing



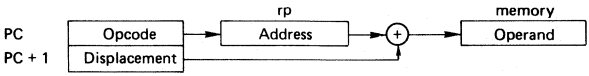
FUNCTIONAL DESCRIPTIONS (CONT.)

Relative Addressing



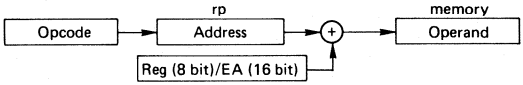
This addressing mode is used by the "Table"-command. It transfers the contents of 2 memory cells – addressed relatively to PC via the Accu A – into BC register-pair (TABLE-command).
Application: Table look-up

Base-Addressing



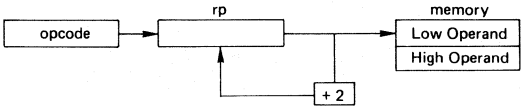
Register Pair DE or HL used as base pointer to the memory; immediate data (8 bit) or displacement added to the base.

Base-Index-Addressing



Register pair DE or HL used as base pointers to the memory; Register (8 bit) or Extended Accumulator (EA) as displacement added to the base.

Double auto increment



The opcode specifies the register pair which contains the memory address of the operand (16-bit). The contents of the register pair is automatically incremented by two to point to a new 16-bit operand.

FUNCTIONAL DESCRIPTION (CONT.)

BIT ADDRESS INSTRUCTIONS

The following bits may be addressed directly with certain instructions:

- Any bit in a 16-byte group in RAM
- Any bit in the five 8-bit I/O ports (A, B, C, D, F)
- Any bit in the variable threshold port
- Any bit in the following special registers:

  9-bit interrupt mask register, serial mode register, timer mode register, timer/event counter output register

An addressed bit may be tested, set, cleared, or complemented.
An addressed bit may be moved to or from the carry flag.
An addressed bit may be ANDed, ORed, X-ORed with the carry flag.

Difference between the μPD7801, μPD7811, μPD7807, and μPD7809

		μPD7801	μPD7811	μPD7807	μPD7809
Number of Instructions		134	158	165	165
16-Bit Operation Instruction		No	Yes	Yes	Yes
Multipy/Divide Instruction		No	Yes	Yes	Yes
Instruction Cycle		2μs/4MHz	1μs/12MHz	1μs/12MHz	1μs/12MHz
Number of General-purpose Registers		16	18	18	18
On-chip ROM Capacity		4K Bytes	4K Bytes	No	8K Bytes
On-chip RAM Capacity		128 Bytes	256 Bytes	256 Bytes	256 Bytes
Direct-Addressable External Memory Capacity		60K Bytes	60K Bytes	64K Bytes	56K Bytes
Interrupt Source	Internal	2	8	8	8
	External	3	3	3	3
I/O Lines		48	40+4	28*	40
Threshold Variable Port		No	No	8 Bits	8 Bits
Timer/Counter	Timer	12 Bits	8 Bits x 2	8 Bits x 2	8 Bits x 2
	Counter	No	16 Bits	16 Bits	16 Bits
Watchdog Timer		No	No	Yes	Yes
Serial Interface	Asynchronous	No	Yes	Yes	Yes
	Synchronous	No	Yes	Yes	Yes
	I/O Interface	Yes	Yes	Yes	Yes
A/D Converter		No	Yes	No	No
Standby Function		No	Yes	Yes	Yes
Hold Function		Yes	no	Yes	Yes
Technology		NMOS	NMOS	NMOS	NMOS
Package		64-Pin QUIP	64-Pin QUIP	64-Pin QUIP	64-Pin QUIP

*: at 4K-byte Access

OPERAND FORMAT/DESCRIPTION

FORMAT	DESCRIPTION
r	V, A, B, C, D, E, H, L
r1	EAH, EAL, B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, PD, PF, MKH, MKL, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TXB, TM0, TM1, WDM, MT
sr1	PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM, PT, RXB, WDM
sr2	PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM
sr3	ETM0, ETM1
sr4	ECNT, ECPT0, ECPT1
sr5	PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM, PT
rp	SP, B, D, H
rp1	V, B, D, H, EA
rp2	SP, B, D, H, EA
rp3	B, D, H
rpa	B, D, H, D+, H+, D−, H−
rpa1	B, D, H
rpa2	B, D, H, D+, H+, D−, H−, D+byte, H+A, H+B, H+EA, H+byte
rpa3	D, H, D++, H++, D+byte, H+A, H+B, H+EA, H+byte
wa	8 bit immediate data
word	16 bit immediate data
byte	8 bit immediate data
bit	8 bit immediate data
f	CY, HC, Z
irf	FNMI, FT0, FT1, F1, F2, FE0, FE1, FEIN, FSR, FST, ER, OV, IFE2, SB

REMARKS

1. sr ~ sr5 (special register)

PA	:	PORT A
PB	:	PORT B
PC	:	PORT C
PD	:	PORT D
PF	:	PORT F
PT	:	PORT T
MA	:	MODE A
MB	:	MODE B
MC	:	MODE C
MCC	:	MODE CONTROL C
MF	:	MODE F
MM	:	MEMORY MAPPING
MT	:	MODE T
TM0	:	TIMER REG0
TM1	:	TIMER REG1
TMM	:	TIMER MODE
ETM0	:	TIMER/EVENT COUNTER REG0
ETM1	:	TIMER/EVENT COUNTER REG1
ECNT	:	TIMER/EVENT COUNTER UPCOUNTER
ECPT0	:	TIMER/EVENT COUNTER CAPTURE0
ECPT1	:	TIMER/EVENT COUNTER CAPTURE1
ETMM	:	TIMER/EVENT COUNTER MODE
EOM	:	TIMER/EVENT COUNTER OUTPUT MODE
WDM	:	WATCHDOG TIMER MODE
TXB	:	Tx BUFFER
RXB	:	Rx BUFFER
SMH	:	SERIAL MODE High
SML	:	SERIAL MODE Low
MKH	:	MASK High
MKL	:	MASK Low

2. rp ~ rp3 (register pair)

SP	:	STACK POINTER
B	:	BC
D	:	DE
H	:	HL
V	:	VA
EA	:	EXTENDED ACCUMULATOR

3. rpa ~ rpa3 (rp addressing)

B	:	(BC)
D	:	(DE)
H	:	(HL)
D+	:	(DE)+
H+	:	(HL)+
D−	:	(DE)−
H−	:	(HL)−
D++	:	(DE)++
H++	:	(HL)++
D+byte	:	(DE+byte)
H+A	:	(HL+A)
H+B	:	(HL+B)
H+EA	:	(HL+EA)
H+byte	:	(HL+byte)

4. f (flag)

CY	:	CARRY
HC	:	HALF CARRY
Z	:	ZERO

5. irf (interrupt flag)

FMMI	:	INTFNMI
FT0	:	INTFT0
FT1	:	INTFT1
F1	:	INTF1
F2	:	INTF2
FE0	:	INTFE0
FE1	:	INTFE1
FEIN	:	INTFEIN
FSR	:	INTFSR
FST	:	INTFST
ER	:	ERROR
OV	:	OVERFLOW
IEF2	:	INTERRUPT ENABLE F/F2
SB	:	STANDBY

Parts of this material may be changed without prior notice due to the introduction of new functions of products under development.

INSTRUCTION SET

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
8-BIT DATA TRANSFER	MOV		r1, A	0 0 0 1 1 T_2 T_1 T_0				4	r1 ← A	
			A, r1	0 0 0 0 1 T_2 T_1 T_0				4	A ← r1	
		*	sr, A	0 1 0 0 1 1 0 1	1 1 S_5 S_4 S_3 S_2 S_1 S_0			10	sr ← A	
		*	A, sr1	0 1 0 0 1 1 0 0	1 1 S_5 S_4 S_3 S_2 S_1 S_0			10	A ← sr1	
			r, word	0 1 1 1 0 0 0 0	0 1 1 0 1 R_2 R_1 R_0	Low Adrs	High Adrs	17	r ← (word)	
			word, r	0 1 1 1 0 0 0 0	0 1 1 1 1 R_2 R_1 R_0	Low Adrs	High Adrs	17	(word) ← r	
		*	r, byte	0 1 1 0 1 R_2 R_1 R_0	Data			7	r ← byte	
	MVI		sr2, byte	0 1 1 0 0 1 0 0	S_3 0 0 0 0 S_2 S_1 S_0	Data		14	sr2 ← byte	
	MVIW	*	wa, byte	0 1 1 1 0 0 0 1	Offset	Data		13	(V.wa) ← byte	
	MVIX	*	rpa1, byte	0 1 0 0 1 0 A_1 A_0	Data			10	(rpa1) ← byte	
	STAW	*	wa	0 1 1 0 0 0 1 1	Offset			10	(V.wa) ← A	
	LDAW	*	wa	0 0 0 0 0 0 0 1	Offset			10	A ← (V.wa)	
	STAX	*	rpa2	A_3 0 1 1 1 A_2 A_1 A_0	Data (*1)			7/13	(rpa2) ← A	
	LDAX	*	rpa2	A_3 0 1 0 1 A_2 A_1 A_0	Data (*1)			7/13	A ← (rpa2)	
	EXX			0 1 0 0 1 0 0 0	1 0 1 0 1 1 1 1			8	B ↔ B', C ↔ C', D ↔ D', E ↔ E', H ↔ H', L ↔ L'	
	EXA			0 1 0 0 1 0 0 0	1 0 1 0 1 1 0 0			8	V, A ↔ V', A', EA ↔ EA'	
	EXH			0 1 0 0 1 0 0 0	1 0 1 0 1 1 1 0			8	H, L ↔ H', L'	
	EXR			0 1 0 0 1 0 0 0	1 0 1 0 1 1 0 1			8	V ↔ V', A ↔ A', B ↔ B', C ↔ C', D ↔ D', E ↔ E', H ↔ H', L ↔ L', EA ↔ EA'	

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
16-BIT DATA TRANSFER	BLOCK		D+	0 0 0 1 0 0 0 0				13* (C+1)	(DE)+ ← (HL)+, C ← C−1 End if borrow	
			D−	0 0 0 1 0 0 0 1				13* (C+1)	(DE)− ← (HL)−, C ← C−1 End if borrow	
	DMOV		rp3, EA	1 0 1 1 0 1 P_1 P_0				4	$rp3_L$ ← EAL, $rp3_H$ ← EAH	
			EA, rp3	1 0 1 0 0 1 P_1 P_0				4	EAL ← $rp3_L$, EAH ← $rp3_H$	
			sr3, EA	0 1 0 0 1 0 0 0	1 1 0 1 0 0 1 U_0			14	sr3 ← EA	
			EA, sr4	↓ ↓	1 1 0 0 0 0 V_1 V_0			14	EA ← sr4	
	SBCD		word	0 1 1 1 0 0 0 0	0 0 0 1 1 1 1 0	Low Adrs	High Adrs	20	(word) ← C, (word+1) ← B	
	SDED		word		0 0 1 0 1 1 1 0			20	(word) ← E, (word+1) ← D	
	SHLD		word		0 0 1 1 1 1 1 0			20	(word) ← L, (word+1) ← H	
	SSPD		word	↓ ↓	0 0 0 0 1 1 1 0	↓ ↓		20	(word) ← SP_L, (word+1) ← SP_H	
	STEAX		rpa3	0 1 0 0 1 0 0 0	1 0 0 1 C_3 C_2 C_1 C_0	Data (*2)		14/20	(rpa3) ← EAL, (rpa3+1) ← EAH	
	LBCD		word	0 1 1 1 0 0 0 0	0 0 0 1 1 1 1 1	Low Adrs	High Adrs	20	C ← (word), B ← (word+1)	
	LDED		word		0 0 1 0 1 1 1 1			20	E ← (word), D ← (word+1)	
	LHLD		word		0 0 1 1 1 1 1 1			20	L ← (word), H ← (word+1)	
	LSPD		word	↓ ↓	0 0 0 0 1 1 1 1	↓ ↓		20	SP_L ← (word), SP_H ← (word+1)	
	LDEAX		rpa3	0 1 0 0 1 0 0 0	1 0 0 0 C_3 C_2 C_1 C_0	Data (*2)		14/20	EAL ← (rpa3), EAH ← (rpa3+1)	
	PUSH		rp1	1 0 1 1 0 Q_2 Q_1 Q_0				13	(SP−1) ← $rp1_H$, (SP−2) ← $rp1_L$ SP ← SP−2	
	POP		rp1	1 0 1 0 0 Q_2 Q_1 Q_0				10	$rp1_L$ ← (SP), $rp1_H$ ← (SP+1) SP ← SP+2	
	LXI	*	rp2, word	0 P_2 P_1 P_0 0 1 0 0	Low Byte	High Byte		10	rp2 ← word	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
	TABLE		01001000	10101000			17	C ← (PC+3+A) B ← (PC+3+A+1)	
8-BIT ARITHMETIC (REGISTER)	ADD	A, r	01100000	11000 R_2 R_1 R_0			8	A ← A+r	
		r, A		01000 R_2 R_1 R_0			8	r ← r+A	
	ADC	A, r		11010 R_2 R_1 R_0			8	A ← A+r+CY	
		r, A		01010 R_2 R_1 R_0			8	r ← r+A+CY	
	ADDNC	A, r		10100 R_2 R_1 R_0			8	A ← A+r	No Carry
		r, A		00100 R_2 R_1 R_0			8	r ← r+A	No Carry
	SUB	A, r		11100 R_2 R_1 R_0			8	A ← A−r	
		r, A		01100 R_2 R_1 R_0			8	r ← r−A	
	SBB	A, r		11110 R_2 R_1 R_0			8	A ← A−r−CY	
		r, A		01110 R_2 R_1 R_0			8	r ← r−A−CY	
	SUBNB	A, r		10110 R_2 R_1 R_0			8	A ← A−r	No Borrow
		r, A		00110 R_2 R_1 R_0			8	r ← r−A	No Borrow
	ANA	A, r		10001 R_2 R_1 R_0			8	A ← A ∧ r	
		r, A		00001 R_2 R_1 R_0			8	r ← r ∧ A	
	ORA	A, r		10011 R_2 R_1 R_0			8	A ← A ∨ r	
		r, A		00011 R_2 R_1 R_0			8	r ← r ∨ A	
	XRA	A, r		10010 R_2 R_1 R_0			8	A ← A ∨̄ r	
		r, A		00010 R_2 R_1 R_0			8	r ← r ∨̄ A	
	GTA	A, r		10101 R_2 R_1 R_0			8	A−r−1	No Borrow
		r, A	▼ ▼	00101 R_2 R_1 R_0			8	r−A−1	No Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
8-BIT ARITHMETIC (REG.)	LTA	A, r	01100000	10111 R_2 R_1 R_0			8	A−r	Borrow
		r, A		00111 R_2 R_1 R_0			8	r−A	Borrow
	NEA	A, r		11101 R_2 R_1 R_0			8	A−r	No Zero
		r, A		01101 R_2 R_1 R_0			8	r−A	No Zero
	EQA	A, r		11111 R_2 R_1 R_0			8	A−r	Zero
		r, A		01111 R_2 R_1 R_0			8	r−A	Zero
	ONA	A, r		11001 R_2 R_1 R_0			8	A ∧ r	No Zero
	OFFA	A, r	▼ ▼	11011 R_2 R_1 R_0			8	A ∧ r	Zero
8-BIT ARITHMETIC (MEMORY)	ADDX	rpa	01110000	11000 A_2 A_1 A_0			11	A ← A+ (rpa)	
	ADCX	rpa		11010 A_2 A_1 A_0			11	A ← A+ (rpa)+CY	
	ADDNCX	rpa		10100 A_2 A_1 A_0			11	A ← A+ (rpa)	No Carry
	SUBX	rpa		11100 A_2 A_1 A_0			11	A ← A− (rpa)	
	SBBX	rpa		11110 A_2 A_1 A_0			11	A ← A− (rpa)−CY	
	SUBNBX	rpa		10110 A_2 A_1 A_0			11	A ← A− (rpa)	No Borrow
	ANAX	rpa		10001 A_2 A_1 A_0			11	A ← A ∧ (rpa)	
	ORAX	rpa		10011 A_2 A_1 A_0			11	A ← A ∨ (rpa)	
	XRAX	rpa		10010 A_2 A_1 A_0			11	A ← A ∨̄ (rpa)	
	GTAX	rpa		10101 A_2 A_1 A_0			11	A− (rpa)−1	No Borrow
	LTAX	rpa	▼ ▼	10111 A_2 A_1 A_0			11	A− (rpa)	Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	NEAX	rpa	01110000	11101 A_2 A_1 A_0			11	A– (rpa)	No Zero
	EQAX	rpa		11111 A_2 A_1 A_0			11	A– (rpa)	Zero
	ONAX	rpa		11001 A_2 A_1 A_0			11	A ∧ (rpa)	No Zero
	OFFAX	rpa	↓ ↓	11011 A_2 A_1 A_0			11	A ∧ (rpa)	Zero
	ADI •	A, byte	01000110	← Data →			7	A ← A+byte	
		r, byte	01110100	01000 R_2 R_1 R_0	Data		11	r ← r+byte	
		sr2, byte	01100100	S_3 1000 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	
	ACI •	A, byte	01010110	← Data →			7	A ← A+byte+CY	
		r, byte	01110100	01010 R_2 R_1 R_0	Data		11	r ← r+byte+CY	
		sr2, byte	01100100	S_3 1010 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte+CY	
	ADINC •	A, byte	00100110	← Data →			7	A ← A+byte	No Carry
		r, byte	01110100	00100 R_2 R_1 R_0	Data		11	r ← r+byte	No Carry
		sr2, byte	01100100	S_3 0100 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	No Carry
	SUI •	A, byte	01100110	← Data →			7	A ← A–byte	
		r, byte	01110100	01100 R_2 R_1 R_0	Data		11	r ← r–byte	
		sr2, byte	01100100	S_3 1100 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte	
	SBI •	A, byte	01110110	← Data →			7	A ← A–byte–CY	
		r, byte	01110100	01110 R_2 R_1 R_0	Data		11	r ← r–byte–CY	
		sr2, byte	01100100	S_3 1110 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte–CY	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	SUINB •	A, byte	00110110	← Data →			7	A ← A–byte	No Borrow
		r, byte	01110100	00110 R_2 R_1 R_0	Data		11	r ← r–byte	No Borrow
		sr2, byte	0110 ↓	S_3 0110 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte	No Borrow
	ANI •	A, byte	00000111	← Data →			7	A ← A ∧ byte	
		r, byte	01110100	00001 R_2 R_1 R_0	Data		11	r ← r ∧ byte	
		sr2, byte	01100100	S_3 0001 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∧ byte	
	ORI •	A, byte	00010111	← Data →			7	A ← A ∨ byte	
		r, byte	01110100	00011 R_2 R_1 R_0	Data		11	r ← r ∨ byte	
		sr2, byte	0110 ↓	S_3 0011 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨ byte	
	XRI •	A, byte	00010110	← Data →			7	A ← A ∨̄ byte	
		r, byte	01110100	00010 R_2 R_1 R_0	Data		11	r ← r ∨̄ byte	
		sr2, byte	0110 ↓	S_3 0010 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨̄ byte	
	GTI •	A, byte	00100111	← Data →			7	A–byte–1	No Borrow
		r, byte	01110100	00101 R_2 R_1 R_0	Data		11	r–byte–1	No Borrow
		sr5, byte	0110 ↓	S_3 0101 S_2 S_1 S_0	↓		14	sr5–byte–1	No Borrow
	LTI •	A, byte	00110111	← Data →			7	A–byte	Borrow
		r, byte	01110100	00111 R_2 R_1 R_0	Data		11	r–byte	Borrow
		sr5, byte	0110 ↓	S_3 0111 S_2 S_1 S_0	↓		14	sr5–byte	Borrow

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	NEI	*	A, byte	01100111	← Data →			7	A–byte	No Zero
			r, byte	01110100	01101 R_2 R_1 R_0	Data		11	r–byte	No Zero
			sr5, byte	0110 ↓	S_3 1101 S_2 S_1 S_0	↓		14	sr5–byte	No Zero
	EQI	*	A, byte	01110111	← Data →			7	A–byte	Zero
			r, byte	01110100	01111 R_2 R_1 R_0	Data		11	r–byte	Zero
			sr5, byte	0110 ↓	S_3 1111 S_2 S_1 S_0	↓		14	sr5–byte	Zero
	ONI	*	A, byte	01000111	← Data →			7	A ∧ byte	No Zero
			r, byte	01110100	01001 R_2 R_1 R_0	Data		11	r ∧ byte	No Zero
			sr5, byte	0110 ↓	S_3 1001 S_2 S_1 S_0	↓		14	sr5 ∧ byte	No Zero
	OFFI	*	A, byte	01010111	← Data →			7	A ∧ byte	Zero
			r, byte	01110100	01011 R_2 R_1 R_0	Data		11	r ∧ byte	Zero
			sr5, byte	0110 ↓	S_3 1011 S_2 S_1 S_0	↓		14	sr5 ∧ byte	Zero
WORKING REGISTER	ADDW		wa	01110100	11000000	Offset		14	A ← A+(V.wa)	
	ADCW		wa		1101			14	A ← A+(V.wa)+CY	
	ADDNCW		wa		1010			14	A ← A+(V.wa)	No Carry
	SUBW		wa		1110			14	A ← A–(V.wa)	
	SBBW		wa		1111			14	A ← A–(V.wa)–CY	
	SUBNBW		wa		1011 ↓			14	A ← A–(V.wa)	No Borrow
	ANAW		wa		10001000			14	A ← A ∧ (V.wa)	
	ORAW		wa	↓ ↓	1001 ↓	↓		14	A ← A ∨ (V.wa)	

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
WORKING REGISTER	XRAM		wa	01110100	10010000	Offset		14	A ← A ⊻ (V.wa)	
	GTAW		wa		10101000			14	A–(V.wa)–1	No Borrow
	LTAW		wa		1011			14	A–(V.wa)	Borrow
	NEAW		wa		1110			14	A–(V.wa)	No Zero
	EQAW		wa		1111			14	A–(V.wa)	Zero
	ONAW		wa		1100			14	A ∧ (V.wa)	No Zero
	OFFAW		wa	↓ ↓	1101 ↓	↓		14	A ∧ (V.wa)	Zero
	ANIW	*	wa, byte	00000101	← Offset →	Data		19	(V.wa) ← (V.wa) ∧ byte	
	ORIW	*	wa, byte	0001				19	(V.wa) ← (V.wa) ∨ byte	
	GTIW	*	wa, byte	0010				13	(V.wa)–byte–1	No Borrow
	LTIW	*	wa, byte	0011				13	(V.wa)–byte	Borrow
	NEIW	*	wa, byte	0110				13	(V.wa)–byte	No Zero
	EQIW	*	wa, byte	0111				13	(V.wa)–byte	Zero
	ONIW	*	wa, byte	0100				13	(V.wa) ∧ byte	No Zero
	OFFIW	*	wa, byte	0101 ↓	↓	↓		13	(V.wa) ∧ byte	Zero
16-BIT ARITHMETIC	EADD		EA, r2	01110000	01000 R_1 R_0			11	EA ← EA+r2	
	DADD		EA, rp3	0100	11000 1 P_1 P_0			11	EA ← EA+rp3	
	DADC		EA, rp3		1101			11	EA ← EA+rp3+CY	
	DADDNC		EA, rp3		1010 ↓			11	EA ← EA+rp3	No Carry
	ESUB		EA, r2	0000 ↓	011000 R_1 R_0			11	EA ← EA–r2	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
16-BIT ARITHMETIC	DSUB	EA, rp3	01110100	111001 P_1 P_0			11	EA ← EA−rp3	
	DSBB	EA, rp3		1111			11	EA ← EA−rp3−CY	
	DSUBNB	EA, rp3		1011 ↓			11	EA ← EA−rp3	No Borrow
	DAN	EA, rp3		100011 P_1 P_0			11	EA ← EA ∧ rp3	
	DOR	EA, rp3		1001 ↓			11	EA ← EA ∨ rp3	
	DXR	EA, rp3		100101 P_1 P_0			11	EA ← EA ⊻ rp3	
	DGT	EA, rp3		101011 P_1 P_0			11	EA−rp3−1	No Borrow
	DLT	EA, rp3		1011			11	EA−rp3	Borrow
	DNE	EA, rp3		1110			11	EA−rp3	No Zero
	DEQ	EA, rp3		1111			11	EA−rp3	Zero
	DON	EA, rp3		1100			11	EA ∧ rp3	No Zero
	DOFF	EA, rp3	↓ ↓	1101 ↓			11	EA ∧ rp3	Zero
MULTIP/ DIVIDE	MUL	r2	01001000	001011 R_1 R_0			32	EA ← A X r2	
	DIV	r2	↓ ↓	0011 ↓			59	EA ← EA÷r2, r2 ← surplus	
INCREMENT/ DECREMENT	INR	r2	010000 R_1 R_0				4	r2−r2+1	Carry
	INRW *	wa	00100000	← Offset →			16	(V.wa) ← (V.wa)+1	Carry
	INX	rp	00 P_1 P_0 0010				7	rp ← rp+1	
		EA	10101000				7	EA ← EA+1	
	DCR	r2	010100 R_1 R_0				4	r2 ← r2−1	Borrow
	DCRW *	wa	00110000	← Offset →			16	(V.wa) ← (V.wa)−1	Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
	DCX	rp	00 P_1 P_0 0011				7	rp ← rp−1	
		EA	10101001				7	EA ← EA−1	
BIT MANIPULATION	MOV *	CY, bit	01011111	Bit Adrs			10	CY ← (bit)	
		bit, CY	01011010				13	(bit) ← CY	
	AND *	CY, bit	00110001				10	CY ← CY ∧ (bit)	
	OR *	CY, bit	01011100				10	CY ← CY ∨ (bit)	
	XOR *	CY, bit	01011110				10	CY ← CY ⊻ (bit)	
	SETB *	bit	01011000				13	(bit) ← 1	
	CLR *	bit	01011011				13	(bit) ← 0	
	NOT *	bit	01011001				13	(bit) ← $\overline{(bit)}$	
	SK *	bit	01011101				10	Skip if (bit)=1	(bit)=1
	SKN *	bit	01010000	↓			10	Skip if (bit)=0	(bit)=0
OTHERS	DAA		01100001				4	Decimal Adjust Accumulator	
	STC		01001000	00101011			8	CY ← 1	
	CLC		↓ ↓	00101010			8	CY ← 0	
	CMC		01001000	10101010			8	CY ← $\overline{CY}$	
	NEGA		↓ ↓	00111010			8	A ← A+1	
ROTAT/ SHIFT	RLD		01001000	00111000			17	Rotate Left Digit	
	RRD		↓ ↓	↓ 1001			17	Rotate Right Digit	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
ROTATE AND SHIFT	RLL	r2	01001000	001101 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow CY$, $CY \leftarrow r2_7$	
	RLR	r2		00 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow CY$, $CY \leftarrow r2_0$	
	SLL	r2		001001 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	
	SLR	r2		00 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	
	SLLC	r2		000001 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	Carry
	SLRC	r2		00 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	Carry
	DRLL	EA		10110100			8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow CY$, $CY \leftarrow EA_{15}$	
	DRLR	EA		0000			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow CY$, $CY \leftarrow EA_0$	
	DSLL	EA		10100100			8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow 0$, $CY \leftarrow EA_{15}$	
	DSLR	EA		0000			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow 0$, $CY \leftarrow EA_0$	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
JUMP	JMP *	word	01010100	← Low Adrs →	High Adrs		10	PC ← word	
	JB		00100001				4	$PC_H \leftarrow B$, $PC_L \leftarrow C$	
	JR	word	11 ← jdispl →				10	PC ← PC+1+jdispl	
	JRE *	word	0100111 ← jdisp →				10	PC ← PC+2+jdispl	
	JEA		01001000	00101000			8	PC ← EA	
CALL	CALL *	word	01000000	← Low adrs →	High Adrs		16	$(SP-1) \leftarrow (PC+3)_H$, $(SP-2) \leftarrow (PC+3)_L$, PC ← word, SP ← SP−2	
	CALB		01001000	00101001			17	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$, $PC_H \leftarrow B$, SP ← SP−2	
	CALF *	word	01111 ← fa →				13	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$, $PC_{15-11} \leftarrow 00001$, $PC_{10-0} \leftarrow$ fa, SP ← SP−2	
	CALT	word	100 ← ta →				16	$(SP-1) \leftarrow (PC+1)_H$, $(SP-2) \leftarrow (PC+1)_L$, $PC_L \leftarrow (128+2ta)$, $PC_H \leftarrow (129+2ta)$, SP ← SP−2	
	SOFTI		01110010				16	$(SP-1) \leftarrow PSW$, $(SP-2) \leftarrow (PC+1)_H$, $(SP-3) \leftarrow (PC+1)_L$, PC ← 0060H, SP ← SP−3	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
RETURN	RET		10111000				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$ SP ← SP+2	
	RETS		1001				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$ SP ← SP+2, PC ← PC+n	
	RETI		01100010				13	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$ PSW ← (SP+2), SP ← SP+3	Unconditional Skip
SKIP	SK	f	01001000	00001 F_2 F_1 F_0			8	Skip if f=1	f=1
	SKN	f		0001			8	Skip if f=0	f=0
	SKIT	irf		010 I_4 I_3 I_2 I_1 I_0			8	Skip if irf=1, then reset irf	irf=1
	SKNIT	irf		011 I_4 I_3 I_2 I_1 I_0			8	Skip if irf=0 Reset irf, if irf=1	irf=0
CPU CONTROL	NOP		00000000				4	No Operation	
	EI		10101010				4	Enable Interrupt	
	DI		10111010				4	Disable Interrupt	
	HLT		01001000	00111011			11	Halt	

Notes:

(*1): B2(Data) : rpa2 = D+byte, H+byte
(*2): B3(Data) : rpa3 = D+byte, H+byte
(*3): right side of slash (/) in states indicates case rpa2, rpa3 = D+byte, H+A, H+B, H+EA, H+byte
(*4): in the case of skip condition, the idle states are as follows.

1-byte instruction : 4 states
2-byte instruction : 8 states
3-byte instruction : 11 states
2-byte instruction (with *) : 7 states
3-byte instruction (with *) : 10 states
4-byte instruction : 14 states

ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Threshold Voltage	V_{TH}		−0.5 to V_{CC} + 0.1	V
Operating Temperature	T_{opt}	10 MHz < f_{XTAL} ≤ 12 MHz	−10 to +70	°C
		f_{XTAL} ≤ 10 MHz	−40 to +85	°C
Storage Temperature	T_{stg}		−65 to + 150	°C

OPERATING CONDITION

OSC. FREQ. / PARAMETER	T_a	V_{CC}, AV_{CC}
10 MHz < f_{XTAL} ≤ 12 MHz *1	−10°C to +70°C	+5.0V ± 5 %
f_{XTAL} ≤ 10 MHz *1	−40°C to +85°C	+5.0V ± 10 %

CAPACITANCE

T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_c = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2*2	0.5	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.2	mA
V_{CC} Supply Current	I_{CC}			150*2	200	mA

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE ↓	t_{AL}	*3, *5	65		ns
Address Hold from ALE ↓	t_{LA}	*3, *5	50		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*3, *5	150		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*3, *5		360	ns
ALE ↓ to Data Input	t_{LDR}	*3, *5		215	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*3, *5		180	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*3, *5	35		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*3, *5	115		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *3, *5	280		ns
		OP Code Fetch *3, *5	530		ns
ALE Width High	t_{LL}	*3, *5	125		ns
$\overline{M1}$ Setup Time to $\overline{ALE}$ ↓	t_{ML}	*3	65		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*3	50		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*3	65		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*3	50		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*3, *5	150		ns
ALE ↓ to Data Output	t_{LDW}	*3, *5		195	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*3, *5	35		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*3, *5	230		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*3, *5	95		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*3, *5	115		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *5	280		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1		μs
			*7	500		ns
		$\overline{SCK}$ Output		2		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	420		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	420		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

EXTENDED TEMPERATURE

DC CHARACTERISTICS

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3); 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤ V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2*2	0.6	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.5	mA
V_{CC} Supply Current	I_{CC}			150*2	220	mA

AC CHARACTERISTICS READ/WRITE OPERATION

EXTENDED TEMPERATURE

(T_a = −40°C to + 85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		100	250	ns
Address Setup to ALE ↓	t_{AL}	*4, *5	100		ns
Address Hold from ALE ↓	t_{LA}	*4, *5	70		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*4, *5	200		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*4, *5		480	ns
ALE ↓ to Data Input	t_{LDR}	*4, *5		300	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*4, *5		250	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*4, *5	50		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*4, *5	150		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *4, *5	350		ns
		OP Code Fetch *4, *5	650		ns
ALE Width High	t_{LL}	*4, *5	160		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*4	100		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*4	70		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*4	100		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*4	70		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*4, *5	200		ns
ALE ↓ to Data Output	t_{LDW}	*4, *5		210	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*4, *5	50		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*4, *5	300		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*4, *5	130		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*4, *5	150		ns
$\overline{WR}$ Width Low	t_{WW}	*4, *5	350		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1.2		μs
			*7	500		ns
		$\overline{SCK}$ Output		2.4		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	505		ns
			*7	200		ns
		$\overline{SCK}$ Output		1.1		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	505		ns
			*7	200		ns
		$\overline{SCK}$ Output		1.1		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

HOLD OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

(T_a = −40°C to + 85°C V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
HOLD ↑ Setup Time to ALE ↑	t_{SHDL}		2T + 150			ns
ALE ↑ to HLDA ↑ Delay	t_{DLHA}				T + 150	ns
HLDA ↑ to BUS Floating	t_{FBHA}		0			ns
HOLD ↓ to HLDA ↓ Delay	t_{HDDA}		T −50		4T + 150	ns
HLDA ↓ to Bus Enable Time	t_{EHAB}		0			ns
Bus Setup Time to ALE	t_{BL}		2T −100			ns

3

COMPARATOR CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Comparison Accuracy	V_{ACOMP}				± 100	mV
Threshold Voltage	V_{TH}		0		V_{CC}+0.1	V
Comparison Time	t_{COMP}		144		145	T_{CYC}
PT Input Voltage	V_{IPT}		0		V_{CC}	V

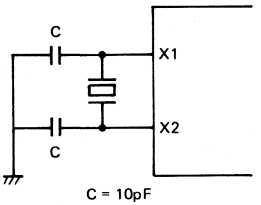
ZERO-CROSS CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = −40°C to + 85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

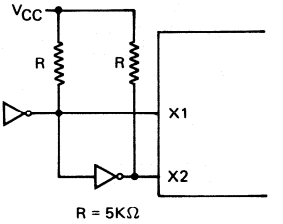
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

*1: XTAL oscillation circuit



C = 10pF

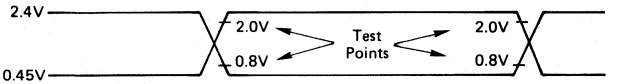
*8: External clock drive circuit



R = 5KΩ

*2: T_a = +25°C, V_{CC} = V_{DD} = 5V
*3: f_{XTAL} = 12 MHz
*4: f_{XTAL} = 10 MHz
*5: Load Capacitance: C_L = 150 pF
*6: Asynchronous mode with 1x baud rate, synchronous, I/O interface mode
*7: Asynchronous mode with 16x or 64x baud rate

AC TIMING TEST POINTS



EXTERNAL CLOCK

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = −40°C to + 85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
High Level Width	$t_{\phi H}$		30	250	ns
Low Level Width	$t_{\phi L}$		30	250	ns
Rising Time	t_r		0	30	ns
Falling Time	t_f		0	30	ns

DATA RETENTION CHARACTERISTICS

(T_a = −10 to +70°C, V_{CC} = 0V, V_{DD} = V_{DDDR})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{DDDR}	RESET = V_{IL}	3.2		5.5	V
Data Retention Supply Current	I_{DDDR}	RESET = V_{IL}, V_{DDDR} = 3.2 V		1.3	3.0	mA

BUS TIMING DEPENDING ON tCYC

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220 *1	MAX	ns
t_{LDR}	5T − 200 *1	MAX	ns
t_{RD}	4T − 150 *1	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read) *1	MIN	ns
	7T − 50 (OP Code Fetch) *1		
t_{LL}	2T − 40	MIN	ns
t_{ML}	2T − 100	MIN	ns
t_{LM}	T − 30	MIN	ns
t_{IL}	2T − 100	MIN	ns
t_{LI}	T − 30	MIN	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100 *1	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50 *1	MIN	ns
t_{CYK}	12T ($\overline{SCK}$ Input) *2	MIN	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	5T + 5 (SCK Input) *2	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		
t_{KKH}	5T + 5 (SCK Input) *2	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		

*1: Add 3T to each parameter in the case of external memory access using program WAIT function.

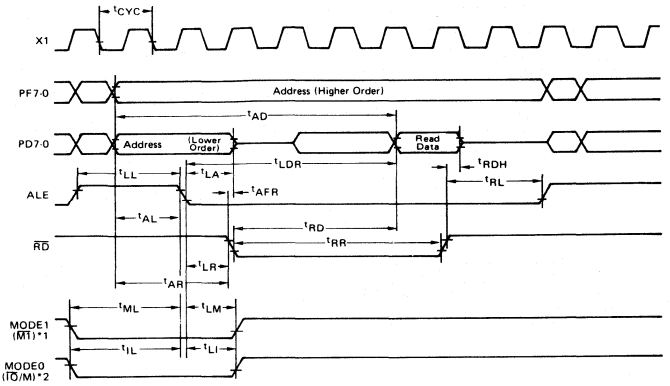
*2: Asynchronous mode with 1x baud rate, Synchronous, I/O Interface Mode

*3: T = t_{CYC} = 1/f_{XTAL}

*4: **The items not listed in this table are not dependent on f_{XTAL}.**

3

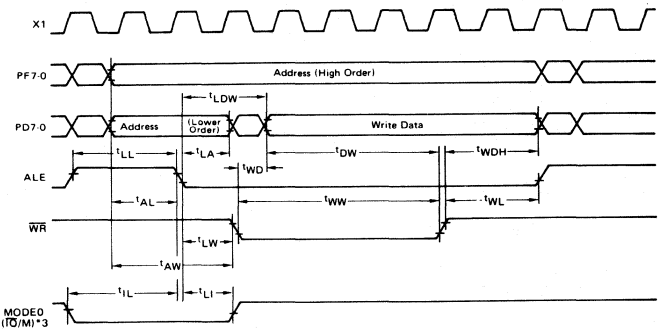
READ OPERATION



*1: $\overline{M1}$ signal is output to the MODE1 pin at 1st OP code fetch cycle when MODE 1 pin is pulled-up to V_{CC}.

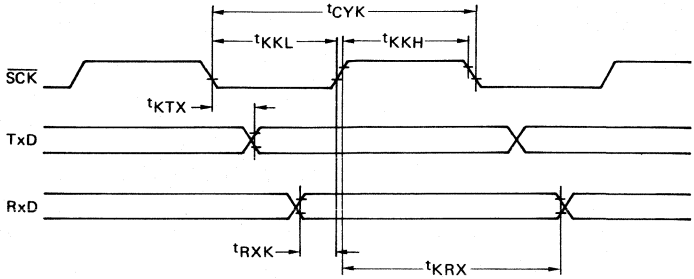
*2: $\overline{IO}$/M signal is output to the MODE0 pin at sr to sr2 register read timing when MODE0 pin is pulled-up to V_{CC}.

WRITE OPERATION

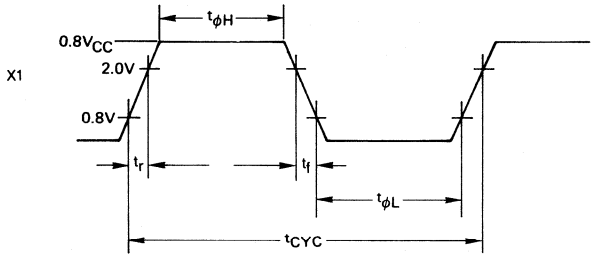


*3: $\overline{IO}$/M signal is output to the MODE0 pin at sr to sr2 register write timing when MODE0 pin is pulled-up to V_{CC}.

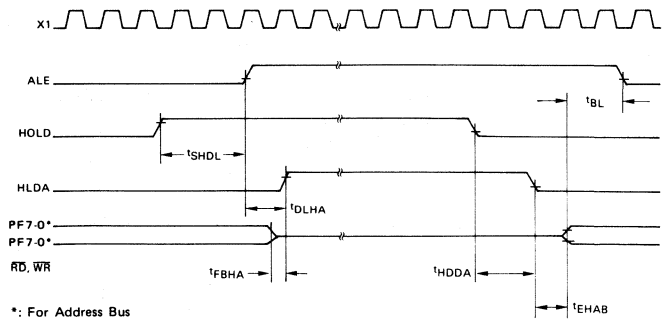
SERIAL OPERATION



X1 INPUT WAVEFORM



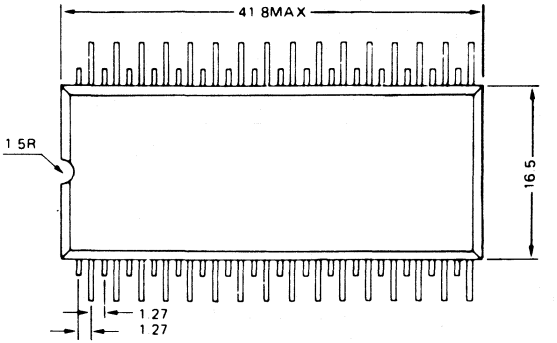
HOLD OPERATION

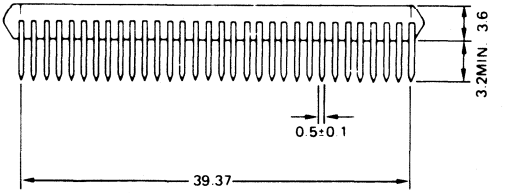


*: For Address Bus

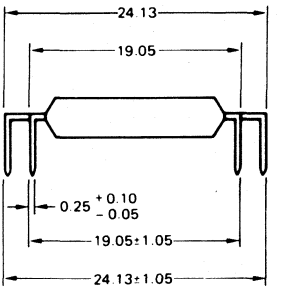
3

64 PIN PLASTIC
QUIP OUTLINE BENT LEADS
(Unit : mm)
μPD7807G/μPD7808G

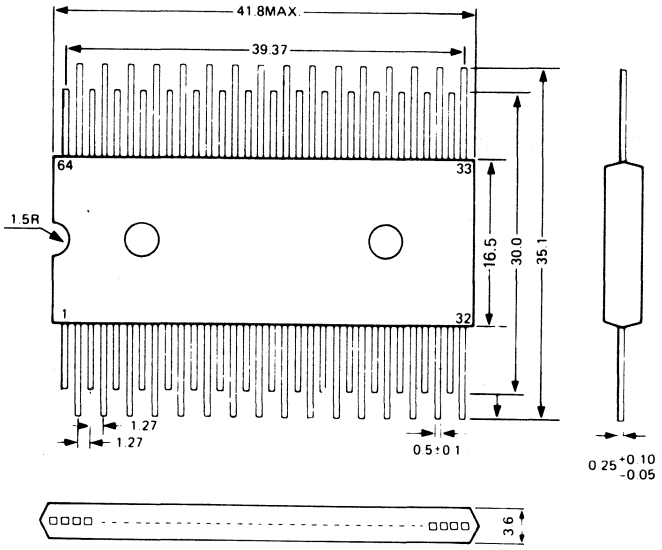




When ordering this package, specify as follows:
μPD7807G-36
μPD7808G-xxx-36



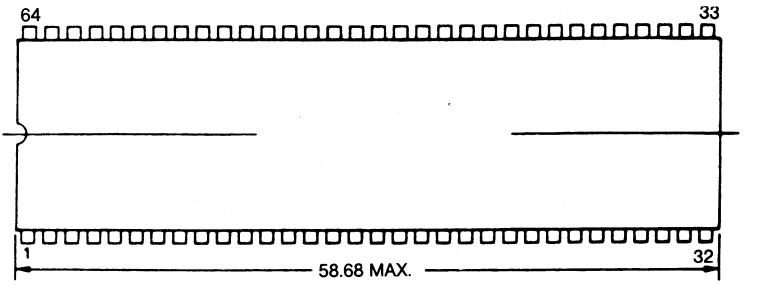
64 PIN PLASTIC QUIP
PACKAGE OUTLINE
STRAIGHT LEADS
(Unit : mm)
μPD7808



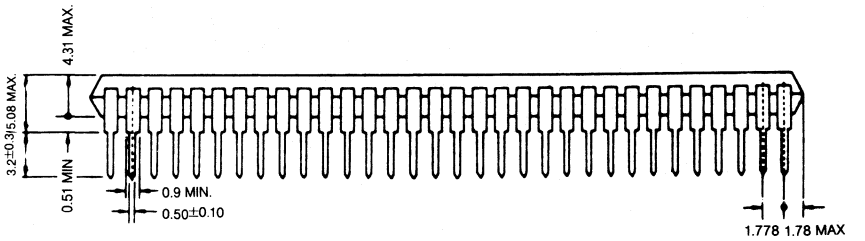
When ordering this package, specify as follows μPD7808G-xxx-37

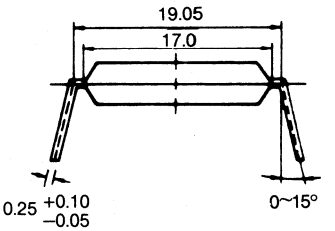
PACKAGE OUTLINE
μPD7807CW
μPD7808CW

64-PIN SHRINK DIP



When ordering this package, specify as follows:
μPD7807CW
μPD7808CW-xxx





ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Threshold Voltage	V_{TH}		−0.5 to V_{CC} + 0.1	V
Operating Temperature	T_{opt}	10 MHz < f_{XTAL} ≤ 12 MHz	−10 to +70	°C
		f_{XTAL} ≤ 10 MHz	−40 to + 85	°C
Storage Temperature	T_{stg}		−40 to + 125	°C

OPERATING CONDITION

OSC. FREQ. \ PARAMETER	T_a	V_{CC}, AV_{CC}
10 MHz < f_{XTAL} ≤ 12 MHz *1	−10°C to +70°C	+5.0V ± 5 %
f_{XTAL} ≤ 10 MHz *1	−40°C to +85°C	+5.0V ± 10 %

CAPACITANCE

(T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_c = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2*2	0.5	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.2	mA
V_{CC} Supply Current	I_{CC}			150*2	200	mA

3

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE ↓	t_{AL}	*3, *5	65		ns
Address Hold from ALE ↓	t_{LA}	*3, *5	50		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*3, *5	150		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*3, *5		360	ns
ALE ↓ to Data Input	t_{LDR}	*3, *5		215	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*3, *5		180	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*3, *5	35		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*3, *5	115		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *3, *5	280		ns
		OP Code Fetch *3, *5	530		ns
ALE Width High	t_{LL}	*3, *5	125		ns
$\overline{M1}$ Setup Time to $\overline{ALE}$ ↓	t_{ML}	*3	65		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*3	50		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*3	65		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*3	50		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*3, *5	150		ns
ALE ↓ to Data Output	t_{LDW}	*3, *5		195	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*3, *5	35		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*3, *5	230		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*3, *5	95		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*3, *5	115		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *5	280		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1		μs
			*7	500		ns
		$\overline{SCK}$ Output		2		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	400		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	400		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

EXTENDED TEMPERATURE

DC CHARACTERISTICS

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3); 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤ V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2	0.6	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.5	mA
V_{CC} Supply Current	I_{CC}			150*2	220	mA

AC CHARACTERISTICS READ/WRITE OPERATION

EXTENDED TEMPERATURE

(T_a = −40°C to + 85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		100	250	ns
Address Setup to ALE ↓	t_{AL}	*4, *5	100		ns
Address Hold from ALE ↓	t_{LA}	*4, *5	70		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*4, *5	200		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*4, *5		480	ns
ALE ↓ to Data Input	t_{LDR}	*4, *5		300	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*4, *5		250	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*4, *5	50		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*4, *5	150		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *4, *5	350		ns
		OP Code Fetch *4, *5	650		ns
ALE Width High	t_{LL}	*4, *5	160		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*4	100		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*4	70		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*4	100		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*4	70		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*4, *5	200		ns
ALE ↓ to Data Output	t_{LDW}	*4, *5		210	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*4, *5	50		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*4, *5	300		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*4, *5	130		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*4, *5	150		ns
$\overline{WR}$ Width Low	t_{WW}	*4, *5	350		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1.2		μs
			*7	500		ns
		$\overline{SCK}$ Output		2.4		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	500		ns
			*7	200		ns
		$\overline{SCK}$ Output		1.1		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	500		ns
			*7	200		ns
		$\overline{SCK}$ Output		1.1		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

HOLD OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
HOLD ↑ Setup Time to ALE ↑	t_{SHDL}		2T + 150			ns
ALE ↑ to HLDA ↑ Delay	t_{DLHA}				T + 150	ns
HLDA ↑ to BUS Floating	t_{FBHA}		0			ns
HOLD ↓ to HLDA ↓ Delay	t_{HDDA}		T −50		4T + 150	ns
HLDA ↓ to Bus Enable Time	t_{EHAB}		0			ns
Bus Setup Time to ALE	t_{BL}		2T −100			ns

3

COMPARATOR CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Comparison Accuracy	V_{ACOMP}				± 100	mV
Threshold Voltage	V_{TH}		0		V_{CC}+0.1	V
Comparison Time	t_{COMP}		144		145	T_{CYC}
PT Input Voltage	V_{IPT}		0		V_{CC}	V

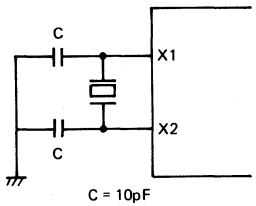
ZERO-CROSS CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

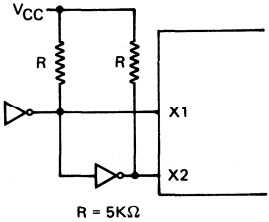
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

*1: XTAL oscillation circuit



C = 10pF

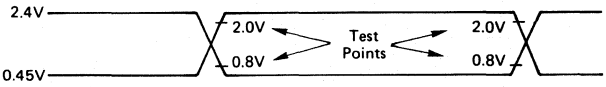
*8: External clock drive circuit



R = 5KΩ

*2: T_a = +25°C, V_{CC} = V_{DD} = 5V
*3: f_{XTAL} = 12 MHz
*4: f_{XTAL} = 10 MHz
*5: Load Capacitance: C_L = 150 pF
*6: Asynchronous mode with 1x baud rate, synchronous, I/O interface mode
*7: Asynchronous mode with 16x or 64x baud rate

AC TIMING TEST POINTS



EXTERNAL CLOCK

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
High Level Width	$t_{\phi H}$		30	250	ns
Low Level Width	$t_{\phi L}$		30	250	ns
Rising Time	t_r		0	30	ns
Falling Time	t_f		0	30	ns

DATA RETENTION CHARACTERISTICS

(T_a = −10 to +70°C, V_{CC} = 0V, V_{DD} = V_{DDDR})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{DDDR}	RESET = V_{IL}	3.2		5.5	V
Data Retention Supply Current	I_{DDDR}	RESET = V_{IL}, V_{DDDR} = 3.2 V		1.3	3.0	mA

BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220 *1	MAX	ns
t_{LDR}	5T − 200 *1	MAX	ns
t_{RD}	4T − 150 *1	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read) *1 7T − 50 (OP Code Fetch) *1	MIN	ns
t_{LL}	2T − 40	MIN	ns
t_{ML}	2T − 100	MIN	ns
t_{LM}	T − 30	MIN	ns
t_{IL}	2T − 100	MIN	ns
t_{LI}	T − 30	MIN	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100 *1	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50 *1	MIN	ns
t_{CYK}	12T ($\overline{SCK}$ Input) *2 24T ($\overline{SCK}$ Output)	MIN	ns
t_{KKL}	5T + 5 ($\overline{SCK}$ Input) *2 12T − 100 ($\overline{SCK}$ Output)	MIN	ns
t_{KKH}	5T + 5 ($\overline{SCK}$ Input) *2 12T − 100 ($\overline{SCK}$ Output)	MIN	ns

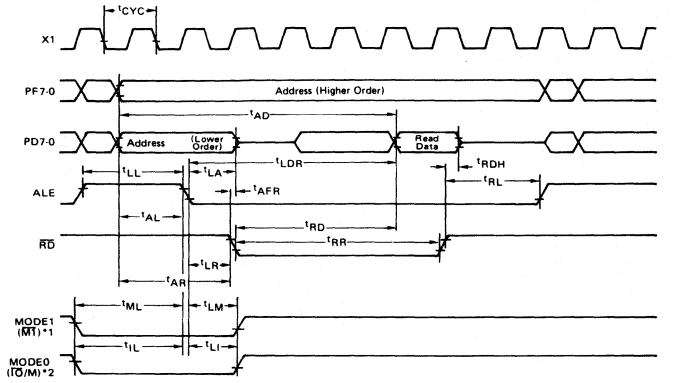
*1: Add 3T to each parameter in the case of external memory access using program WAIT function.

*2: Asynchronous mode with 1x baud rate, Synchronous, I/O Interface Mode

*3: T = t_{CYC} = 1/f_{XTAL}

*4: **The items not listed in this table are not dependent on f_{XTAL}.**

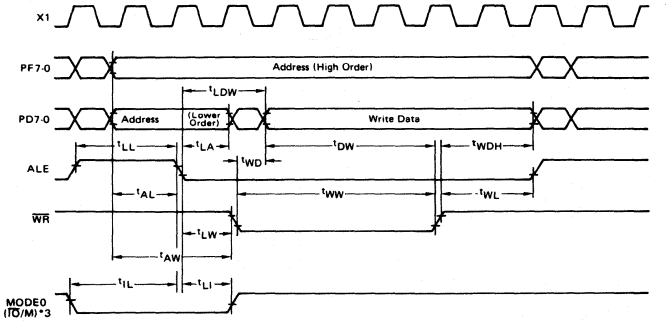
READ OPERATION



*1: $\overline{M1}$ signal is output to the MODE1 pin at 1st OP code fetch cycle when MODE 1 pin is pulled-up to V_{CC}.

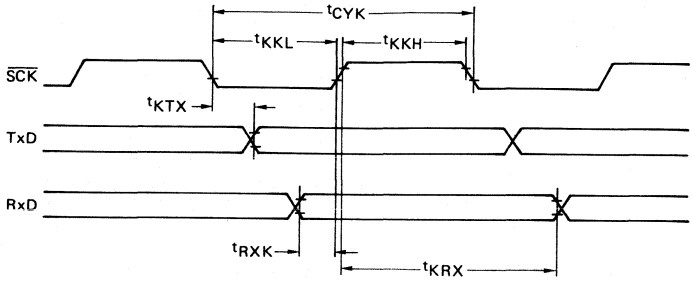
*2: $\overline{IO}/M$ signal is output to the MODE0 pin at sr to sr2 register read timing when MODE0 pin is pulled-up to V_{CC}.

WRITE OPERATION

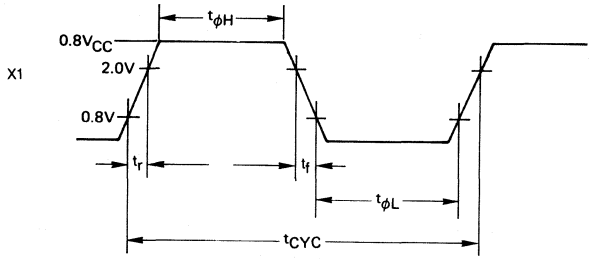


*3: $\overline{IO}/M$ signal is output to the MODE0 pin at sr to sr2 register write timing when MODE0 pin is pulled-up to V_{CC}.

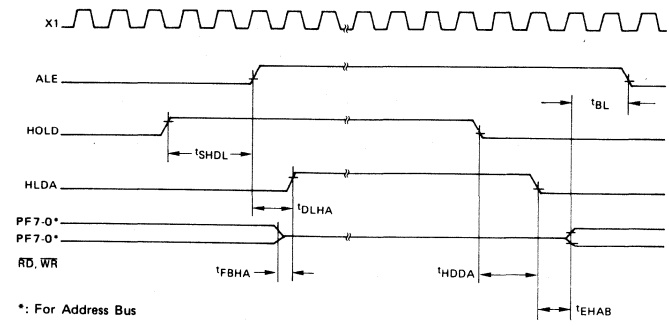
SERIAL OPERATION



X1 INPUT WAVEFORM

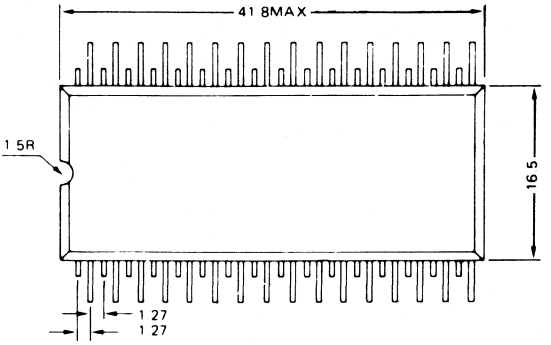


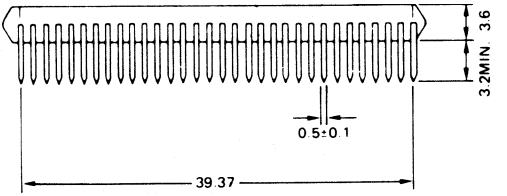
HOLD OPERATION



3

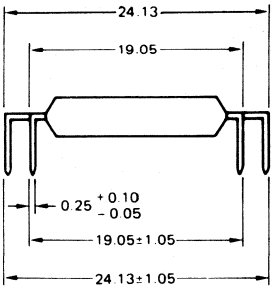
64 PIN PLASTIC
QUIP OUTLINE BENT LEADS
(Unit : mm)
μPD7809G



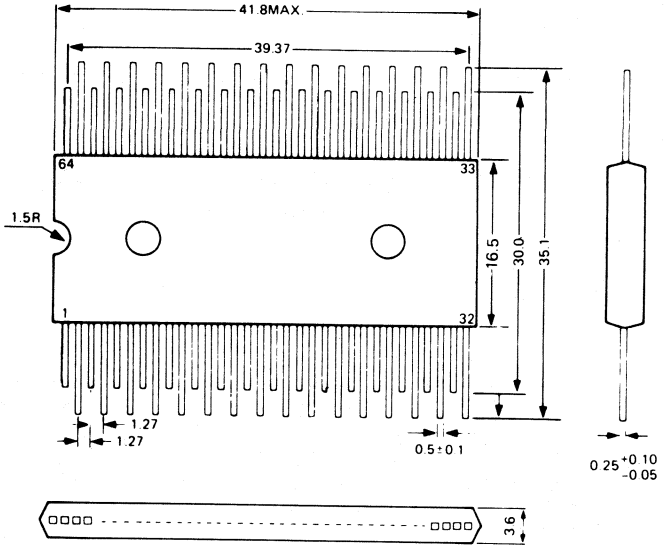


When ordering this package, specify as follows:

μPD7809G-xxx-36



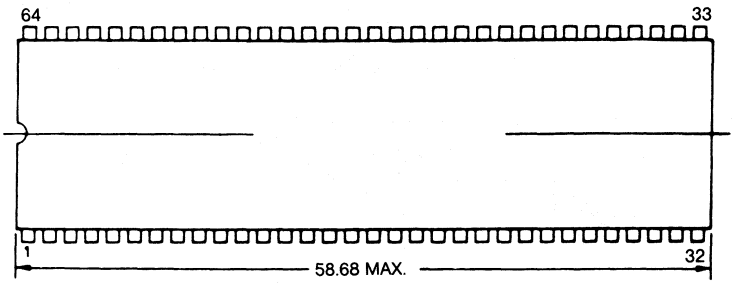
64 PIN PLASTIC
PACKAGE OUTLINE
STRAIGHT LEADS
(Unit : mm)
μPD7809



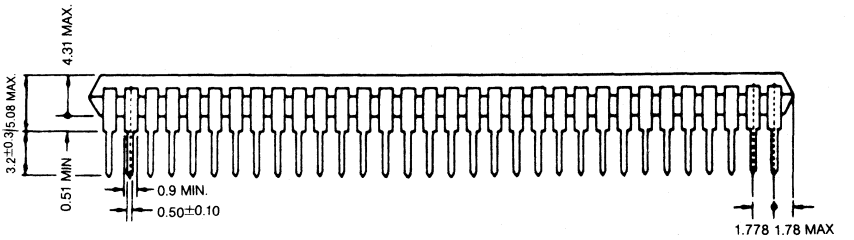
When ordering this package, specify as follows: μPD7809G-xxx-37

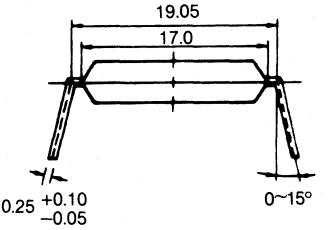
PACKAGE OUTLINE
μPD7809CW

64-PIN SHRINK DIP



When ordering this package, specify as follows:
μPD7807CW
μPD7808CW-xxx





ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Threshold Voltage	V_{TH}		−0.5 to V_{CC} + 0.1	V
Operating Temperature	T_{opt}	4 MHz < f_{XTAL} ≤ 12 MHz	−10 to +50	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OPERATING CONDITION

OSC. FREQ. \ PARAMETER	T_a	V_{CC}, AV_{CC}
4 MHz ≤ f_{XTAL} ≤ 12 MHz	−10°C to +70°C	+5.0V ± 5 %

CAPACITANCE

T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_C = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤ V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2*2	0.5	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.2	mA
V_{CC} Supply Current	I_{CC}			240*2	320	mA

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE ↓	t_{AL}	*3, *5	65		ns
Address Hold from ALE ↓	t_{LA}	*3, *5	50		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*3, *5	150		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*3, *5		360	ns
ALE ↓ to Data Input	t_{LDR}	*3, *5		215	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*3, *5		180	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*3, *5	35		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*3, *5	115		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *3, *5	280		ns
		OP Code Fetch *3, *5	530		ns
ALE Width High	t_{LL}	*3, *5	125		ns
$\overline{M1}$ Setup Time to $\overline{ALE}$ ↓	t_{ML}	*3	65		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*3	50		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*3	65		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*3	50		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*3, *5	150		ns
ALE ↓ to Data Output	t_{LDW}	*3, *5		195	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*3, *5	35		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*3, *5	230		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*3, *5	95		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*3, *5	115		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *5	280		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1.66		μs
			*7	500		ns
		$\overline{SCK}$ Output		2		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	750		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	750		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

HOLD OPERATION

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
HOLD ↑ Setup Time to ALE ↑	t_{SHDL}		2T + 150			ns
ALE ↑ to HLDA ↑ Delay	t_{DLHA}				T + 150	ns
HLDA ↑ to BUS Floating	t_{FBHA}		0			ns
HOLD ↓ to HLDA ↓ Delay	t_{HDDA}		T −50		4T + 150	ns
HLDA ↓ to Bus Enable Time	t_{EHAB}		0			ns
Bus Setup Time to ALE	t_{BL}		2T −100			ns

COMPARATOR CHARACTERISTICS

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

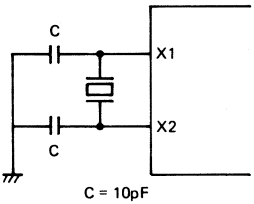
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Comparison Accuracy	V_{ACOMP}				± 100	mV
Threshold Voltage	V_{TH}		0		V_{CC}+0.1	V
Comparison Time	t_{COMP}		144		145	T_{CYC}
PT Input Voltage	V_{IPT}		0		V_{CC}	V

ZERO-CROSS CHARACTERISTICS

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

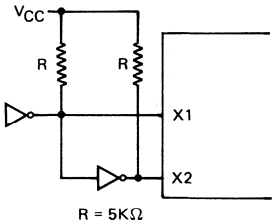
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

*1: XTAL oscillation circuit



C = 10pF

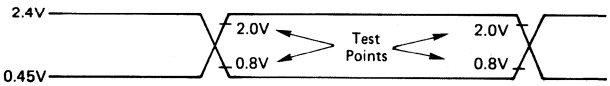
*8: External clock drive circuit



R = 5KΩ

*2: T_a = +25°C, V_{CC} = V_{DD} = 5V
*3: f_{XTAL} = 12 MHz
*4: f_{XTAL} = 10 MHz
*5: Load Capacitance: C_L = 150 pF
*6: Asynchronous mode with 1x baud rate, synchronous, I/O interface mode
*7: Asynchronous mode with 16x or 64x baud rate

AC TIMING TEST POINTS



EXTERNAL CLOCK

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
High Level Width	$t_{\phi H}$		30	250	ns
Low Level Width	$t_{\phi L}$		30	250	ns
Rising Time	t_r		0	30	ns
Falling Time	t_f		0	30	ns

DATA RETENTION CHARACTERISTICS

(T_a = −10 to +50°C, V_{CC} = 0V, V_{DD} = V_{DDDR})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{DDDR}	RESET = V_{IL}	3.2		5.5	V
Data Retention Supply Current	I_{DDDR}	RESET = V_{IL}, V_{DDDR} = 3.2 V		1.3	3.0	mA

BUS TIMING DEPENDING ON tCYC

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220 *1	MAX	ns
t_{LDR}	5T − 200 *1	MAX	ns
t_{RD}	4T − 150 *1	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read) *1	MIN	ns
	7T − 50 (OP Code Fetch) *1		
t_{LL}	2T − 40	MIN	ns
t_{ML}	2T − 100	MIN	ns
t_{LM}	T − 30	MIN	ns
t_{IL}	2T − 100	MIN	ns
t_{LI}	T − 30	MIN	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100 *1	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50 *1	MIN	ns
t_{CYK}	20T ($\overline{SCK}$ Input) *2	MIN	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	10T − 80 ($\overline{SCK}$ Input) *2	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		
t_{KKH}	10T − 80 ($\overline{SCK}$ Input) *2	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		

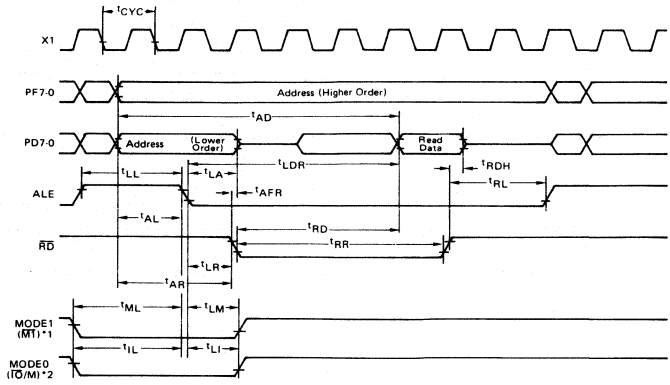
*1: Add 3T to each parameter in the case of external memory access using program WAIT function.

*2: Asynchronous mode with 1x baud rate, Synchronous, I/O Interface Mode

*3: T = t_{CYC} = 1/f_{XTAL}

*4: **The items not listed in this table are not dependent on f_{XTAL}.**

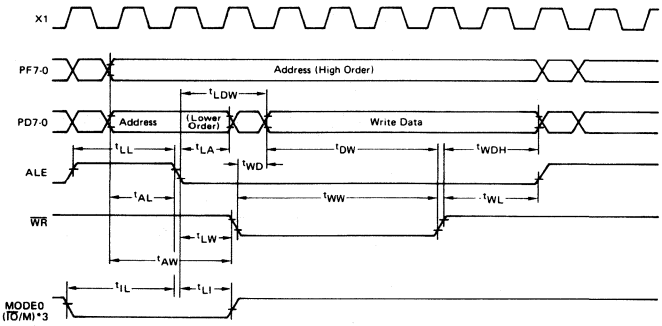
READ OPERATION



*1: $\overline{M1}$ signal is output to the MODE1 pin at 1st OP code fetch cycle when MODE 1 pin is pulled-up to V_{CC}.

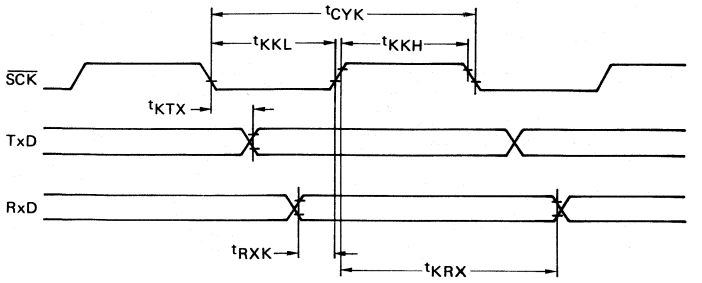
*2: $\overline{IO}/M$ signal is output to the MODE0 pin at sr to sr2 register read timing when MODE0 pin is pulled-up to V_{CC}.

WRITE OPERATION

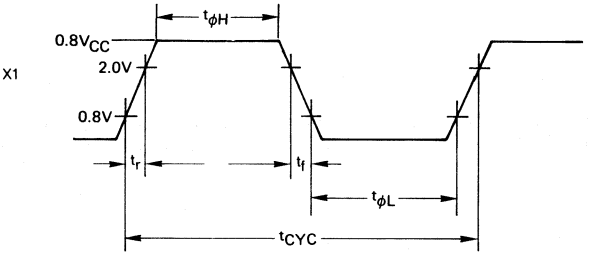


*3: $\overline{IO}/M$ signal is output to the MODE0 pin at sr to sr2 register write timing when MODE0 pin is pulled-up to V_{CC}.

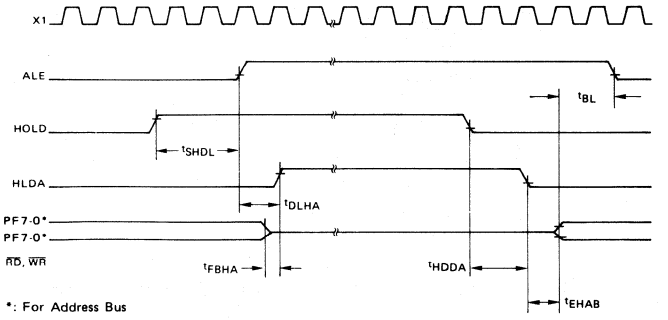
SERIAL OPERATION



X1 INPUT WAVEFORM



HOLD OPERATION



*: For Address Bus

DC PROGRAMMING CHARACTERISTICS

(T_a = +25°C ± 5°C, V_{CC} = +5V ± 10 %, V_{PP} = +21V ± 0.5V, V_{SS} = 0V, V_{CC} −0.8 ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current All except INT1, TI(PC3)	I_{LI}	0V ≤ V_{IN} < V_{CC}			± 10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −200μA	2.4			V
V_{CC} Supply Current	I_{CC}			200	300	mA
Input Low Level (All Inputs)	V_{IL}		0		0.8	V
Input High Level	V_{IH1}	All except $\overline{SCK}$, RESET and X1	2.0		V_{CC}	V
	V_{IH2}	SCK, X1	0.8 V_{CC}		V_{CC}	V
V_{PP} Supply Current	I_{PP}	$\overline{PGM}$ = V_{IL}			30	mA

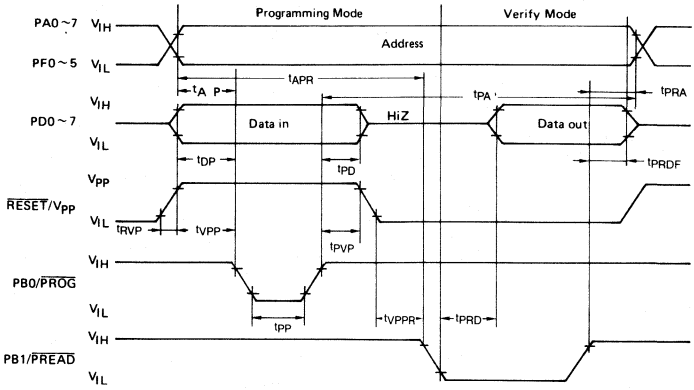
AC PROGRAMMING CHARACTERISTICS

(T_a = +25°C ± 5°C, V_{CC} = +5V ± 10 %, V_{PP} = +21V ± 0.5V, V_{SS} = 0V, V_{CC} −0.8 ≤ V_{DD} ≤ V_{CC})

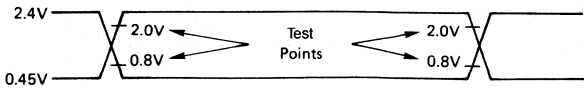
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Address Setup Time	Programming Mode	t_{AP}		2			μs
	Verify Mode	t_{APR}		2			μs
V_{PP} Setup Time		t_{VPP}		2			μs
Data Setup Time		t_{DP}		2			μs
Address Hold Time	Programming Mode	t_{PA}		2			μs
	Verify Mode	t_{PRA}		0			μs
V_{PP} Hold Time		t_{PVP}		2			μs
Data Hold Time		t_{PD}		2			μs
$\overline{READ}$ to Output Float Delay		t_{PRDR}		0		130	ns
Data Valid from $\overline{READ}$		t_{PRD}				1	μs
$\overline{PROG}$ Pulse Width During Programming		t_{PP}		45	50	55	ms
V_{PP} Pulse Rise Time During Programming		t_{RVP}		50			ns
V_{PP} Recovery Time		t_{VPPR}		2			μs
Input Rise/Fall Time		t_{IR}, t_{IF}				20	ns

TIMING WAVEFORM

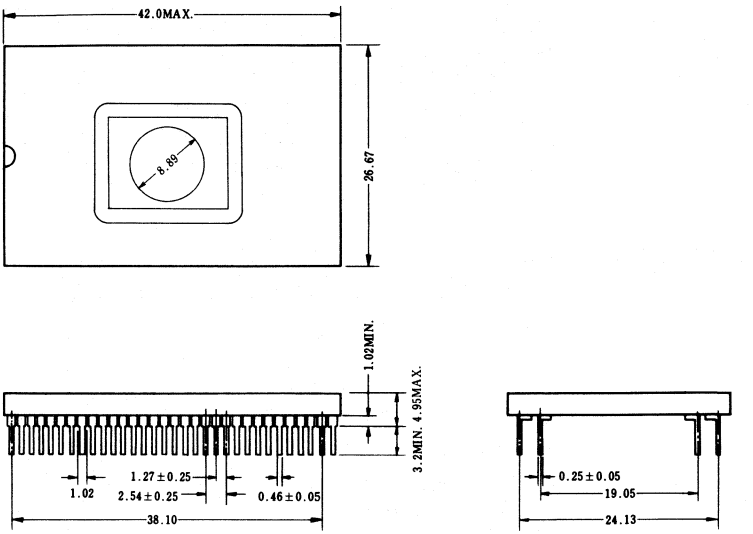
PROGRAMMING



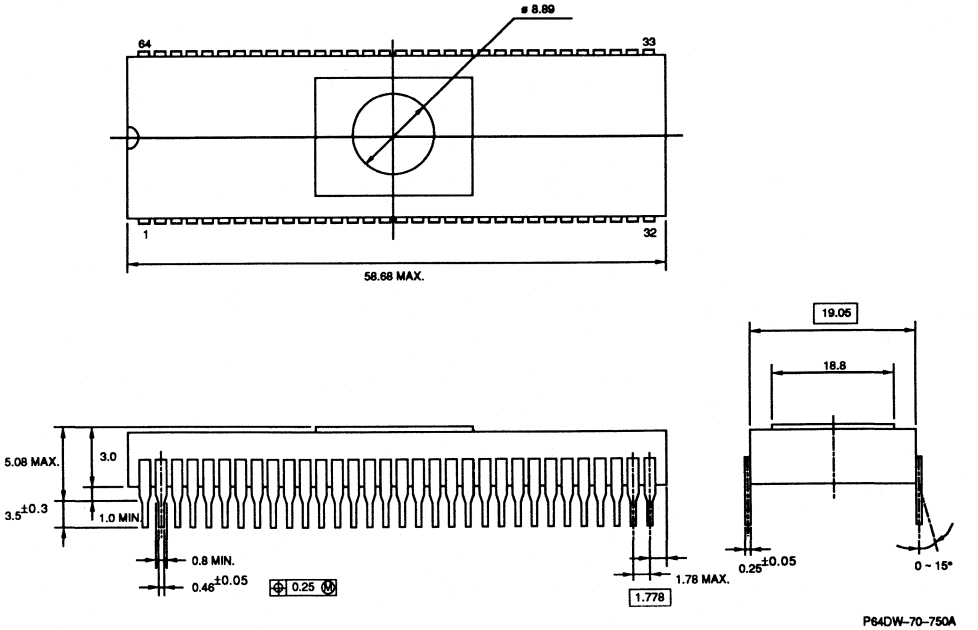
AC TIMING MEASUREMENT POINTS



64 PIN CERAMIC QUIP OUTLINE (Unit : mm)
μPD78P09R



64-PIN SHRINK DIP WITH CERAMIC WINDOW (750 mil) (Unit: mm)



SINGLE CHIP 8-BIT MICROCOMPUTER WITH ON CHIP A/D CONVERTER

DESCRIPTION

The NEC μPD7810/7811 is a high-performance single-chip microcomputer integrating sophisticated on-chip peripheral functionality normally provided by external components. The devices's internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make the μPD7810/7811 appropriate in data processing as well as control applications. The device integrates a 16-bit ALU, 4K-ROM, 256-byte RAM with an 8-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a USART and two zero-cross detect inputs on a single die, to direct the device into fast, high-end processing applications involving analog signal interface and processing.

The μPD7811 is the mask-ROM high volume production device embedded with customer program. The μPD7810 is a ROM-less version for prototyping and small volume production. The μPD78PG11E is a piggy-back EPROM version for design development.
The μPD7810H/11H is a high speed version of the μPD7810/11 (15 MHz operation)

FEATURES

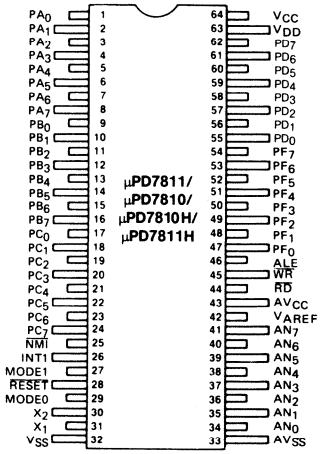
- Powerful Instruction Set Including 16-bit Multiply and Divide, 158 instructions
- High-Speed 1μsec Cycle Time-12 MHz Operation (0.85 μsec for 7810H/11H, 15 MHz)
- On-Chip 4K-Byte ROM (7811), 256-Byte RAM
- 44 I/O Lines
- Easily Expandable Memory up to 60K Bytes (externally)
- On-Chip 8-Bit A/D Converter-8 Input Channels
- Multi-Functional 16-Bit Timer/Counter
- Two Programmable 8-Bit Timers
- Full-Duplex Serial Communication Interface, synchronous and asynchronous
- Zero-Cross Detection Capability
- Vectored Interrupts, 3 external/8 internal
- Low Power Standby Operation
- 8085A Bus Compatible
- Single Power Supply +5V, N-MOS Technology
- Available in 64 Pin Package
- Standby function
- On-chip clock generator
- 64K-Byte total memory address range

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	ROM
μPD7810CW	64-PIN SDIP	ROM-Less
μPD7810G-36	64-PIN QUIP (Bent leads)	
μPD7810HCW	64-PIN SDIP	ROM-Less
μPD7810HG-36	64-PIN QUIP (Bent leads)	
μPD7811G-XXX-36	64-PIN QUIP (Bent leads)	4K-MASK ROM
μPD7811HCW	64-PIN SDIP	4K-MASK ROM
μPD7811HG-XXX-36	64-PIN QUIP (Bent leads)	
μPD7811HG-XXX-37	64-PIN QUIP (Straight)	
μPD7811G-XXX-37	64-PIN QUIP (Straight)	
μPD78PG11E	64-PIN CERAMIC QUIP (Bent leads)	PIGGY BACK
μPD7810G(A)	64-PIN QUIP	ROM-Less
μPD7811G(A)	64-PIN QUIP	4K-MASK ROM

NOTE: QUIP = QUAD IN LINE, SDIP = SHRINKED DUAL IN LINE,
FLAT = FLAT PACKAGE (SMD), (A) = AUTOMOTIVE GRADE (–40 to +85°C)

PIN CONFIGURATION



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION	
1–8	PA_0–PA_7	Port A: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port A in input mode.	
9–16	PB_0–PB_7	Port B: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port B in input mode.	
17	PC_0	Port C: (Three-state input/output) 8-bit programmable I/O port. Each line independently pro-programmable as an input or output. Alternatively, Port C may be used as control lines for USART and timer, event-counter and external interrupts. Reset puts Port C in Port mode and all lines in input mode.	Transmit Data (TxD): Serial data output terminal.
18	PC_1		Receive Data (RxD): Serial data input terminal.
19	PC_2		Serial Clock ($\overline{SCK}$): Serial clock input/output terminal. When internal clock is used, the output can be selected; when an external clock is used, the input can be selected.
20	PC_3		Timer Input ((TI)/interrupt request input (INT2): Timer clock input terminal; can also be used as falling edge, maskable-interrupt input terminal and AC input zero-cross detection terminal.
21	PC_4		Timer Output (TO): This output signal is a square wave whose frequency is determined by the timer/counter.
22	PC_5		Counter Input (CI): External pulse input terminal to the timer/event counter.
23–24	PC_6, PC_7		Counter Outputs 0, 1 (CO_0–CO_1): Programmable rectangular wave output terminal based on timer/event counter.
25	$\overline{NMI}$	Falling-edge, nonmaskable interrupt ($\overline{NMI}$) input.	
26	INT1	This signal is a rising-edge, maskable interrupt input. This input is also used to make the zero-cross detection AC input.	
27	MODE1	Used as input in conjunction with MODE0 to select appropriate memory expansion mode. Also outputs M1 Signal during each opcode fetch.	
28	$\overline{RESET}$	(Input, active low). $\overline{RESET}$ initializes the μPD7811.	
29	MODE0	Used as input in conjunction with MODE1 to select appropriate memory expansion mode. Also used to output $\overline{IO}$/M.	
30–31	X_2, X_1 (crystal)	This is a crystal connection terminal for system clock oscillation. When an external clock is supplied X_1 is the input.	
32	V_{SS}	Power supply ground potential.	
33	AV_{SS}	A/D converter power supply ground potential. Sets conversion's range lower limit.	

3

PIN IDENTIFICATION (cont.)

PIN NO.	PIN SYMBOL	FUNCTION
34–41	AN_0–AN_7	Eight analog inputs to the A/D converter. AN_7–AN_4 can also be used as a digital input port for falling edge detection.
42	V_{AREF}	Reference voltage for A/D converter. Sets conversion's range upper limit.
43	AV_{CC}	Power supply voltage for A/D converter.
44	$\overline{RD}$	(Three-state output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes high during Reset.
45	$\overline{WR}$	(Three-state output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes high during Reset.
46	ALE	The strobe signal is for latching the address signal to the output from PD_7–PD_0 when accessing external expansion memory.
47–54	PF_0–PF_7	Port F: (Three-state input/output) 8-bit programmable I/O port. Each line configurable independently as an input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
55–62	DB_0–DB_7	Port D: 8-bit programmable I/O port. This byte can be designated as either input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
63	V_{DD}	This ia a second power supply line for on-chip RAM back-up
64	V_{CC}	+5V power supply.

Notes:
1 clock cycle = 1 CL = 3/f.
1 machine cycle = 3 or 4 clock cycles.
1 instruction cycle = 1 to 19 machine cycles.
f: System clock frequency (MHz).

NEW INSTRUCTIONS

In addition to the existing instruction set for μPD7801, the following new instructions are incorporated in the μPD7810/11:

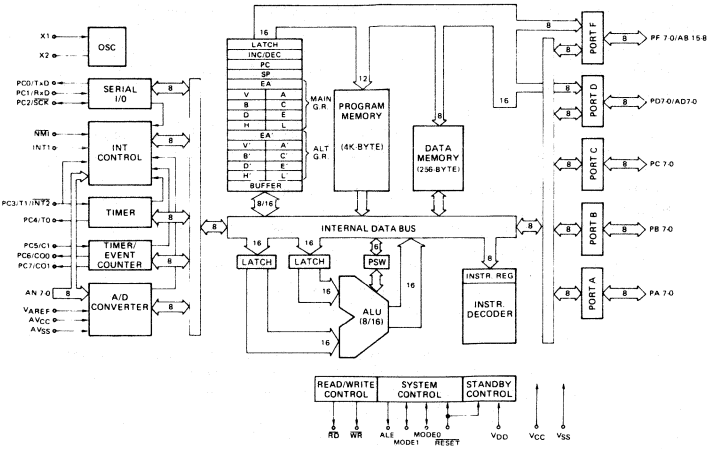
16-bit data transfer between memory and extended accumulator
16-bit data arithmetic and logical operation.

16-bit data addition and subtraction and 16-bit comparsion.
16-bit data shift and rotation
direct multiply and divide instructions.

8-bit by 8-bit division less then 8 μsec execution time.

16-bit divided by 8-bit less than 15 μsec execution
table look-up operation.
Register pair HL and DE are used as base register. Accumulator, B-register and extended accumulator are used as index register.

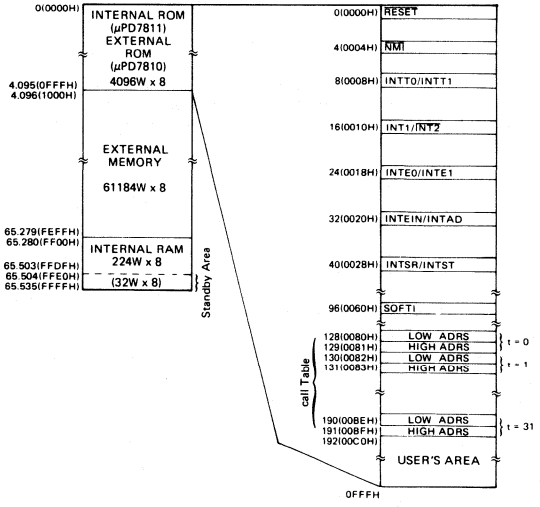
BLOCK DIAGRAM



Note: the μPD7810/10H has no programmable ROM (4K bytes) on chip.

MEMORY MAP

The μPD7811 can directly address up to 64K-bytes of memory. Except for the on-chip ROM (0-4095) and RAM (65280–65535), any memory location can be used as ROM or RAM. The following memory map defines the 0-64K-byte memory space for the μPD7811.



FUNCTIONAL DESCRIPTION

INPUT/OUTPUT

8 Analog Input Lines
44 Digital I/O Lines: five 8-bit ports (Port A, Port B, Port C, Port D, Port F) and 4 input lines (AN_4–AN_7)

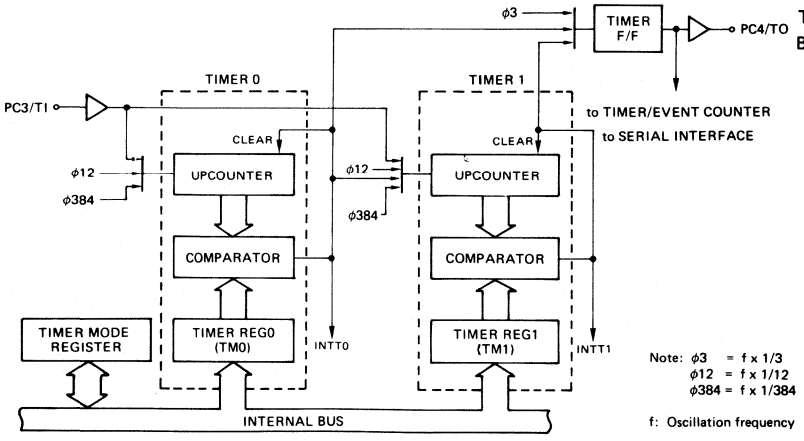
1. Analog Input Lines
   AN_0–AN_7 are configured as analog input lines for on-chip A/D converter.
2. Port Operation
   - Port A, Port B, Port C, Port F
     Each line of these ports can be individually programmed as an input or as an output. When used as I/O ports, all have latches outputs, high-impedance inputs.
   - Port D
     Port D can be programmed as a byte input or a byte output.
   - AN_4–AN_7
     The high-order analog input lines, AN_4–AN_7 can be used as digital input lines for falling edge detection.
3. Control Lines
   Under software control, each line of Port C can be configured individually to provide control lines for serial interface, timer and timer/counter, and interrupts.
4. Memory Expansion
   In addition to the single-chip operation mode the μPD7811 has 4 memory expansion modes. Under software control, Port D can provide multiplexed low-order address and data bus and Port F can provide high-order address bus. The relation between memory expansion modes and the pin configurations of Port D and Port F is shown in the table that follows.

MEMORY EXPANSION		PORT CONFIGURATION
None	Port D Port F	I/O Port I/O Port
256 Bytes	Port D Port F	Multiplexed Address/Data Bus I/O Port
4K Bytes	Port D Port F_0–F_3 Port F_4–F_7	Multiplexed Address/Data Bus Address Bus I/O Port
16K Bytes	Port D Port F_0–F_5 Port F_6–F_7	Multiplexed/Data Bus Address Bus I/O Port
60K Bytes	Port D Port F	Multiplexed Address/Data Bus Address Bus

TIMERS

The timer/event counter consists of two 8-bit timers. The timers may be programmed independently or may be cascaded and used as a 16-bit timer. The timer can be set by software to increment at intervals of 4 machine cycles (1μs at 12MHz operation) or 128 machine cycles (32μs at 12MHz), or to increment on receipt of a pulse at TI.

TIMER BLOCK DIAGRAM



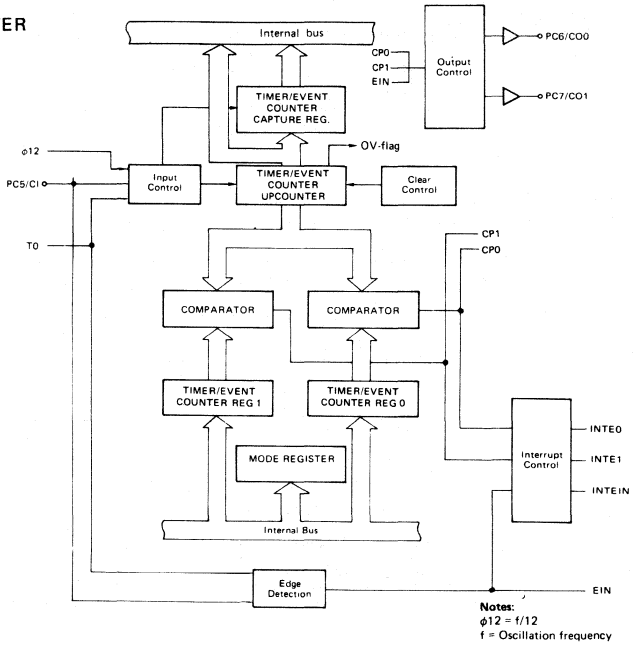
FUNCTIONAL DESCRIPTION (CONT.)

TIMER/EVENT COUNTER

The 16-bit Multifunctional timer/event counter can be used for the following operations:

- Interval timer
- External event counter
- Frequency measurement
- Pulse width measurement
- Programmable square-wave output
- Single pulse generation

TIMER/EVENT COUNTER BLOCK DIAGRAM



Notes:
φ12 = f/12
f = Oscillation frequency

ANALOG/DIGITAL CONVERTER

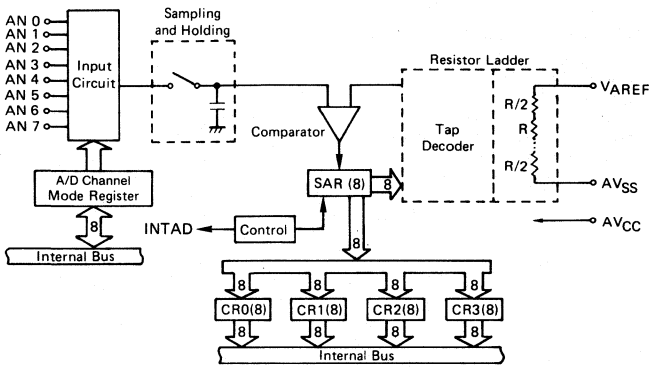
- 8 Input Channels
- 4 Conversion Result Registers
- 2 Powerful Operation Modes
  - Auto Scan Mode
  - Channel Select Mode
- Successive Approximation Technique

Absolute Accuracy	± 1.5 LSB (± 0.6%)
Conversion Range	0 ~ 5V
Conversion Time	48 μs

- Interrupt Generation

The μPD7810/7811 features an 8-bit, high-speed, high accuracy A/D converter. The A/D converter comprises a 256-Resistor Ladder and Successive Approximation Register (SAR). There are four conversion result registers (CR_0–CR_3). The 8-channel analog input may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR_0–CR_3. In the scan mode, the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers.

A/D CONVERTER BLOCK DIAGRAM

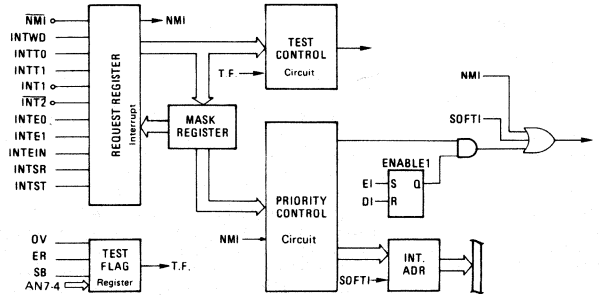


INTERRUPT STRUCTURE

There are 11 interrupt sources. Three are external interrupts and 8 are internal. These 11 interrupt sources are divided into 6 priority levels as shown in the table below.

INTERRUPT REQUEST	INTERRUPT VECTOR	TYPE OF INTERRUPT		IN/EXT
IRQ0	4	NMI	(Non-maskable interrupt)	External
IRQ1	8	INTT0 INTT1	(Coincidence signal from timer 0) (Coincidence signal from timer 1)	Internal
IRQ2	16	INT1 INT2	(Maskable intrrupt) (Maskable interrupr)	External
IRQ3	24	INTE0 INTE1	(Coincidence signal from timer/ event counter) Coincidence signal from timer/ event counter)	Internal
IRQ4	32	INTEIN INTAD	(Falling signal of C1 and T0 counter) (A/D converter interrupt)	In/External
IRQ5	40	INTSR INST	(Serial receive interrupt) (Serial send interrupt)	Internal

INTERRUPT CONTROL BLOCK DIAGRAM



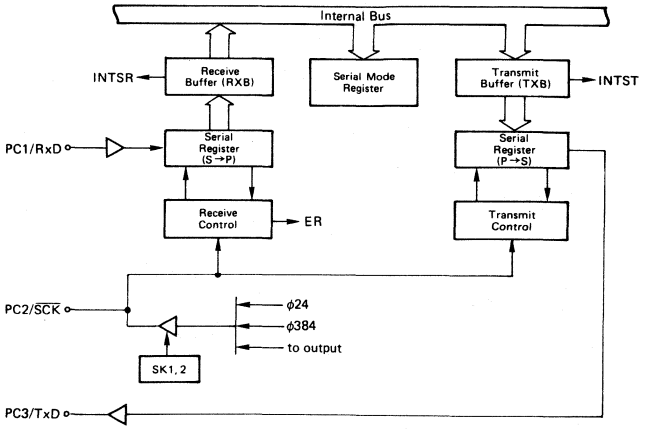
STANDBY FUNCTION

The μPD7810/7811 offers a standby function that allows the user to save up to 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On powerup the μPD7811 checks whether recovery was made from standby mode or from cold start.

UNIVERSAL SERIAL INTERFACE

The serial interface can operate in any of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first for ease of communication with certain peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception. In the search mode, data are transferred one bit at a time from serial register to receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from serial register to transmit buffer occurs 8 bits at a time.

UNIVERSAL SERIAL INTERFACE BLOCK DIAGRAM



Note: $\phi 24 = \frac{1}{24}$

f: oscillation frequency (MHz)

$\phi 384 = \frac{1}{384}$

ZERO-CROSSING DETECTOR

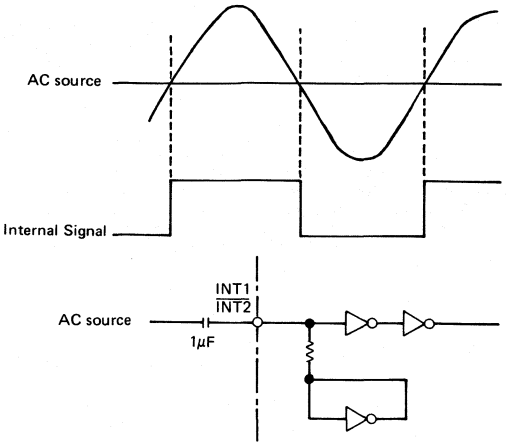
The INT1 and INT2 terminals (used also as TI and PC_3) can be used to detect the zero-crossing point of slow moving AC signals. When driven directly, these pins respond as a normal digital input.

To utilize the zero-cross detection mode, an AC signal of approximately 1 – 1.8V peak-to-peak magnitude and a maximum frequency of 1kHz is coupled through an external capacitor to these pins.

For the INT1 pin, the internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one and INT1 interrupt is generated.

For the INT2 pin, the state is sensed as a one until the falling edge crosses the DC average level, when it becomes a zero and INT2 interrupt is generated.

The zero-cross detection capability allows the user to make the 50–60Hz power signal the basis for system timing and to control voltage phase sensitive devices.



ZERO-CROSSING
DETECTION CIRCUIT

MODE0/MODE1-TERMINALS

The logic level applied to M0/M1-Terminals determines the memory map of μPD7810/7811 and the use of Port D/F as multiplexed Address/Data Bus.

M0	M1	MEMORY	ADDRESSES	LOCATION
0	1	4K	0 . . . . . FFFH	internal*
0	0	4K	0 . . . . . FFFH	external
0	1	16K	0 . . . . . 3FFFH	external
1	0	64K	0 . . . . . FEFFH	external

* MO, M1 = 0,1 realizes the ROM version (access of internal ROM), all others represent access of external memory only. In case external memory is used in addition to internal, memory mapping register has to be programmed then (see below).

MEMORY EXPANDES MODES	MEMORY MAPPING REGISTER			NUMBER OF I/O LINES
	MM2	MM1	MM0	
Port Mode	0	0	X	44
256 Expanded	0	1	0	36
4K Expanded	1	0	0	32
16K Expanded	1	1	0	30
60K Expanded	1	1	1	28

(using μPD7811)

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
	AV_{CC}		−0.5 to +7.0	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Reference Input Voltage	V_{AREF}		−0.5 to V_{CC}	V
Operating Temperature	T_{opt}	10 MHz < f_{XTAL} ≤ 12 MHz	−10 to +70	°C
		f_{XTAL} ≤ 10 MHz	−40 to + 85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OPERATING CONDITION

PARAMETER / OSC. FREQ.	T_a	V_{CC}, AV_{CC}
10 MHz < f_{XTAL} ≤ 12 MHz	−10°C to +70°C	+5.0V ± 5 %
f_{XTAL} ≤ 10 MHz	−40°C to +85°C	+5.0V ± 10 %

CAPACITANCE

(T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_c = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except SCK, RESET, X1 and X2	2.0		V_{CC}	V
	V_{IH2}	SCK, X1, X2 *1	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	RESET	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_{IN} ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_{IN} ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	0.45V ≤ V_O ≤ V_{CC}			± 10	μA
AV_{CC} Supply Current	AI_{CC}			6	12	mA
V_{DD} Supply Current	I_{DD}	μPD7811, 7810		1.5 *2	3.2	mA
		μPD78PG11E		1.5 *2	3.2	mA
V_{CC} Supply Current	I_{CC}	μPD7811,7810		150 *2	200	mA
		μPD78PG11E		140 *2	230	mA
Data Retention Voltage	V_{DDDR}	V_{CC} = 0V, RESET = V_{IL}	3.2			V

*2: T_a = 25°C, V_{CC} = V_{DD} = +5.0V

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≦ V_{DD} ≦ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE ↓	t_{AL}		65		ns
Address Hold from ALE ↓	t_{LA}		50		ns
Address to RD ↓ Delay Time	t_{AR}		150		ns
RD ↑ to Address Floating	t_{AFR}			20	ns
Address to Data Input	t_{AD}			360	ns
ALE ↓ to Data Input	t_{LDR}			215	ns
RD↓ to Data Input	t_{RD}			180	ns
ALE ↓ to RD ↓ Delay Time	t_{LR}		35		ns
Data Hold Time from RD ↑	t_{RDH}		0		ns
RD ↑ to ALE↓ Delay Time	t_{RL}		115		ns
RD Width Low	t_{RR}	Data Read	280		ns
		OP Code Fetch	530		ns
ALE Width High	t_{LL}		125		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*3, *6	65		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*3, *6	50		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*3, *7	65		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*3, *7	50		ns
Adress to WR ↓ Delay	t_{AW}		150		ns
ALE ↓ to Data Output	t_{LDW}			195	ns
WR ↓ to Data Output	t_{WD}			100	ns
ALE ↓ to WR ↓ Delay Time	t_{LW}		35		ns
Data Setup Time to WR ↑	t_{DW}		230		ns
Data Hold Time from WR ↑	t_{WDH}		95		ns
WR ↑ to ALE ↑ Delay Time	t_{WL}		115		ns
WR Width Low	t_{WW}		280		ns
Address to Data Input Delay	t_{ACC}	78PG11E only		360	ns

Note 1: f_{XTAL} = 10 MHz
2: Load Capacitance: C_L = 150pF

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*8	1.66		μs
			*9	500		ns
		$\overline{SCK}$ Output		2		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*8	750		ns
			*9	200		ns
		$\overline{SCK}$ Output		900		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*8	750		ns
			*9	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*8		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*8		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*8			210	ns

*8: 1x Baud Rate in Asynchronous, Synchronous, I/O Interface Mode
*9: 16x Baud Rate or 64x Baud Rate in Asynchronous

ZERO-CROSS CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} −0.8V ≦ V_{DD} ≦ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

A/D CONVERTER CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = AV_{CC} = +5.0V ± 5 %, V_{SS} = AV_{SS} = 0V, AV_{CC} −0.5 ≤ V_{AREF} ≤ AV_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	Min	TYP		UNITS
Resolution			8			Bits
Absolute Accuracy		T_a = −10°C to +50°C 83ns ≤ t_{CYC} ≤ 170ns			0.4% ± 1/2	LSB
		83ns ≤ t_{CYC} ≤ 170ns			0.6% ± 1/2	LSB
Conversion Time	t_{CONV}	83ns ≤ t_{CYC} ≤ 110ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling Time	t_{SAMP}	83ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤170ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
V_{AREF} Current	I_{AREF}		0.2	0.5	1.5	mA

3

EXTENDED TEMPERATURE

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

DC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1, X2	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1, X2 *1	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_{IN} ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_{IN} ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	0.45V≤V_O≤V_{CC}			± 10	μA
AV_{CC} Supply Current	AI_{CC}			6	12	mA
V_{DD} Supply Current	I_{DD}	μPD7811, 7810		1.5 *2	3.5	mA
		μPD78PG11E		1.5 *2	3.5	mA
V_{CC} Supply Current	I_{CC}	μPD7811,7810		150 *2	220	mA
		μPD78PG11E		140 *2	250	mA
Data Retention Voltage	V_{DDDR}	V_{CC} = OV, $\overline{RESET}$ = V_{IL}	3.2			V

AC CHARACTERISTICS READ/WRITE OPERATION

EXTENDED TEMPERATURE

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		100	250	ns
Address Setup to ALE ↓	t_{AL}		100		ns
Address Hold from ALE ↓	t_{LA}		70		ns
Address to RD ↓ Delay Time	t_{AR}		200		ns
RD ↓ to Address Floating	t_{AFR}			20	ns
Address to Data Input	t_{AD}			480	ns
ALE ↓ to Data Input	t_{LDR}			300	ns
RD↓ to Data Input	t_{RD}			250	ns
ALE ↓ to RD ↓ Delay Time	t_{LR}		50		ns
Data Hold Time from RD ↑	t_{RDH}		0		ns
RD ↑ to ALE↑ Delay Time	t_{RL}		150		ns
RD Width Low	t_{RR}	Data Read	350		ns
		OP Code Fetch	650		ns
ALE Width High	t_{LL}		160		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*6	100		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*6	70		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*7	100		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*7	70		ns
Adress to WR ↓ Delay	t_{AW}		200		ns
ALE ↓ to Data Output	t_{LDW}			210	ns
WR ↓ to Data Output	t_{WD}			100	ns
ALE ↓ to WR ↓ Delay Time	t_{LW}		50		ns
Data Setup Time to WR ↑	t_{DW}		300		ns
Data Hold Time from WR ↑	t_{WDH}		130		ns
WR ↑ to ALE ↑ Delay Time	t_{WL}		150		ns
WR Width Low	t_{WW}		350		ns
Address to Data Input Delay	t_{ACC}	78PG11E only		480	ns

Note 1: f_{XTAL} = 10 MHz
2: Load Capacitance; C_L = 150pF

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*8	2.0		μs
			*9	500		ns
		$\overline{SCK}$ Output		2.4		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*8	920		ns
			*9	200		ns
		$\overline{SCK}$ Output		1.1		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*8	920		ns
			*9	200		ns
		$\overline{SCK}$ Output		1.1		μs
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*8		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*8		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*8			210	ns

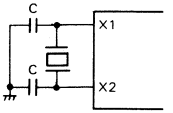
ZERO-CROSS CHARACTERISTICS

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

EXTENDED TEMPERATURE

*1 The following oscillation circuit using XTAL is recommended.



C=10 pF

*2 T_a = +25 °C, V_{CC} = V_{DD} = 5 V

*3 f_{XTAL} = 12 MHz

*4 f_{XTAL} = 10 MHz

*5 Load capacitance : C_L = 150 pF

*6 MODE0, MODE1 pins are connected to V_{CC} through R in μPD7810, μPD7811, μPD78PG11E

*7 MODE0, MODE1 pins are connected to V_{CC} through R in μPD7810

*8 1xBaud Rate in Asynchronous, Synchronous, I/O Interface Mode

*9 16x, 64x Baud Rate in Asynchronous

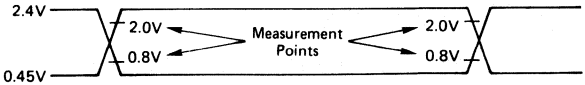
A/D CONVERTER CHARACTERISTICS

EXTENDED TEMPERATURE

(T_a = −40°C to +85°C, V_{CC} = AV_{CC} = +5.0V ± 10%, V_{SS} = AV_{SS} = 0V, AV_{CC} −0.5V ≦ V_{AREF} ≦ AV_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	Min	TYP		UNITS
Resolution			8			Bits
Absolute Accuracy		T_a = −10°C to +50°C 100ns ≦ t_{CYC} ≦ 170ns			0.4% ± 1/2	LSB
		100ns ≦ t_{CYC} ≦ 170ns			0.6% ± 1/2	LSB
Conversion Time	t_{CONV}	100ns ≦ t_{CYC} ≦ 170ns	576			t_{CYC}
		110ns ≦ t_{CYC} ≦ 170ns	432			t_{CYC}
Sampling Time	t_{SAMP}	100ns ≦ t_{CYC} ≦ 110ns	96			t_{CYC}
		110ns ≦ t_{CYC} ≦170ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
V_{AREF} Current	I_{AREF}		0.2	0.5	1.5	mA

AC TIMING MEASUREMENT POINT



BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220	MAX	ns
t_{LDR}	5T − 200	MAX	ns
t_{RD}	4T − 150	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read)	MIN	ns
	7T − 50 (OP Code Fetch)		
t_{LL}	2T − 40	MIN	ns
t_{ML} *2	2T − 100	MIN.	ns
t_{LM} *2	T − 30	MIN.	ns
t_{IL} *3	2T − 100	MIN.	ns
t_{LI} *3	T − 30	MIN.	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50	MIN	ns
t_{CYK}	20T ($\overline{SCK}$ Input) *1	MIN	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	10T − 80 ($\overline{SCK}$ Input) *1	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		
t_{KKH}	10T − 80 ($\overline{SCK}$ Input) *1	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		

*1: 1x Baud Rate in Asynchronous, Synchronous, I/O Interface Mode.
*2: MODE0, MODE1 pins are connected to V_{CC} through R.
*3: MODE0, MODE1 pins are connected to V_{CC} through R in μPD7810.

Note: T = t_{CYC} = $1/f_{XTAL}$

3

OTHER OPERATIONS

(T_a = −10°C to +70°C, V_{CC} = +5.0V± 5%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})
(T_a = −40°C to + 85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0,8V ≤ V_{DD} ≤ V_{CC})

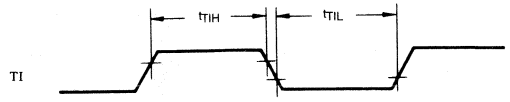
Parameter	Symbol	Conditions	MIN	MAX	UNITS
TI width high, low	t_{TIH}, t_{TIL}		6		t_{CYC}
CI width high, low	t_{CI1H}, t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ width high, low	t_{NIH}, t_{NIL}		36		t_{CYC}
INT1 width high, low	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ width high, low	t_{I2H}, t_{I2L}		36		t_{CYC}
$\overline{RESET}$ width high, low	t_{RSH}, t_{RSL}		60		t_{CYC}

EXTERNAL CLOCK TIMING

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} =0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})
(T_a = −40°C to + 85°C, V_{CC} = + 5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

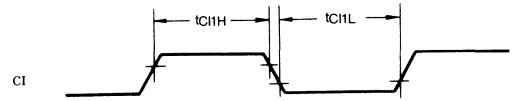
Parameter	Symbol	Twst Conditions	MIN	MAX	UNITS
X1 input width high	$t_{ØH}$		30	250	ns
X1 input width low	$t_{ØL}$		30	250	ns
X1 input rise time	t_r		0	30	ns
X1 input fall time	t_f		0	30	ns

TIMER INPUT TIMING

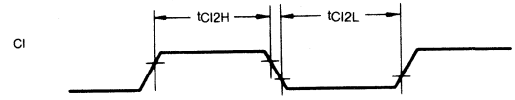


TIMER/EVENT COUNTER INPUT TIMING

EVENT COUNT MODE

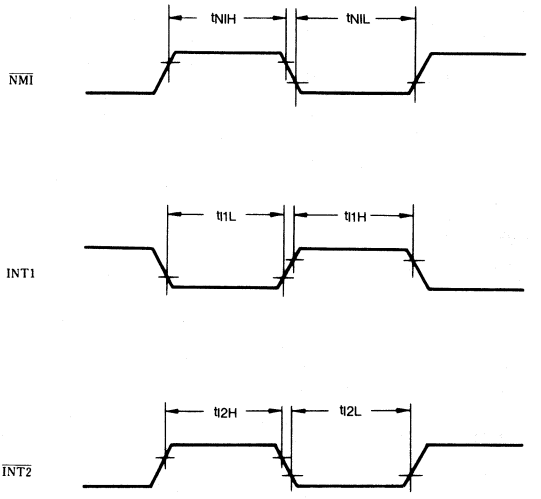


PULSE WIDTH MEASUREMENT MODE

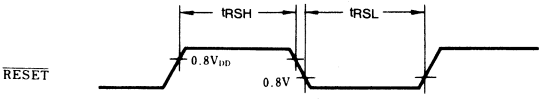


3

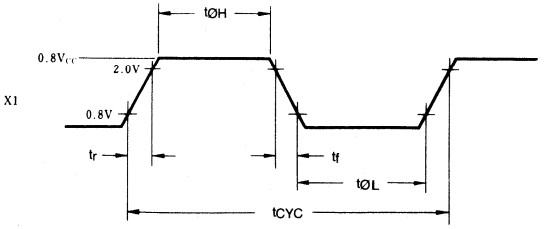
INTERRUPT INPUT TIMING



RESET INPUT TIMING



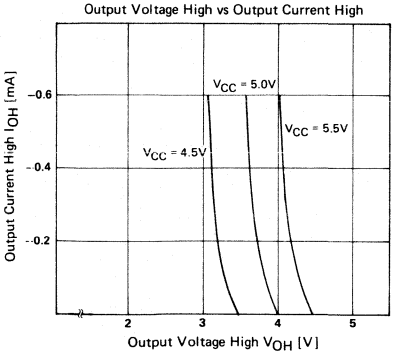
EXTERNAL CLOCK TIMING



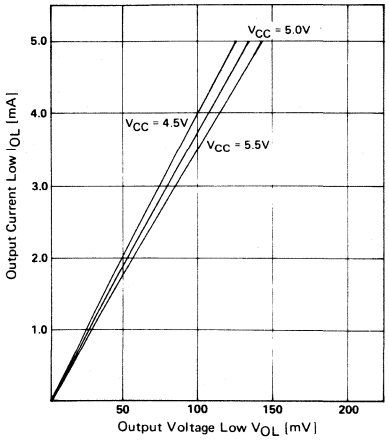
CHARACTERISTICS CURVE
– REFERENCE –

(T_a = 25°C)

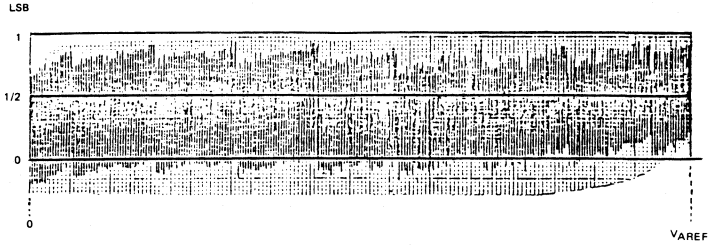
Output Voltage High vs Output Current High



Output Voltage Low vs Output Current Low

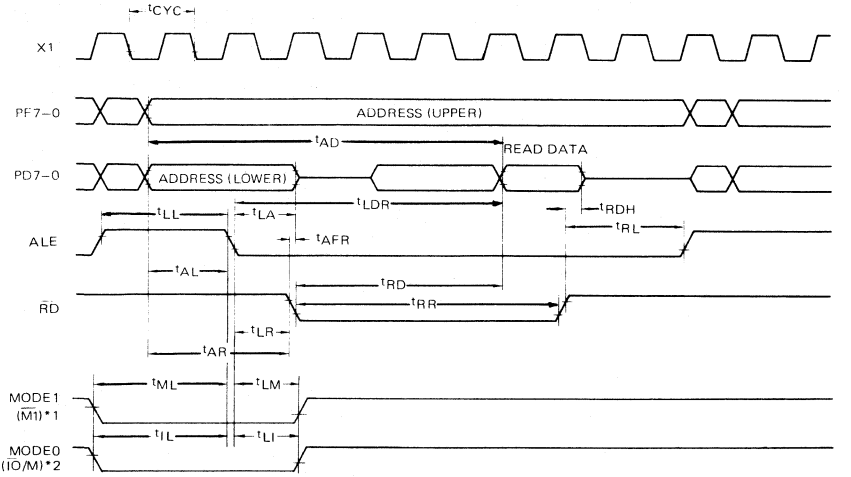


CHARACTERISTIC OF A/D CONVERTER



TIMING WAVEFORM

Read Operation

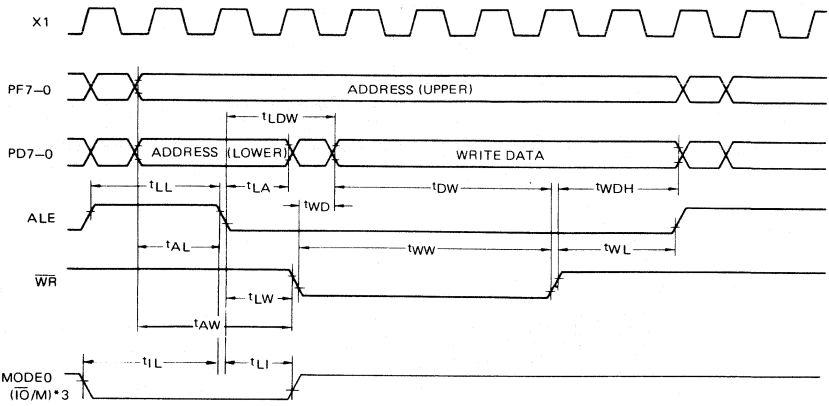


*1 $\overline{M1}$ is output at the fetch cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

*2 $\overline{IO}/M$ is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

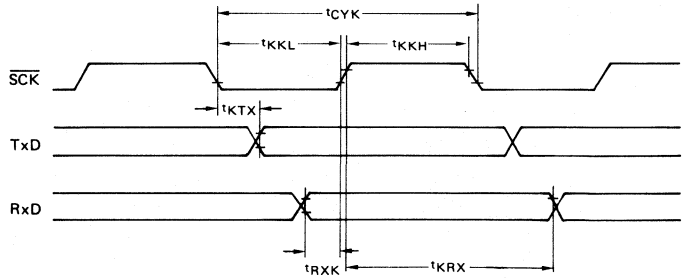
TIMING WAVEFORM

Write Operation

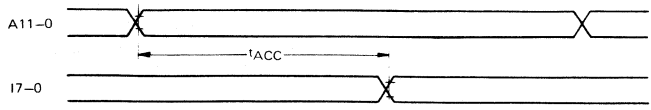


*3 $\overline{IO}$/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

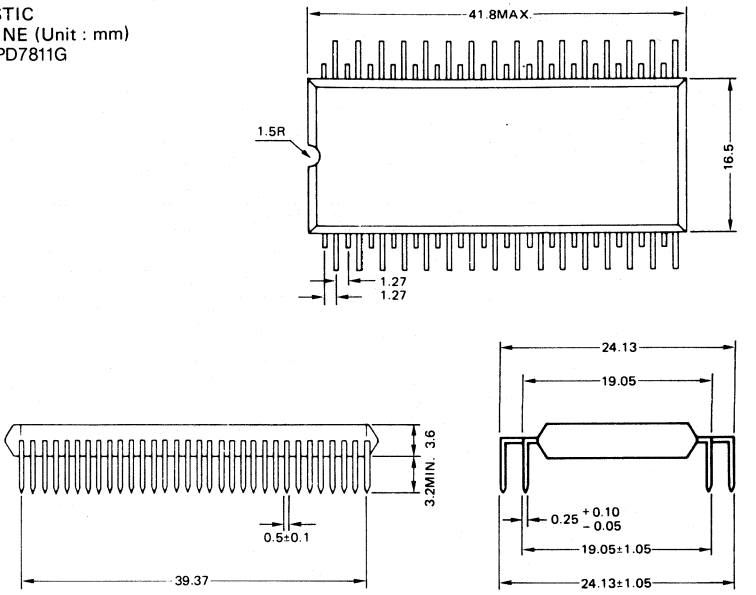
Serial Operation



EPROM Timing (for μPD78PG11E)

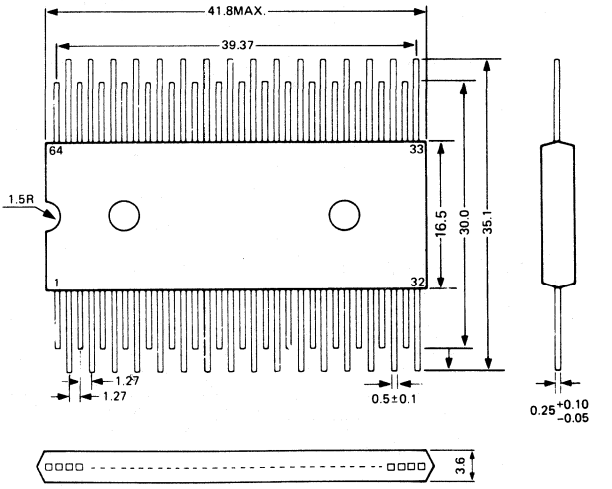


64 PIN PLASTIC
QUIP OUTLINE (Unit : mm)
μPD7801G/μPD7811G



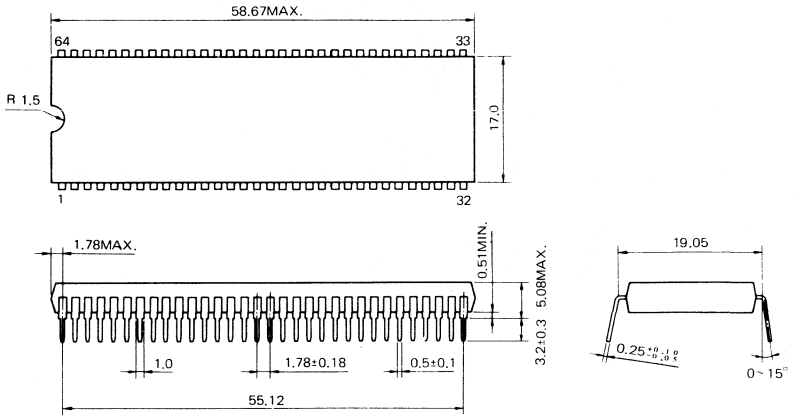
When ordering this package, specify as follows:
μPD7810G-36
μPD7811G-xxx-36

64 PIN PLASTIC QUIP OUTLINE
FLAT LEADS
(Unit : mm)
μPD7811G



When ordering this package, specify as follows: μPD7811G-XXX-37

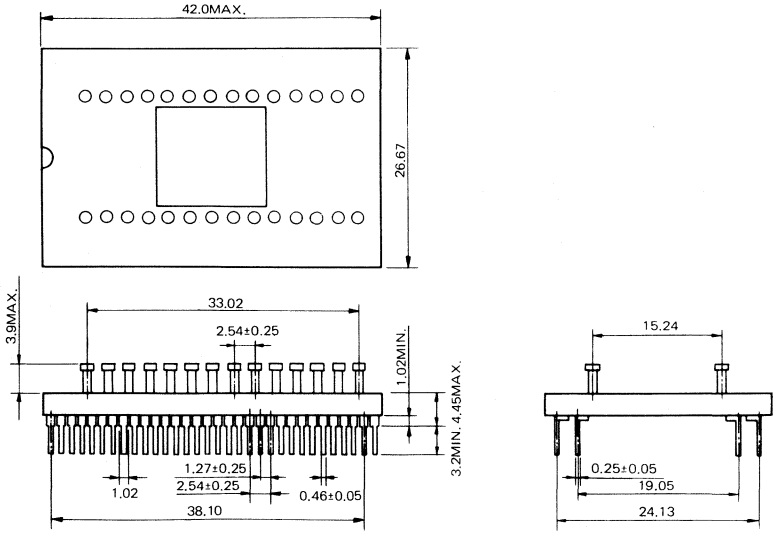
64 PIN PLASTIC
SHRINK DIP OUTLINE (Unit : mm)
μPD 7810CW/μPD7811CW

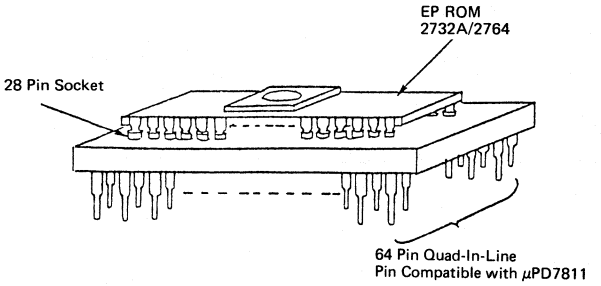


When ordering this package, specify as follows:
μPD7810CW

3

64 PIN CERAMIC
PIGGY BACK QUIP OUTLINE (Unit : mm)
μPD78PG11E





QUIL CERAMIC PIGGY BACK
PACKAGE OUTLINE
μPD78PG11E

- μPD78PG11E can access eprom when addressing 0 to 4095
- All memory of the 2732A memory (4K-Byte memory)
- Lower 4K-Byte of the 2764 memory (8K-Byte memory)

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
	AV_{CC}		−0.5 to +7.0	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Reference Input Voltage	V_{AREF}		−0.5 to V_{CC}	V
Operating Temperature	T_{opt}	$f_{XTAL} \leq$ 15 MHz	−10 to +70	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OPERATING CONDITION

PARAMETER / OSC. FREQ.	T_a	V_{CC}, AV_{CC}
$f_{XTAL} \leq$ 15 MHz	−10°C to +70°C	+5.0V ± 10 %

CAPACITANCE

(T_a= 25°C, $V_{CC} = V_{DD} = V_{SS}$ = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_C = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ $V_{DD} \leq V_{CC}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ $V_I \leq V_{CC}$			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ $V_I \leq V_{CC}$			± 10	μA
Output Leakage Current	I_{LO}	$0.45V \leq V_O \leq V_{CC}$			± 10	μA
AV_{CC} Supply Current	AI_{CC}			6	12	mA
V_{DD} Supply Current	I_{DD}			1.5 *1	3.2	mA
V_{CC} Supply Current	I_{CC}			150 *1	200	mA
Data Retention Voltage	V_{DDDR}	$V_{CC} = 0$, $\overline{RESET} = V_{IL}$	3.2			V

*1: T_a = 25°C, $V_{CC} = V_{DD}$ = +5.0V

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ±10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		66	250	ns
Address Setup to ALE ↓	t_{AL}		30		ns
Address Hold from ALE ↓	t_{LA}		35		ns
Address to RD ↓Delay Time	t_{AR}		100		ns
RD ↓to Address Floating	t_{AFR}			20	ns
Address to Data Input	t_{AD}			250	ns
ALE ↓to Data Input	t_{LDR}			135	ns
RD↓to Data Input	t_{RD}			120	ns
ALE ↓to RD ↓Delay Time	t_{LR}		15		ns
Data Hold Time from RD ↑	t_{RDH}		0		ns
RD ↑ to ALE↑ Delay Time	t_{RL}		80		ns
RD Width Low	t_{RR}	Data Read	215		ns
		OP Code Fetch	415		ns
ALE Width High	t_{LL}		90		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}		30		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}		35		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}		30		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}		35		ns
Adress to WR ↓Delay	t_{AW}		100		ns
ALE ↓to Data Output	t_{LDW}			180	ns
WR ↓to Data Output	t_{WD}			100	ns
ALE ↓to WR ↓Delay Time	t_{LW}		15		ns
Data Setup Time to WR ↑	t_{DW}		165		ns
Data Hold Time from WR ↑	t_{WDH}		60		ns
WR ↑to ALE ↑Delay Time	t_{WL}		80		ns
WR Width Low	t_{WW}		215		ns

Note 1: f_{XTAL} = 12 MHz
2: Load Capacitance; C_L = 150pF

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*2	800		ns
			*3	500		ns
		$\overline{SCK}$ Output		1.6		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*2	335		ns
			*3	200		ns
		$\overline{SCK}$ Output		700		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*2	335		ns
			*3	200		ns
		$\overline{SCK}$ Output		700		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*2		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*2		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*2			210	ns

*2: 1x Baud Rate in Asynchronous, Synchronous, I/O Interface Mode
*3: 16x Baud Rate or 64x Baud Rate in Asynchronous

ZERO-CROSS CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

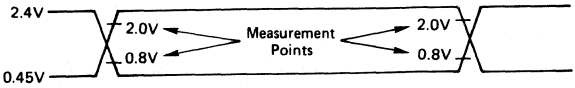
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

A/D CONVERTER CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = AV_{CC} = +5.0V ±10%, V_{SS} = AV_{SS} = 0V, AV_{CC} − 0.5 ≤ V_{AREF} ≤ AV_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	Min	TYP		UNITS
Resolution			8			Bits
Absolute Accuracy		T_a = 0°C to +70°C, 66ns ≤ t_{CYC} ≤ 170ns			0.4% ± 1/2	LSB
Conversion Time	t_{CONV}	66ns ≤ t_{CYC} ≤ 110ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling Time	t_{SAMP}	66ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
V_{AREF} Current	I_{AREF}		0.1	2.0	5.0	mA

AC TIMING MEASUREMENT POINT



BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220	MAX	ns
t_{LDR}	5T − 200	MAX	ns
t_{RD}	4T − 150	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read)	MIN	ns
	7T − 50 (OP Code Fetch)		
t_{LL}	2T − 40	MIN	ns
t_{ML} *2	2T − 100	MIN.	ns
t_{LM} *2	T − 30	MIN.	ns
t_{IL} *3	2T − 100	MIN.	ns
t_{LI} *3	T − 30	MIN.	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50	MIN	ns
t_{CYK}	12T ($\overline{SCK}$ Input) *1	MIN	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	5T + 5 ($\overline{SCK}$ Input) *1	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		
t_{KKH}	5T + 5 ($\overline{SCK}$ Input) *1	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		

*1: 1x Baud Rate in Asynchronous, Synchronous, I/O Interface Mode.

Note 1: T = t_{CYC} = 1/f_{XTAL}

2: The items out of this table are not dependent on f_{XTAL}.

3

OTHER OPERATIONS

(T_a = −10°C to + 70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

Parameter	Symbol	Conditions	MIN	MAX	UNITS
TI width high, low	t_{TIH}, t_{TIL}		6		t_{CYC}
CI width high, low	t_{CI1H}, t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ width high, low	t_{NIH}, t_{NIL}		36		t_{CYC}
INT1 width high, low	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ width high, low	t_{I2H}, t_{I2L}		36		t_{CYC}
$\overline{RESET}$ width high, low	t_{RSH}, t_{RSL}		60		t_{CYC}

EXTERNAL CLOCK TIMING

(T_a = −10°C to + 70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

Parameter	Symbol	Test Condition	MIN	MAX	UNITS
X1 input width high	$t_{\phi H}$		20	250	ns
X1 input width low	$t_{\phi L}$		20	250	ns
X1 input rise time	t_r		0	20	ns
X1 input fall time	t_f		0	20	ns

RECOMENDED CERAMIC RESONATORS FOR μPD7810H AND μPD7811H

(T_a = −10°C to +70°C)

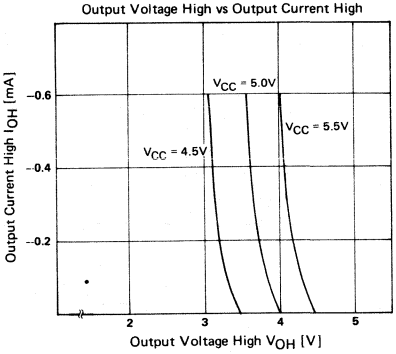
Manufacturer	Product name	Recommended circuit constants (pF)	
		C1	C2
Murata	CSA15.00X3	22	22
	CSA12.0MT	30	30
	CSA 7.37MT		

Caution: To use a crystal resonator, the following external capacitors are recommended:
C1 = C2 = 10 pF

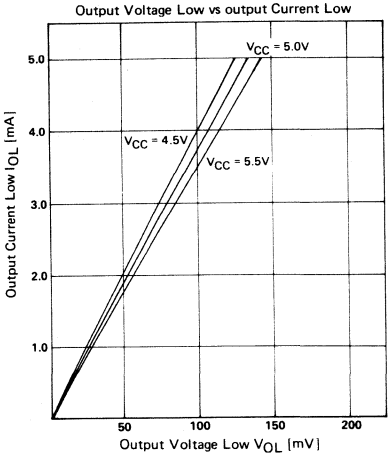
CHARACTERISTICS CURVE
– REFERENCE –

(T_a = 25°C)

Output Voltage High vs Output Current High



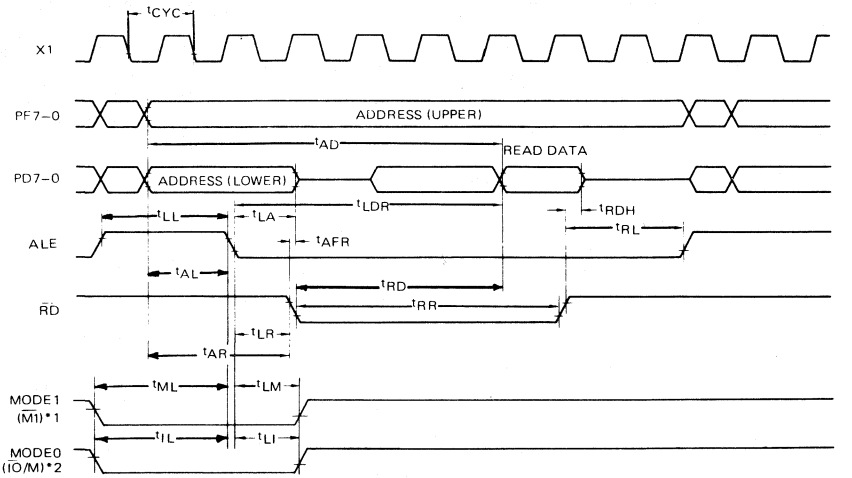
Output Voltage Low vs output Current Low



3

TIMING WAVEFORM

Read Operation

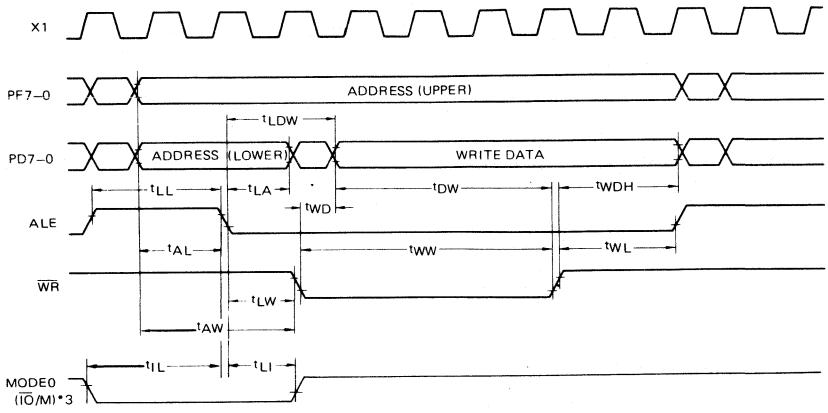


*1 $\overline{M_1}$ is output at the fetch cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

*2 $\overline{IO}/M$ is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

TIMING WAVEFORM

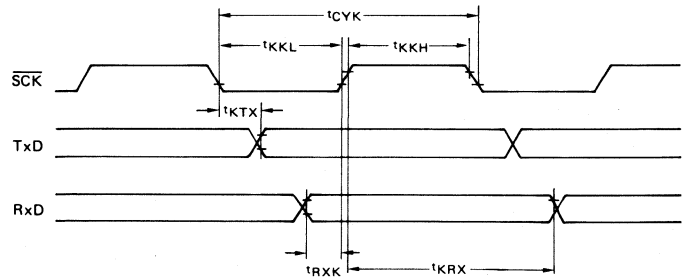
Write Operation



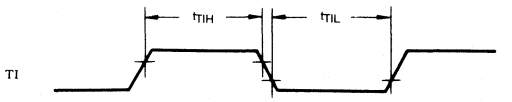
*3 $\overline{IO}$/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

3

Serial Operation

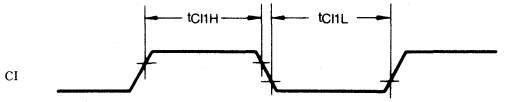


TIMER INPUT TIMING

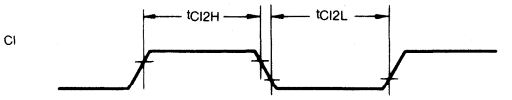


TIMER/EVENT COUNTER INPUT TIMING

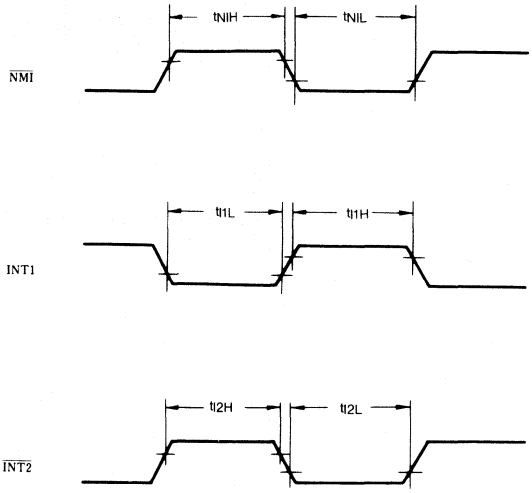
EVENT COUNT MODE



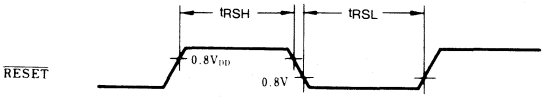
PULSE WIDTH MEASUREMENT MODE



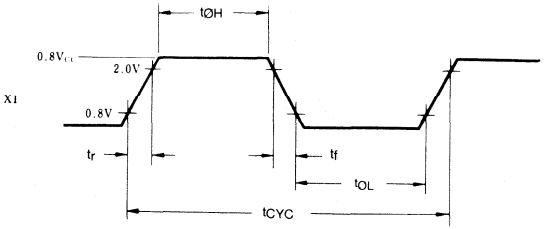
INTERRUPT INPUT TIMING



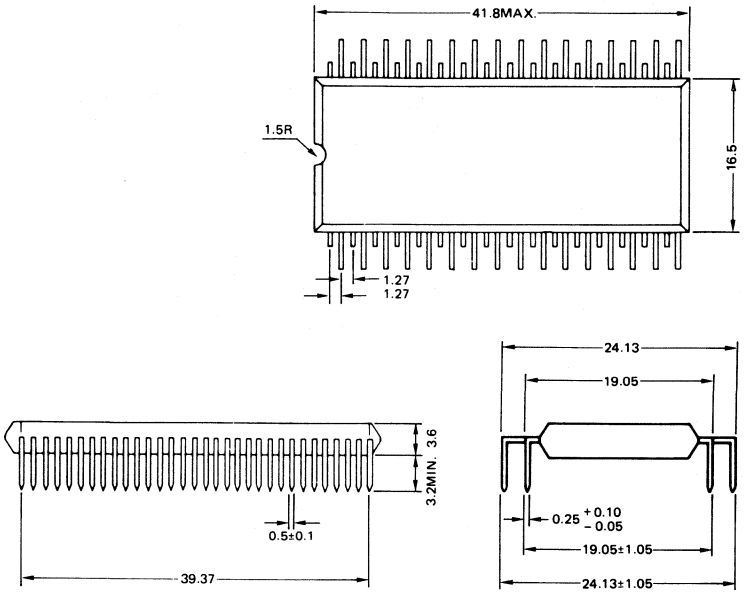
RESET INPUT TIMING



EXTERNAL CLOCK TIMING

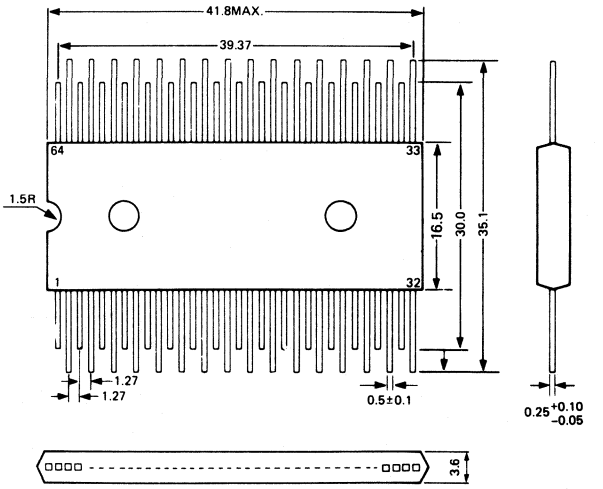


64 PIN PLASTIC
QUIP OUTLINE (Unit : mm)
μPD7810HG/μPD7811HG



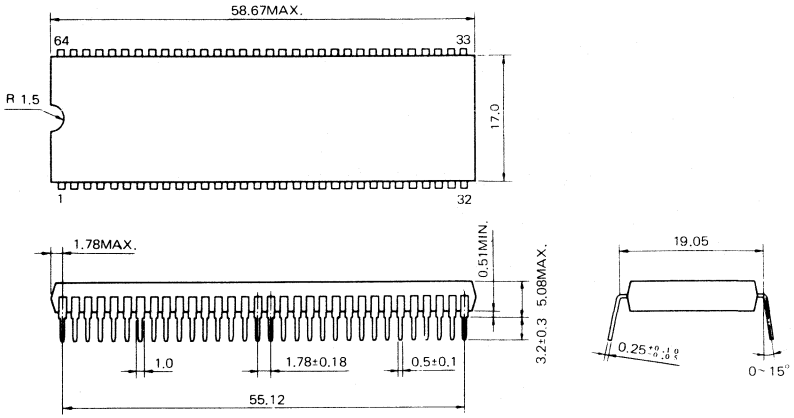
When ordering this package, specify as follows:
μPD7810HG-36
μPD7811HG-xxx-36

64 PIN PLASTIC
QUIP PACKAGE OUTLINE
(Unit : mm)
μPD7811HG



When ordering this package, specify as follows: μPD7811HG-XXX-37

64 PIN PLASTIC
SHRINK DIP OUTLINE (Unit : mm)
μPD7810HCW/μPD7811HCW



When ordering this package, specify as follows:
μPD7810HCW
μPD7811HCW-xxx

3

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH ON CHIP A/D CONVERTER

DESCRIPTION

The NEC μPD87C10/C11/C14/C10A/C11A/C12A/C14A are CMOS derivatives of the μPD7810/11. The NEC μPD87C10/C11/C14/C10A/C11A/C12A/C14A are high-performance single-chip microcomputers integrating sophisticated on-chip peripheral functionality normally provided by external components.

The devices's internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make μPD78C10/C11/C14/C11A/C12A/C14A appropriate for data processing as well as control applications. The device integrates a 16-bit ALU, 4K-ROM, 256-byte RAM with an 8-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a USART and two zerocross detect inputs on a single die, to direct the device into fast, high-end processing applications involving analog signal interface and processing.

The μPD87C10/C11/C14/C11A/C12A/C14Aare the mask-ROM high volume production devices embedded with customer program. The μPD78C11A/C12A/C14A are advanced version of μPD78C11/C14 with an enhanced serial interface and mask option for pull-up resistors on PORT A, B, C.

The μPD78C10 is a ROM-less version for prototyping and small volume production. For final evaluation the μPD78CG14E (Piggy back version) or the μPD78CP14 (OTP version) is available.

FEATURES

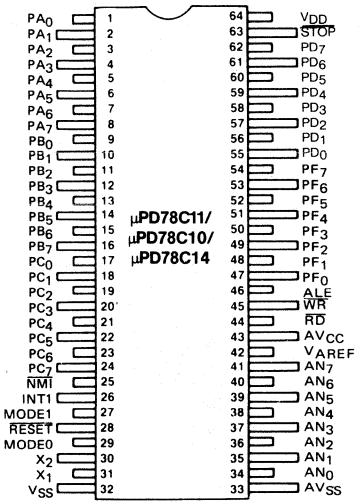
- Powerful Instruction Set Including 16-bit Multiply and Divide, 158 instructions
- High-Speed 1 μsec Cycle Time-12 MHz Operation
- On-Chip 4K-Byte ROM (78C11), 8K-Byte ROM (78C12A), 16K-Byte ROM (78C14), 256-Byte RAM
- 44 I/O Lines
- Easily Expandable Memory up to 60K Bytes/48K Bytes (externally)
- On-Chip 8-Bit A/D Converter-8 Input Channels
- Multi-Functional 16-Bit Timer/Counter
- Two Programmable 8-Bit Timers
- Full-Duplex Serial Communication Interface, synchronous and asynchronous
- Zero-Cross Detection Capability
- Vectored Interrupts, 3 external/8 internal
- Low Power Standby Operation
- 8085A Bus Compatible
- Singel Power Supply +5V, CMOS Technology
- Available in 64 Pin/68 Pin Packages (QUIP, FLAT, SHRINK DIP, PLCC)
- Standby functions
- On-chip clock generator
- 64K-Byte total memory address range

ORDERING INFORMATION

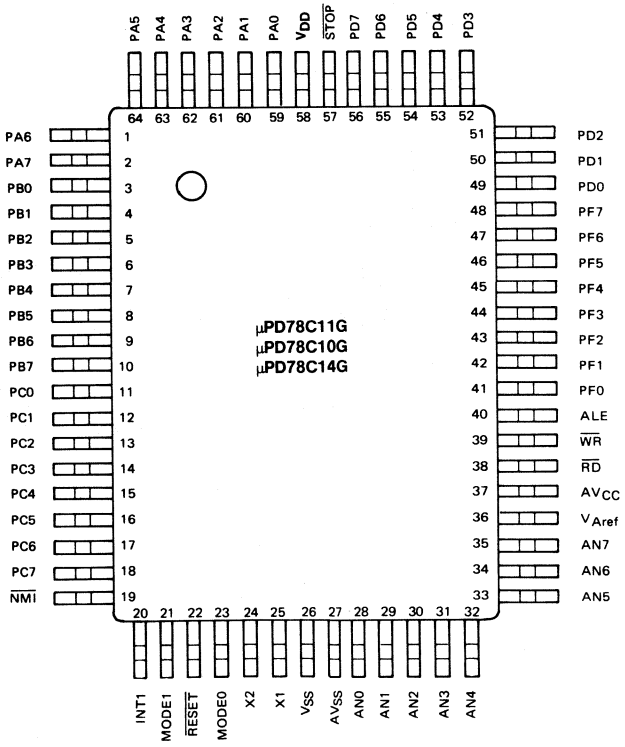
PART NUMBER	PACKAGE TYPE	ROM & SPECIAL FEATURES
μPD78C10CW	64-PIN SDIP	ROM-Less
μPD78C10G-1B	64-PIN FLAT (2.05 mm)	
μPD78C10GF	64-PIN FLAT (2.7 mm)	
μPD78C10G-36	64-PIN QUIP (Bent)	
μPD78C10L	68-PIN PLCC	
μPD78C10G-S	64-PIN QUIP (Bent)	ROM-Less;
μPD78C10L-S	68-PIN PLCC	S-Grade, –40 to +110°C
μPD78C11G-S-XXX-36	64-PIN QUIP (Bent)	4K MASK ROM;
μPD78C11L-S-XXX	68-PIN PLCC	S-Grade, –40 to +110°C
μPD78C11G-XXX-1B	64-PIN FLAT (2.05 mm)	4K MASK ROM
μPD78C11GF-XXX	64-PIN FLAT (2.7 mm)	
μPD78C11G-XXX-37	64-PIN QUIP (Straight)	
μPD78C11G-XXX-36	64-PIN QUIP (Bent)	
μPD78C11L-XXX	68-PIN PLCC	
μPD78C14CW-XXX	64-PIN SDIP	16K MASK ROM
μPD78C14G-XXX-1B	64-PIN FLAT (2.05 mm)	
μPD78C14GF-XXX	64-PIN FLAT (2.7 mm)	
μPD78C14G-XXX-37	64-PIN QUIP (Straight)	
μPD78C14G-XXX-36	64-PIN QUIP (Bent)	
μPD78C14L-XXX	68-PIN PLCC	
μPD78C14G-A-XXX-36	64-PIN QUIP (Bent)	16K MASK ROM
μPD78C14L-A-XXX	68-PIN PLCC	A-Grade, –40 to +85°C
μPD78C10ACW	64-PIN SDIP	ROM-Less
μPD78C10AGQ-36	64-PIN QUIP (Bent)	
μPD78C10AGF	64-PIN FLAT (2.7 mm)	
μPD78C10AL	68-PIN PLCC	
μPD78C11ACW-XXX	64-PIN SDIP	4K MASK ROM
μPD78C11AGQ-XXX-37	64-PIN QUIP (Straight)	
μPD78C11AGQ-XXX-36	64-PIN QUIP (Bent)	
μPD78C11AGF-XXX	64-PIN FLAT (2.7 mm)	
μPD78C11AL-XXX	68-PIN PLCC	
μPD78C12ACW-XXX	64-PIN SDIP	8K MASK ROM
μPD78C12AGQ-XXX-37	64-PIN QUIP (Straight)	
μPD78C12AGQ-XXX-36	64-PIN QUIP (Bent)	
μPD78C12AGF-XXX	64-PIN FLAT (2.7 mm)	
μPD78C12AL-XXX	68-PIN PLCC	
μPD78C14AG-XXX	64-PIN FLAT (0.8 mm pin pitch)	16K MASK ROM
μPD78CG14E	64-PIN QUIP (Bent)	16K PIGGY BACK version
μPD78CP14CW	64-PIN SDIP PLASTIC	16K OTPROM
μPD78CP14G-36	64-PIN QUIP	
μPD78CP14GF	64-PIN FLAT (2.7 mm)	
μPD78CP14L	68-PINPLCC	
μPD78CP14DW	64-PIN SDIP	16K UVPROM
μPD78CP14R	64-PIN QUIP (Bent)	

NOTE: QUIL = QUAD IN LINE, SDIP = SHRINKED DUAL IN LINE, FLAT = FLAT PACKAGE (SMD), L = PLCC

PIN CONFIGURATION
SHRINK DIP, QUIP (Bent, Straight)

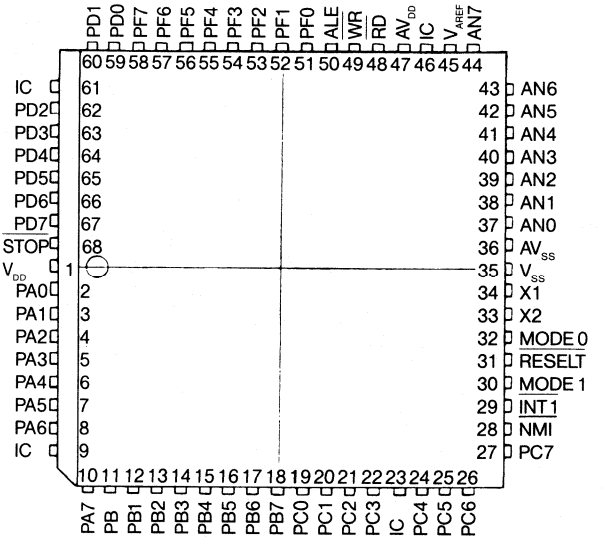


PIN CONFIGURATION
FLAT PACKAGE



3

PIN CONFIGURATION
68-PIN PLCC PACKAGE



Note: IC = keep this pin open because of internal connection (external connection prohibited)

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION	
1–8	PA_0–PA_7	Port A: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port A in input mode.	
9–16	PB_0–PB_7	Port B: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port B in input mode.	
17	PC_0	Port C: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Alternatively, Port C may be used as control lines for USART and timer, event-counter and external interrupts. Reset puts Port C in Port mode and all lines in input mode.	Transmit Data (TxD): Serial data output terminal.
18	PC_1		Receive Data (RxD): Serial data input terminal.
19	PC_2		Serial Clock ($\overline{SCK}$): Serial clock input/output terminal. When internal clock is used, the output can be selected; when an external clock is used, the input can be selected.
20	PC_3		Timer Input ((TI)/interrupt request input (INT2): Timer clock input terminal; can also be used as falling edge, maskable-interrupt input terminal and AC input zero-cross detection terminal.
21	PC_4		Timer Output (TO): This output signal is a square wave whose frequency is determined by the timer/counter.
22	PC_5		Counter Input (CI): External pulse input terminal to the timer/event counter.
23–24	PC_6, PC_7		Counter Outputs 0, 1 (CO_0–CO_1): Programmable rectangular wave output terminal based on timer/event counter.
25	$\overline{NMI}$	Falling-edge, nonmaskable interrupt ($\overline{NMI}$) input.	
26	INT1	This signal is a rising-edge, maskable interrupt input. This input is also used to make the zero-cross detection AC input.	
27	MODE1	Used as input in conjunction with MODE0 to select appropriate memory expansion mode. Also outputs M1 Signal during each opcode fetch.	
28	$\overline{RESET}$	(Input, active low), $\overline{RESET}$ initializes the μPD7811.	
29	MODE0	Used as input in conjunction with MODE1 to select appropriate memory expansion mode. Also used to output $\overline{IO}$/M.	
30–31	X_2, X_1 (crystal)	This is a crystal connection terminal for system clock oscillation. When an external clock is supplied X_1 is the input.	
32	V_{SS}	Power supply ground potential.	
33	AV_{SS}	A/D converter power supply ground potential. Sets conversion's range lower limit.	

3

PIN IDENTIFICATION (cont.)

PIN NO.	PIN SYMBOL	FUNCTION
34–41	AN_0–AN_7	Eight analog inputs to the A/D converter. AN_7–AN_4 can also be used as a digital input port for falling edge detection.
42	V_{AREF}	Reference voltage for A/D converter. Sets conversion's range upper limit.
43	AV_{CC}	Power supply voltage for A/D converter.
44	$\overline{RD}$	(Three-state output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes high during Reset.
45	$\overline{WR}$	(Three-state output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes high during Reset.
46	ALE	The strobe signal is for latching the address signal to the output from PD_7–PD_0 when accessing external expansion memory.
47–54	PF_0–PF_7	Port F: (Three-state input/output) 8-bit programmable I/O port. Each line configurable independently as an input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
55–62	DB_0–DB_7	Port D: 8-bit programmable I/O port. This byte can be designated as either input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
63	$\overline{STOP}$	Input pin for hardware stop mode
64	V_{DD}	+5V power supply.

Notes:
1 clock cycle = 1 CL = 3/f.
1 machine cycle = 3 or 4 clock cycles.
1 instruction cycle = 1 to 19 machine cycles.
f: System clock frequency (MHz).

NEW INSTRUCTIONS

In addition to the existing instruction set for μPD7801, the following new instructions are incorporated in the μPD78C10/C11/C14:

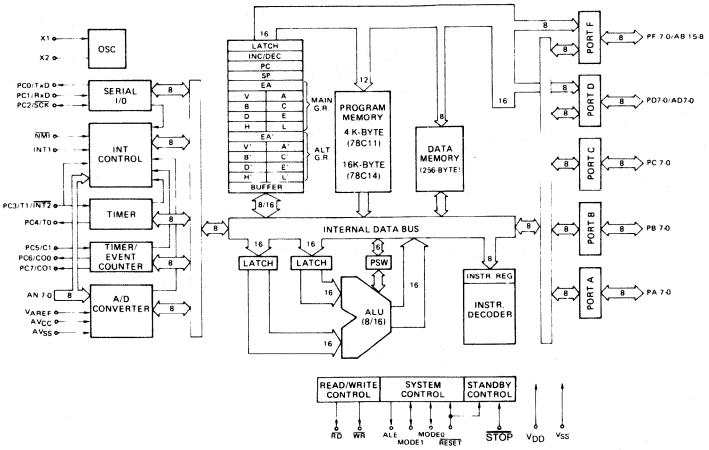
16-bit data transfer between memory and extended accumulator
16-bit data arithmetic and logical operation.

16-bit data addition and subtraction and 16-bit comparsion.
16-bit data shift and rotation
direct multiply and divide instructions.

8-bit by 8-bit division less then 8 μsec execution time.

16-bit divided by 8-bit less than 15 μsec execution
table look-up operation.
Register pair HL and DE are used as base register. Accumulator, B-register and extended accumulator are used as index register.
In addition to the 7811 instruction set, a STOP instruction is available.

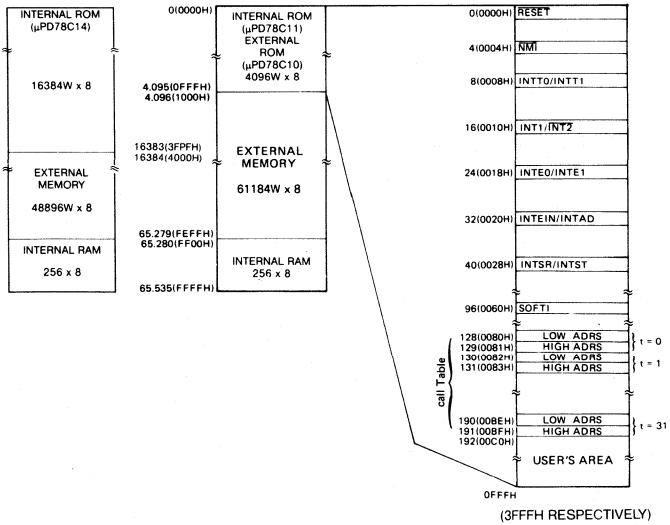
BLOCK DIAGRAM



Note: the μPD78C10 has no programmable ROM

MEMORY MAP

The μPD78C11 can directly address up to 64K-bytes of memory. Except for the on-chip ROM (0-4095) and RAM (65280-65535), any memory location can be used as ROM or RAM. The following memory map defines the 0-64K-byte memory space for the μPD78C11.



FUNCTIONAL DESCRIPTION

INPUT/OUTPUT

8 Analog Input Lines
44 Digital I/O Lines: five 8-bit ports (Port A, Port B, Port C, Port D, Port F) and 4 input lines (AN_4–AN_7)

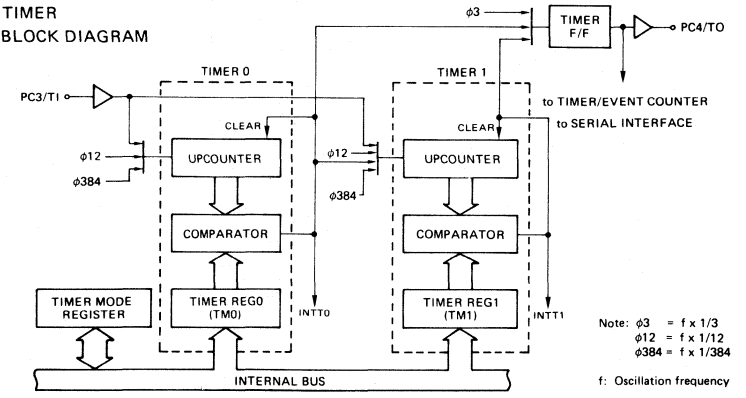
1. Analog Input Lines
   AN_0–AN_7 are configured as analog input lines for on-chip A/D converter.
2. Port Operation
   - Port A, Port B, Port C, Port F
     Each line of these ports can be individually programmed as an input or as an output. When used as I/O ports, all have latches outputs, high-impedance inputs.
   - Port D
     Port D can be programmed as a byte input or a byte output.
   - AN_4–AN_7
     The high-order analog input lines, AN_4–AN_7 can be used as digital input lines for falling edge detection.
3. Control Lines
   Under software control, each line of Port C can be configured individually to provide control lines for serial interface, timer and timer/counter, and interrupts.
4. Memory Expansion
   In addition to the single-chip operation mode the μPD78C11 has 4 memory expansion modes. Under software control, Port D can provide multiplexed low-order address and data bus and Port F can provide high-order address bus. The relation between memory expansion modes and the pin configurations of Port D and Port F is shown in the table that follows.

MEMORY EXPANSION		PORT CONFIGURATION
None	Port D Port F	I/O Port I/O Port
256 Bytes	Port D Port F	Multiplexed Address/Data Bus I/O Port
4K Bytes	Port D Port F_0–F_3 Port F_4–F_7	Multiplexed Address/Data Bus Address Bus I/O Port
16K Bytes	Port D Port F_0–F_5 Port F_6–F_7	Multiplexed/Data Bus Address Bus I/O Port
60K Bytes	Port D Port F	Multiplexed Address/Data Bus Address Bus

TIMERS

The timer/event counter consists of two 8-bit timers. The timers may be programmed independently or may be cascaded and used as a 16-bit timer. The timer can be set by software to increment at intervals of 4 machine cycles (1μs at 12MHz operation) or 128 machine cycles (32μs at 12MHz), or to increment on receipt of a pulse at TI.

TIMER
BLOCK DIAGRAM



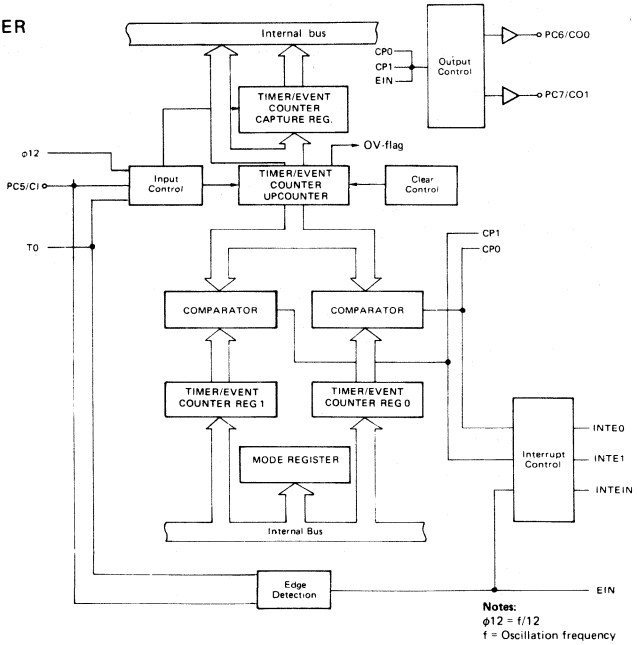
FUNCTIONAL DESCRIPTION (CONT.)

TIMER/EVENT COUNTER

The 16-bit Multifunctional timer/event counter can be used for the following operations:

- Interval timer
- External event counter
- Frequency measurement
- Pulse width measurement
- Programmable square-wave output
- Single pulse generation

TIMER/EVENT COUNTER BLOCK DIAGRAM



ANALOG/DIGITAL CONVERTER

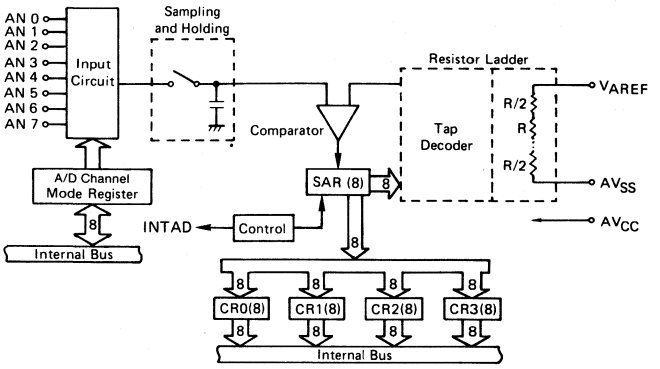
8 Input Channels
4 Conversion Result Registers
2 Powerful Operation Modes
  Auto Scan Mode
  Channel Select Mode
Successive Approximation Technique

Absolute Accuracy *	(±0.6% of FSR)
Conversion Range	0 ~ 5V
Conversion Time	50 μs
Interrupt Generation	

The μPD78C10/C11 features an 8-bit, high speed, high accuracy A/D converter. The A/D converter comprises a 256-Resistor Ladder and Successive Approximation Register (SAR). There are four conversion result registers (CR_0–CR_3). The 8-channel analog input may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR_0–CR_3. In the scan mode, the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers.

* Absolute accuracy depends on VA_{REF} used and temperature range. Please refer to device specification.

A/D CONVERTER BLOCK DIAGRAM

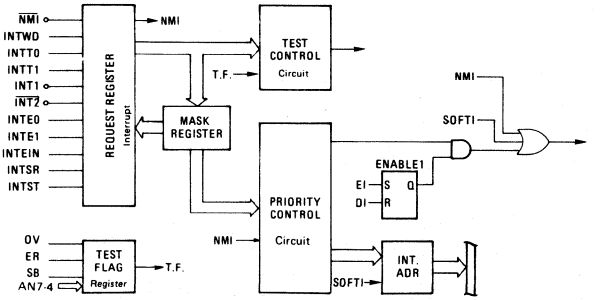


INTERRUPT STRUCTURE

There are 11 interrupt sources. Three are external interrupts and 8 are internal. These 11 interrupt sources are divided into 6 priority levels as shown in the table below.

INTERRUPT REQUEST	INTERRUPT VECTOR	TYPE OF INTERRUPT		IN/EXT
IRQ0	4	NMI	(Non-maskable interrupt)	External
IRQ1	8	INTT0 INTT1	(Coincidence signal from timer 0) (Coincidence signal from timer 1)	Internal
IRQ2	16	INT1 INT2	(Maskable intrrupt) (Maskable interrupr)	External
IRQ3	24	INTE0 INTE1	(Coincidence signal from timer/ event counter) Coincidence signal from timer/ event counter)	Internal
IRQ4	32	INTEIN INTAD	(Falling signal of C1 and T0 counter) (A/D converter interrupt)	In/External
IRQ5	40	INTSR INST	(Serial receive interrupt) (Serial send interrupt)	Internal

INTERRUPT CONTROL BLOCK DIAGRAM



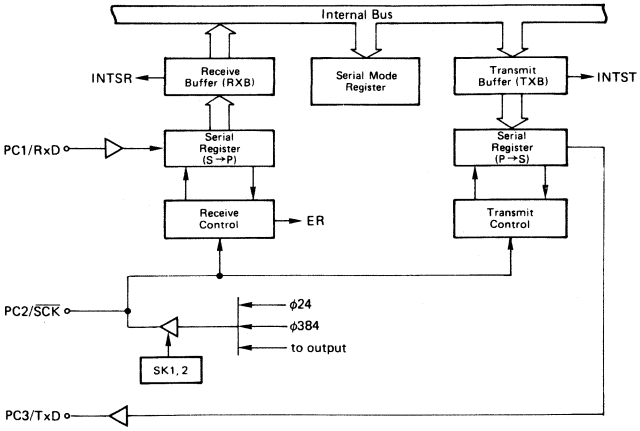
STANDBY FUNCTION

The μPD78C10/C11 offers a standby function that allows the user to save up to 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On power up the μPD78C11 checks whether recovery was made from standby mode or from cold start.

UNIVERSAL SERIAL INTERFACE

The serial interface can operate in any of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first for ease of communication with certain peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception. In the search mode, data are transferred one bit at a time from serial register to receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from serial register to transmit buffer occurs 8 bits at a time.

UNIVERSAL SERIAL INTERFACE BLOCK DIAGRAM



Note: $\phi 24 = \frac{1}{24}$ f: oscillation frequency (MHz)

$\phi 384 = \frac{1}{384}$

ZERO-CROSSING DETECTOR

The INT1 and $\overline{INT2}$ terminals (used also as TI and PC_3) can be used to detect the zero-crossing point of slow moving AC signals. When driven directly, these pins respond as a normal digital input.

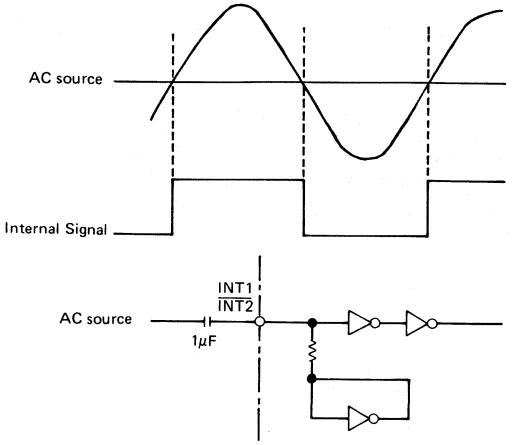
To utilize the zero-cross detection mode, an AC signal of approximately 1 – 1.8V peak-to-peak magnitude and a maximum frequency of 1kHz is coupled through an external capacitor to these pins.

For the INT1 pin, the internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one and INT1 interrupt is generated.

For the $\overline{INT2}$ pin, the state is sensed as a one until the falling edge crosses the DC average level, when it becomes a zero and $\overline{INT2}$ interrupt is generated.

The zero-cross detection capability allows the user to make the 50–60Hz power signal the basis for system timing and to control voltage phase sensitive devices.

In addition to the 7810/11 a register is implemented (ZCM = Zero Cross Mode Register) to allow to switch of the internal zero-cross detection circuit to reduce power consumption, especially during standby.



ZERO-CROSSING
DETECTION CIRCUIT

MODE0/MODE1-TERMINALS

The logic level applied to M0/M1-Terminals determines the memory map of μPD78C10/C11/C14 and the use of Port D/F as multiplexed Address/Data Bus.

M0	M1	MEMORY	ADDRESSES	LOCATION
0	1	4K	0 . . . . . FFFH	internal*
0	0	4K	0 . . . . . FFFH	external
0	1	16K	0 . . . . . 3FFFH	external
1	0	64K	0 . . . . . FEFFH	external

* MO, M1 = 0,1 realizes the ROM version (access of internal ROM), all others represent access of external memory only. In case external memory is used in addition to internal, memory mapping register has to be programmed then (see below).

MEMORY EXPANDES MODES	MEMORY MAPPING REGISTER			NUMBER OF I/O LINES
	MM2	MM1	MM0	
Port Mode	0	0	X	44
256 Expanded	0	1	0	36
4K Expanded	1	0	0	32
16K Expanded	1	1	0	30
48K/60K Expanded	1	1	1	28

(using μPD7811)

Difference Between μPD78C11 and μPD7811

Item \ Product		μPD78C11	μPD7811
No. of instructions		159 (STOP instruction was added.)	158
No. of special registers		28 (ZCM register was added.)	27
Standby function		HALT MODE, software STOP mode, hardware STOP mode. In addition, in the software/hardware STOP mode, the internal RAM data (256 bytes) are retained at the power supply voltage as low as 2.5V	32 bytes of the 256-byte internal RAM data are retained at power supply voltage as low as 3.2V.
Control of zerocross detection circuit's selfbias		Available by setting the ZCM register	Not available
No. of states of the HLT instruction		12	11
Device construction		CMOS	NMOS
Power consumption	Operating	75mW TYP.	750mW TYP.
	Standby	5μW TYP.	4.8mW TYP.
Pin configuration		V_{DD} : Pin 64 $\overline{STOP}$: Pin 63	V_{CC}: Pin 64 V_{DD}: Pin 63

3

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH ON CHIP A/D CONVERTER

DESCRIPTION

The NEC μPD78C17/C18/CP18 are CMOS derivatives of the μPD7810/11.
The NEC μPD78C17/C18/CP18 are high-performance single-chip microcomputers integrating sophisticated on-chip peripheral functionality normally provided by external components.
The devices's internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make μPD78C17/C18/CP18 appropiate for data processing as well as control applications. The device integrates as 16-bit ALU, 32K-ROM, 1K-byte RAM with an 8-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a UART and two zerocross detect inputs on a single die, to direct the device into fast, high-end processing applications involving analog signal interface and processing.
The μPD78C18 is the mask-ROM high volume production device embedded with customer program.
The μPD78C17 is a ROM-less version for prototyping and small volume production. For final evaluation the μPD78CP18 (OTP version) is available.

FEATURES

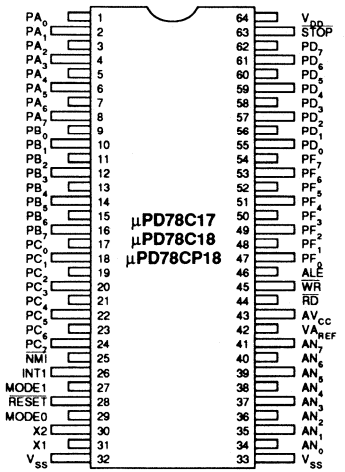
- Powerful Instruction Set including 16-bit Multiply and Divide, 159 instructions
- High-Speed 1μsec Cycle Time-12MHz Operation
- On-Chip 32-K-Byte ROM (78C18), 1K-Byte RAM
- 44 I/O Lines
- Expandable Memory up to 64K-Bytes (32K intern + 32K extern)
- On-Chip 8-Bit A/D Converter- Input Channels
- Multi-Functional 16-Bit Timer/Counter
- Two Programmable 8-Bit Timers
- Full-Duplex Serial Communication Interface, synchronous and asynchronous
- Zero-Cross Detection Capability
- Vectored Interrupts, 3 external/8 internal
- Low Power Standby Operation
- 8085A Bus Compatible
- Single Power Supply +5V, CMOS Technology
- Available in 64 Pin/68 Pin Packages (QUIP, FLAT, SHRINK DIP, LCC)
- Standby functions
- On-chip clock generator
- 64K-Byte total memory address range

ORDERING INFORMATION

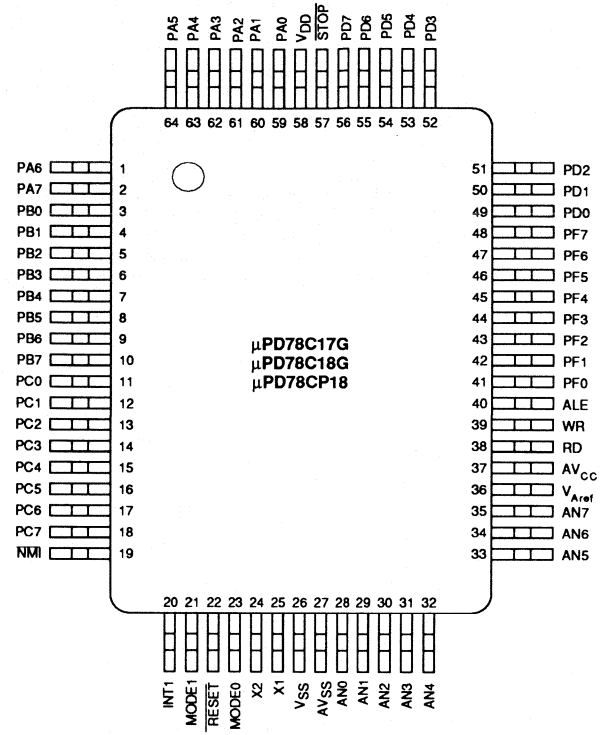
PART NUMBER	PACKAGE TYPE	ROM
μPD78C17CW	64-PIN SDIP	ROM-Less
μPD78C17GF	64-PIN FLAT (2.7 mm)	
μPD78C17G-36	64-PIN QUIP (Bent)	
μPD78C18CW-XXX	64-PIN SDIP	32K MASK ROM
μPD78C18GF-XXX	64-PIN FLAT (2.7 mm)	
μPD78C18GQ-XXX-36	64-PIN QUIP (Bent)	
μPD78CP18CW	64-PIN SDIP	32K OTPROM
μPD78CP18G-36	64-PIN QUIP (Bent)	
μPD78CP18GF	64-PIN FLAT (2.7 mm)	
μPD78CP18	68-PIN LCC PACKAGE	32K UVPROM

NOTE: QUIP = QUAD IN LINE, SDIP = SCHRINKED DUAL IN LINE,
FLAT = FLAT PACKAGE (SMD), L = PLCC

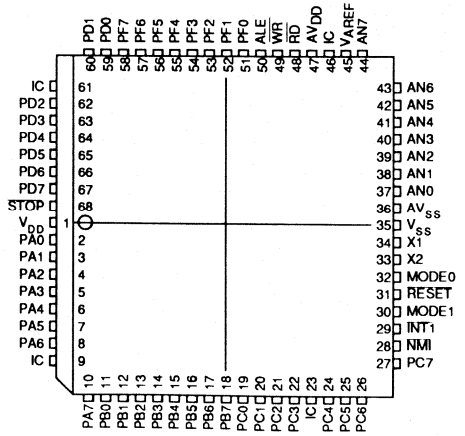
PIN CONFIGURATION
SHRINK DIP, QUIP (Bent, Straight)



PIN CONFIGURATION
FLAT PACKAGE



PIN CONFIGURATION
68-PIN LCC PACKAGE



Note: IC = keep this pin open because of internal connection (external connection prohibited)

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION	
1-8	PA_0-PA_7	Port A: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port A in input mode.	
9-16	PB_0-PB_7	Port B: (three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port B in input mode.	
17	PC_0	Port C: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Alternatively, Port C may be used as control lines for USART and timer, event-counter and external interrupts. Reset puts Port C in Port mode and all lines in input mode.	Transmit Data (Tx D): Serial data output terminal.
18	PC_1		Receive Data (R x D): Serial data input terminal.
19	PC_2		Serial Clock (SCK): Serial clock input/output terminal. When internal clock is used, the output can be selected; when an external clock is used, the input can be selected.
20	PC_3		Timer Input (TI)/interrupt request input (INT2): Timer clock input terminal; can also be used as falling edge, maskable-interrupt input terminal and AC input zero-cross detection terminal.
21	PC_4		Timer Output (TO): This output signal is a square wave whose frequency is determined by the timer/counter.
22	PC_5		Counter Input (CI): External pulse input terminal to the timer/event counter.
23-24	PC_6, PC_7		Counter Outputs 0, 1 (CO_0-CO_1): Programmable rectangular wave output terminal based on timer/event counter.
25	NMI	Falling-edge, nonmaskable interrupt (NMI) input.	
26	INT1	This signal is a rising-edge, maskable interrupt input. This is also used to make the zero-cross detection AC input.	
27	MODE1	Used as input in conjunction with MODE0 to select appropriate memory expansion mode. Also outputs M1 Signal during each opcode fetch.	
28	RESET	(Input, active low), RESET initializes the μPD7811.	
29	MODE0	Used as input in conjunction with MODE1 to select appropriate memory expansion mode. Also used to output IO/M.	
30-31	X_2, X_1 (crystal)	This is a crystal connection terminal for system clock oscillation. When an external clock is supplied X_1 is the input.	
32	V_{SS}	Power supply ground potential.	
33	AV_{SS}	A/D converter power supply ground potential. Sets conversion's range lower limit.	
34-41	AN_0-AN_7	Eight analog inputs to the A/D converter. AN_7-AN_4 can also be used as a digital input port for falling edge detection.	
42	V_{AREF}	Reference voltage for A/D converter. Sets conversion's range upper limit.	
43	AV_{CC}	Power supply voltage for A/D converter.	
44	RD	(Three-state output, activ low) RD is used as a strobe to gate data from external devices onto the data bus. RD goes high during Reset.	
45	WR	(Three-state output, active low) WR, when active, indicates that the the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. WR goes high during Reset.	
46	ALE	The strobe signal is for latching the address signal to the output from PD_7-PD_0 when accessing external expansion memory.	
47-54	PF_0-PF_7	Port F: (Three-state input/output) 8-bit programmable I/O port. Each line configurable independently as an input or output.	Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
55-62	DB_0-DB_7	Port D: 8-bit programmable I/O port. This line can be designated as either input or output.	Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
63	STOP	Input pin for hardware stop mode.	
64	V_{DD}	+5V power supply.	

Notes:
1 cklock cycle = 1CL = 3/F.
1 machine cycle = 3 or 4 clock cycles.
1 instruction cycle = 1 to 9 machine cycles.
f: System clock frequency (MHz).

NEW INSTRUCTIONS

In addition to the existing instruction set for μPD7801, the following new instruction are incorporated in the μPD78C17/C18/CP18.

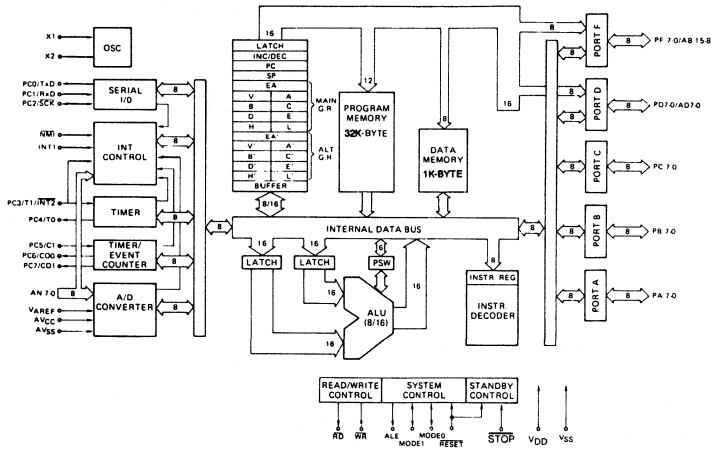
16-bit data transfer between memory and extended accumulator
16-bit data arithmetic and logical operation.

16-bit data addition and subtraction and 16-bit comparision.
16-bit data shift and rotation
direct multiply and divide instructions.

8-bit by 8-bit division less then 8 μsec execution time.

16-bit divided by 8-bit less than 15μsec execution
table look-up operation.
Register pair HL and DE are used as base register Accumulator, B-register and extended accumulator are used as index register.
In addition to the 7811 instruction set, a STOP instruction is available.

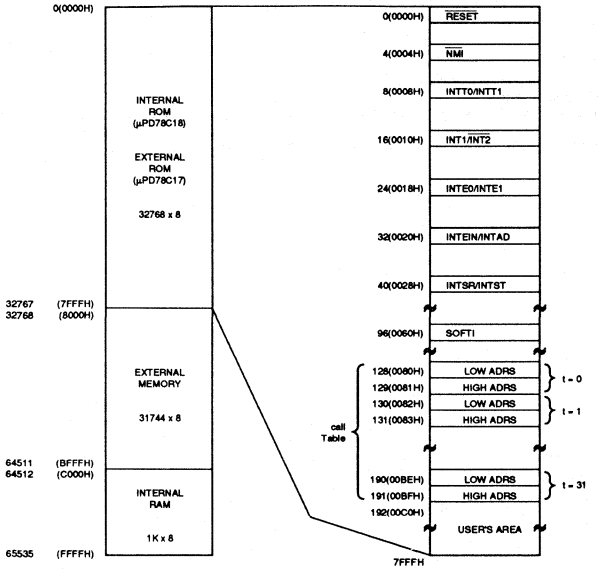
BLOCK DIAGRAM



Note: the μPD78C17 has no programmable ROM

MEMORY MAP

The μPD78C18 can directly address up to 64K-bytes of memory. Except for the on-chip ROM (0–32760) and RAM (64512–65535), any memory location can be used as ROM or RAM.
The following memory map defines the 0-64K-byte memory space for the μPD78C18.



FUNCTIONAL DESCRIPTION

8 Analog Input Lines
44 Digital I/O Lines: five 8-bit ports (Port A, Port B, Port C, Port D, Port F) and 4 input lines (AN_4–AN_7)

INPUT/OUTPUT

1. Analog Input Lines
   AN_0–AN_7 are configured as analog input lines for on-chip A/D converter.

2. Port Operation
   — Port A, Port B, Port C, Port F
   Each line of these ports can be individually programmed as an input or as an output.
   When used as I/O ports, all have latches outputs, high-impedance inputs.
   — Port D
   Port D can be programmed as a byte input or a byte output.
   — AN_4–AN_7
   The high-order analog input lines, AN_4–AN_7 can be used as digital input lines for falling edge detection.

3. Control Lines
   Under software control, each line of Port C can be configured individually to provide control lines for serial interface, timer and timer/counter, and interrupts.

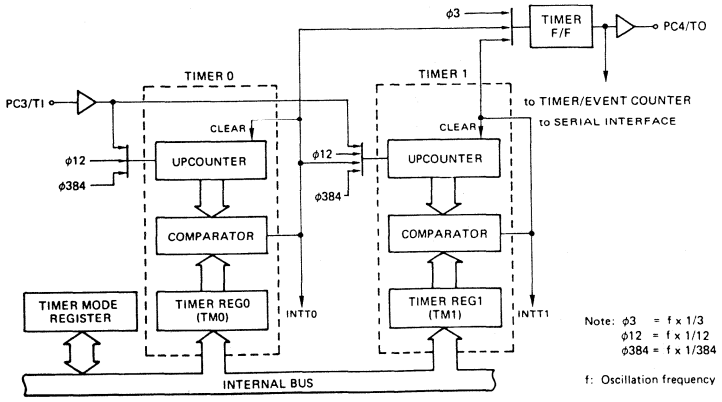
4. Memory Expansion
   In addition to the single-chip operation mode the μPD78C18 has 4 memory expansion modes. Under software control, Port D can provide multiplexed low-order address and data bus and Port F can provide high-order address bus. The relation between memory expansion modes and the pin configurations of Port D and Port F is shown in the table that follows.

MEMORY EXPANSION		PORT CONFIGURATION
None	Port D Port F	I/O Port I/O Port
256 Bytes	Port D Port F	Multiplexed Address/Data Bus I/O Port
4K Bytes	Port D Port F_0-F_3 Port F_4-F_7	Multiplexed Address/data Bus Address Bus I/O Port
16K Bytes	Port D Port F_0-F_5 Port F_6-F_7	Multiplexed/Data Bus Address Bus I/O Port
60K Bytes	Port D Port F	Multiplexed Address/Data Bus Address Bus

TIMERS

The timer/event counter consists of two 8-bit timers. The timers may be programmed independently or may be cascaded and used as a 16-bit timer. The timer can be set by software to increment at intervals of 4 machine cycles (1 μs at 12MHz operation) or 128 machine cycles (32 μs at 12MHz), or to increment on receipt of a pulse at TI.

TIMER BLOCK DIAGRAM

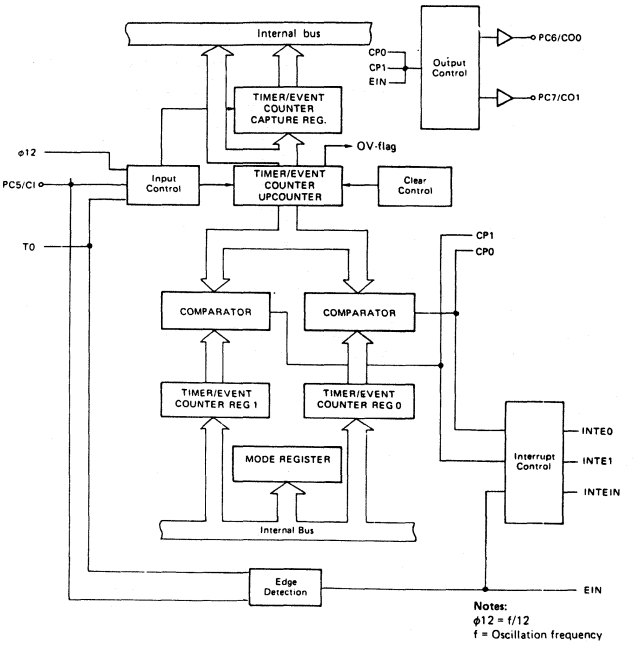


TIMER/EVENT COUNTER

The 16-bit Multifunctional timer/event counter can be used for the following operations:

Interval timer
External event counter
Frequency measurement
Pulse width measurement
Programmable square-wave output
Single pulse generation

TIMER/EVENT COUNTER BLOCK DIAGRAM



ANALOG/DIGITAL CONVERTER

8 Input Channels
4 Conversion Result Registers
2 Powerful Operation modes
  Auto Scan Mode
  Channel Select Mode
Successive Approximation Technique

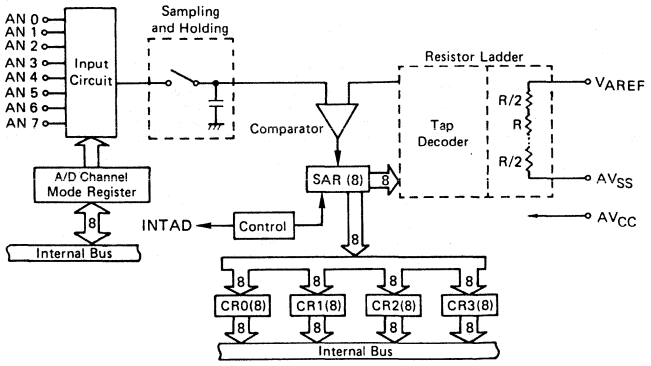
Absolute Accuracy *	(±0.6% of FSR)
Conversion Range	0 ~ 5V
Conversion Time	50μs

Interrupt Generation

The μPD78C17/C18 features an 8-bit, high speed, high accuracy A/D converter. The A/D converter comprises a 256-Resistor Ladder and Successive Approximation Register (SAR).
There are four conversion result registers (CR_0–CR_3). The 8-channel analog inpput may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR_0–CR_3. In the scan mode, the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers.

* Absolute accuracy depends on VA_{REF} used and temperature range. Please refer to device specification.

A/D CONVERTER BLOCK DIAGRAM

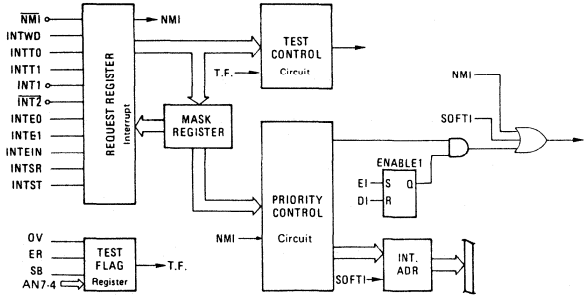


INTERRUPT STRUCTURE

These are 11 interrupt sources. Three are external interrupts and 8 are internal. These 11 interrupt sources are divided into 6 priority levels as shown in the table below.

INTERRUPT REQUEST	INTERRUPT VECTOR	TYPE OF INTERRUPT	IN/EXT
IRQ0	4	NMI (Non-maskable interupt)	External
IRQ1	8	INTT0 (Coincidence signal from timer 0) INTT1 (Coincidence signal from timer 1)	Internal
IRQ2	16	INT1 (Maskable interrupt) INT2 (Maskable interrupt)	External
IRQ3	24	INTE0 (Coincidence signal from timer/event counter) INTE1 (Coincidence signal from timer/event counter)	Internal
IRQ4	32	INTEIN (Falling signal of C1 and T0 counter) INTAD (A/D converter interrupt)	In/External
IRQ5	40	INTSR (Serial receive interrupt) INST (Serial send interrupt)	Internal

INTERRUPT CONTROL BLOCK DIAGRAM



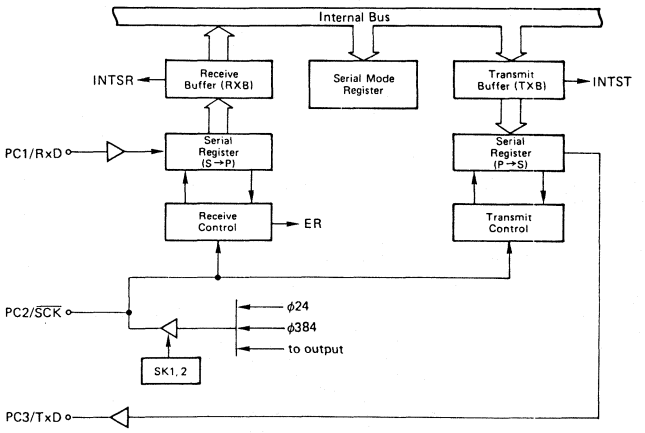
STANDBY FUNCTION

The μPD78C17/C18 offers a standby function that allows the user to save up to 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On power up the μPD78C18 checks whether recovery was made from standby mode or from cold start.

UNIVERSAL SERIAL INTERFACE

The serial interface can operate in any of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first for ease of communication with certain peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception. In the search mode, data are transferred one bit at a time from serial register to receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from serial register to transmit buffer occurs 8 bits at a time.

UNIVERSAL SERIAL INTERFACE BLOCK DIAGRAM



Note: $\phi 24 = \frac{f}{24}$

$\phi 384 = \frac{f}{384}$

f: oscillation frequency (MHz)

ZERO-CROSSING DETECTOR

The INT1 and $\overline{INT2}$ terminals (used also as TI and PC_3) can be used to detect the zero-crossing point of slow moving AC signals. When driven directly, these pins respond as normal digital input.

To utilize the zero-cross detection mode, an AC signal of approximately 1 - 1.8V peak-to-peak magnitude and a maximum frequency of 1kHz is coupled through an external capacitor to these pins.

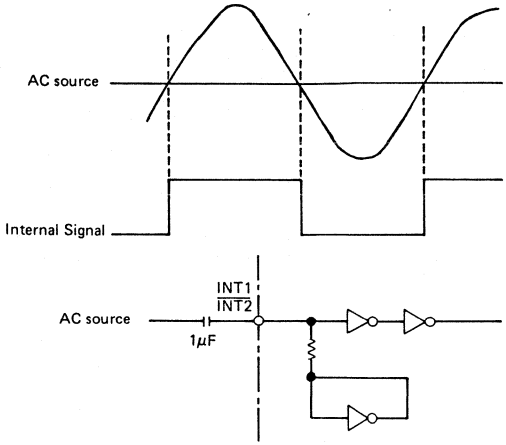
For the INT1 pin, the internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one and INT1 interrupt is generated.

For the $\overline{INT2}$ pin, the state is sensed as a one until the falling edge crosses the DC average level, when it becomes a zero an $\overline{INT2}$ interrupt is generated.

The zero-cross detection capability allows the user to make the 50-60Hz power signal the basis of system timing and to control voltage phase sensitive devices.

A register is implemented (ZCM = Zero Cross Mode Register) to allow to switch of the internal zero-cross detection circuit to reduce power consumption, especially during standby.

ZERO-CROSSING DETECTION CIRCUIT



MODE0/MODE1-TERMINALS

The logic level applied to M0/M1-Terminals determines the memory map of μPD78C17/C18 and the use of Port D/F as multiplexed Address/Data Bus.

M0	M1	MEMORY	ADDRESSES	LOCATION
0	1	4K	0 ..... FFFH	internal*
0	0	4K	0 ..... FFFH	external
0	1	16K	0 ..... 3FFFH	external
1	0	64K	0 ..... FEFFH	external

* M0, M1 = 0,1 realizes the ROM version (access of internal ROM), all others represent access of external memory only. In case external memory is used in addition to internal, memory mapping register has to be programmed then (see below).

MEMORY EXPANDES MODES	MEMORY MAPPING REGISTER			NUMBER OF I/O LINES
	MM2	MM1	MM0	
Port Mode	0	0	X	44
256 Expanded	0	1	0	36
4K Expanded	1	0	0	32
16K Expanded	1	1	0	30
48K/60K Expanded	1	1	1	28

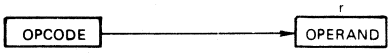
(using μPD7811)

ADDRESSING MODES AND INSTRUCTION SET μCOM87AD (μPD7810/11/PG11/10H/11H/C10/C11/C14/C17/C18 C10A/C11A/C12A/C14A)

ADDRESS MODES

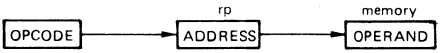
Register Addressing
Register Indirect Addressing
Auto-Increment Addressing
Auto-Decrement Addressing
Working Register Addressing
Direct Addressing
Immediate Addressing
Immediate Extended Addressing
Relative Addressing
Base Addressing
Base Index Addressing
Double Auto Increment Addressing

Register Addressing



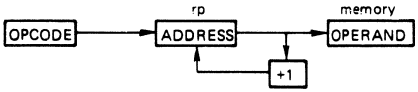
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



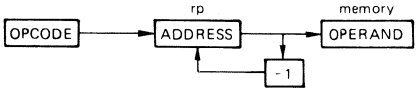
The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are using this address mode.

Auto-Increment Addressing

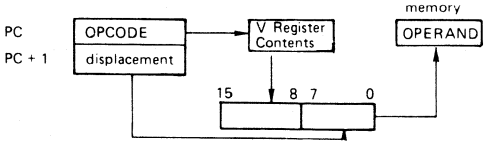


The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

Auto Decrement Addressing

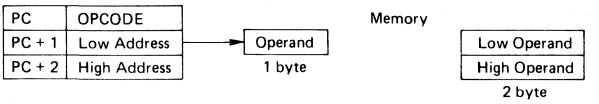


Working Register Addressing



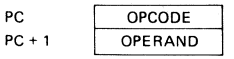
The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix are using this address mode.

Direct Addressing

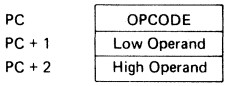


The two bytes following the opcode specify an address of a location containing the operand.

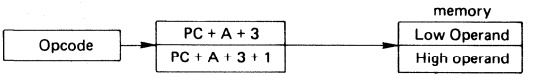
Immediate Addressing



Immediate Extended Addressing

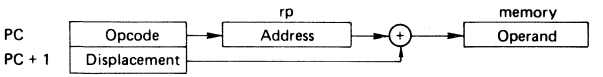


Relative Addressing



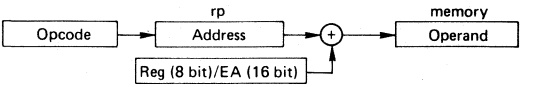
This addressing mode is used by the "Table"-command. It transfers the contents of 2 memory cells – addressed relatively to PC via the Accu A – into BC register-pair.
Application: Table look-up

Base-Addressing



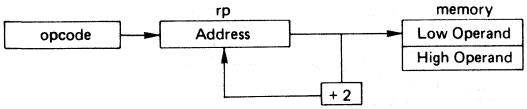
Register Pair DE or HL used as base pointer to the memory; immediate data (8 bit) or displacement added to the base.

Base-Index-Addressing



Register pair DE or HL used as base pointers to the memory; Register (8 bit) or Extended Accumulator (EA) as displacement added to the base.

Double auto increment



The opcode specifies the register pair which contains the memory address of the operand (16 bit). The contents of the register pair is automatically incremented by two to point to a new 16-bit operand.

μCOM 87 AD Instructionset

Operand Expression/Description

EXPRESSION	DESCRIPTION
r r1 r2	V, A, B, C, D, E, H, L EAH, EAL, B, C, D, E, H, L A, B, C
sr sr1 sr2 sr3 sr4	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TXB, TMO, TM1, ZCM (CMOS ONLY) PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM, RXB, CR0, CR1, CR2, CR3 PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM ETM0, ETM1 ECNT, ECPT
rp rp1 rp2 rp3	SP, B, D, H V, B, D, H, EA SP, B, D, H, EA B, D, H
rpa rpa1 rpa2 rpa3	B, D, H, D+, H+, D−, H− B, D, H B, D, H, D+, H+, D−, H−, D+byte, H+A, H+B, H+EA, H+byte D, H, D++, H++, D+byte, H+A, H+B, H+EA, H+byte
wa	8 bit immediate data
word byte bit	16 bit immediate data 8 bit immediate data 3 bit immediate data
f	CY, HC, Z
if	FNMI, FTO, FT1, F1, F2, FEO, FE1, FEIN, FAD, FSR, FST ER, OV, AN4, AN5, AN6, AN7, SB

Note 1

1. sr ~ sr4 (special register)

PA	:	PORT A	ECNT	:	TIMER/EVENT COUNTER UPCOUNTER
PB	:	PORT B			
PC	:	PORT C	ECPT	:	TIMER/EVENT COUNTER CAPTURE
PD	:	PORT D			
PF	:	PORT F	ETMM	:	TIMER/EVENT COUNTER MODE
MA	:	MODE A			
MB	:	MODE B	EOM	:	TIMER/EVENT COUNTER OUTPUT MODE
MC	:	MODE C			
MCC	:	MODE CONTROL C	ANM	:	A/D CHANNEL MODE
MF	:	MODE F	CRO	:	A/D CONVERSION RESULTO ~ 3
MM	:	MEMORY MAPPING	~		
TMO	:	TIMER REGO	CR3		
TM1	:	TIMER REG1	TXB	:	Tx BUFFER
TMM	:	TIMER MODE	RXB	:	Rx BUFFER
ETM0	:	TIMER/EVENT COUNTER REG0	SMH	:	SERIAL MODE High
			SML	:	SERIAL MODE Low
ETM1	:	TIMER/EVENT COUNTER REG1	MKH	:	MASK High
			MKL	:	MASK Low
ZCM	:	ZERO CROSS MODE (CMOS ONLY)			

2. rp ~ rp3 (register pair)

SP	:	STACK POINTER
B	:	BC
D	:	DE
H	:	HL
V	:	VA
EA	:	EXTENDED ACCUMULATOR

3. rpa ~ rpa3 (rp addressing)

B	:	(BC)
D	:	(DE)
H	:	(HL)
D+	:	$(DE)^{+}$
H+	:	$(HL)^{+}$
D−	:	$(DE)^{-}$
H−	:	$(HL)^{-}$
D++	:	$(DE)^{++}$
H++	:	$(HL)^{++}$
D+byte	:	(DE+byte)
H+A	:	(HL+A)
H+B	:	(HL+B)
H+EA	:	(HL+EA)
H+byte	:	(HL+byte)

4. f (flag)

CY	:	CARRY
HC	:	HALF CARRY
Z	:	ZERO

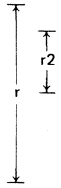
5. if (Interrupt flag)

FNMI	:	INTFNMI
FT0	:	INTFT0
FT1	:	INTFT1
F1	:	INTF1
F2	:	INTF2
FE0	:	INTFE0
FE1	:	INTFE1
FEIN	:	INTFEIN
FAD	:	INTFAD
FSR	:	INTFSR
FST	:	INTFST
ER	:	ERROR
OV	:	OVERFLOW
AN4	:	ANALOG INPUT 4~7
~		
AN7	:	
SB	:	STANDBY

Description of Instruction Code Symbols

r

R_2	R_1	R_0	reg
0	0	0	V
0	0	1	A
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L

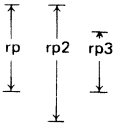


r1

T_2	T_1	T_0	reg
0	0	0	EAH
0	0	1	EAL
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L

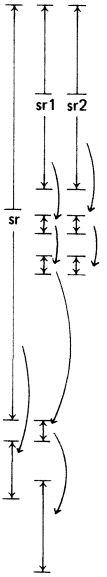
rp

P_2	P_1	P_0	reg-pair
0	0	0	SP
0	0	1	BC
0	1	0	DE
0	1	1	HL
1	0	0	EA



sr

S_5	S_4	S_3	S_2	S_1	S_0	Special-reg
0	0	0	0	0	0	PA
0	0	0	0	0	1	PB
0	0	0	0	1	0	PC
0	0	0	0	1	1	PD
0	0	0	1	0	1	PF
0	0	0	1	1	0	MKH
0	0	0	1	1	1	MKL
0	0	1	0	0	0	ANM
0	0	1	0	0	1	SMH
0	0	1	0	1	0	SML
0	0	1	0	1	1	EOM
0	0	1	1	0	0	ETMM
0	0	1	1	0	1	TMM
0	1	0	0	0	0	MM
0	1	0	0	0	1	MCC
0	1	0	0	1	0	MA
0	1	0	0	1	1	MB
0	1	0	1	0	0	MC
0	1	0	1	1	1	MF
0	1	1	0	0	0	TXB
0	1	1	0	0	1	RXB
0	1	1	0	1	0	TM0
0	1	1	0	1	1	TM1
1	0	1	0	0	0	ZCM (CMOS)
1	0	0	0	0	0	CR0
1	0	0	0	0	1	CR1
1	0	0	0	1	0	CR2
1	0	0	0	1	1	CR3

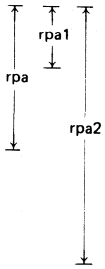


rp1

Q_2	Q_1	Q_0	reg-pair
0	0	0	VA
0	0	1	BC
0	1	0	DE
0	1	1	HL
1	0	0	EA

rpa

A_3	A_2	A_1	A_0	addressing
0	0	0	0	–
0	0	0	1	(BC)
0	0	1	0	(DE)
0	0	1	1	(HL)
0	1	0	0	$(DC)^+$
0	1	0	1	$(HL)^+$
0	1	1	0	$(DC)^-$
0	1	1	1	$(HL)^-$
1	0	1	1	(DE+byte)
1	1	0	0	(HL+A)
1	1	0	1	(HL+B)
1	1	1	0	(HL+EA)
1	1	1	1	(HL+byte)



rpa3

C_3	C_2	C_1	C_0	addressing
0	0	0	0	(DE)
0	0	0	1	(HL)
0	0	1	0	$(DE)^{++}$
0	0	1	1	$(HL)^{++}$
1	0	1	1	(DE+byte)
1	1	0	0	(HL+A)
1	1	0	1	(HL+B)
1	1	1	0	(HL+EA)
1	1	1	1	(HL+byte)

sr3

U_0	Special-reg
0	ETM0
1	ETM1

sr4

V_0	Special-reg
0	ECNT
1	ECPT

3

List of Mode Registers

MODE REGISTER	READ/WRITE	FUNCTION
MA register (Mode A)	W	An 8 bit register for designating the input/output of the port A in units of bit.
MB register (Mode B)	W	An 8 bit register for designating the input/output of the port B in units of bit.
MCC register (Mode Control C)	W	An 8 bit register for designating the port/control mode of the port C in units of bit.
MC register (Mode C)	W	An 8 bit register for designating the input/output of the port C in units of bit.
MM register (Memory Mapping)	W	A 4 bit register for designating the port/expansion mode od port D and port F.
MF register (Mode F)	W	An 8 bit register for designating the input of port F in units of bit.
TMM register (Timer Mode Reg.)	R/W	An 8 bit register for designating the operation mode of timer.
ETMM register (Timer/Event Counter Mode Reg.)	W	An 8 bit for designating the operation mode of timer/event counter.
EOM register (Timer/Event Counter Output Mode Reg.)	R/W	An 8 bit register for controlling the ouput level of CO0, CO1.
SMH register	R/W	7 bit and 8 bit registers for designating the operation mode of serial interface.
SML	W	
ANM register (A/D Channel Mode Reg.)	R/W	An 5 bit register for designating the operation mode of A/D converter and for indicating the input channel during A/D conversion.
ZCM register (Zero Cross Mode Reg.) CMOS only	W	A 2 bit register for switching on/off the internal zero cross detection circuit.

f

F_2	F_1	F_0	INTF
0	0	0	–
0	1	0	CY
0	1	1	HC
1	0	0	Z

if

I_4	I_3	I_2	I_1	I_0	INTF
0	0	0	0	0	INTENMI
0	0	0	0	1	INTFT0
0	0	0	1	0	INTFT1
0	0	0	1	1	INTF1
0	0	1	0	0	INTF2
0	0	1	0	1	INTFE0
0	0	1	1	0	INTFE1
0	0	1	1	1	INTFEIN
0	1	0	0	0	INTFAD
0	1	0	0	1	INTFSR
0	1	0	1	0	INTFST
0	1	0	1	1	ER
0	1	1	0	0	OV
1	0	0	0	0	AN4
1	0	0	0	1	AN5
1	0	0	1	0	AN6
1	0	0	1	1	AN7
1	0	1	0	0	SB

INSTRUCTION SET

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
8-BIT DATA TRANSFER	MOV		r1, A	0 0 0 1 1 T_2 T_1 T_0				4	r1 ← A	
			A, r1	0 0 0 0 1 T_2 T_1 T_0				4	A ← r1	
		•	sr, A	0 1 0 0 1 1 0 1	1 1 S_5 S_4 S_3 S_2 S_1 S_0			10	sr ← A	
		•	A, sr1	0 1 0 0 1 1 0 0	1 1 S_5 S_4 S_3 S_2 S_1 S_0			10	A ← sr1	
			r, word	0 1 1 1 0 0 0 0	0 1 1 0 1 R_2 R_1 R_0	Low Adrs	High Adrs	17	r ← (word)	
			word, r	0 1 1 1 0 0 0 0	0 1 1 1 1 R_2 R_1 R_0	Low Adrs	High Adrs	17	(word) ← r	
	MVI	•	r, byte	0 1 1 0 1 R_2 R_1 R_0	Data			7	r ← byte	
			sr2, byte	0 1 1 0 0 1 0 0	S_3 0 0 0 0 S_2 S_1 S_0	Data		14	sr2 ← byte	
	MVIW	•	wa, byte	0 1 1 1 0 0 0 1	Offset	Data		13	(V.wa) ← byte	
	MVIX	•	rpa1, byte	0 1 0 0 1 0 A_1 A_0	Data			10	(rpa1) ← byte	
	STAW	•	wa	0 1 1 0 0 0 1 1	Offset			10	(V.wa) ← A	
	LDAW	•	wa	0 0 0 0 0 0 0 1	Offset			10	A ← (V.wa)	
	STAX	•	rpa2	A_3 0 1 1 1 A_2 A_1 A_0	Data (*1)			7/13	(rpa2) ← A	
	LDAX	•	rpa2	A_3 0 1 0 1 A_2 A_1 A_0	Data (*1)			7/13	A ← (rpa2)	
	EXX			0 0 0 1 0 0 0 1				4	B ↔ B', C ↔ C', D ↔ D', E ↔ E', H ↔ H', L ↔ L'	
	EXA			0 0 0 1 0 0 0 0				4	V, A ↔ V', A', EA ↔ EA'	
	EXH			0 1 0 1 0 0 0 0				4	H, L ↔ H', L'	

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
16-BIT DATA TRANSFER	BLOCK		D+	0 0 1 1 0 0 0 1				13 x (C+1)	(DE)+ ← (HL)+, C ← C−1 End if borrow	
	DMOV		rp3, EA	1 0 1 1 0 1 P_1 P_0				4	$rp3_L$ ← EAL, $rp3_H$ ← EAH	
			EA, rp3	1 0 1 0 0 1 P_1 P_0				4	EAL ← $rp3_L$, EAH ← $rp3_H$	
			sr3, EA	0 1 0 0 1 0 0 0	1 1 0 1 0 0 1 U_0			14	sr3 ← EA	
			EA, sr4	↓ ↓	1 1 0 0 0 0 0 V_0			14	EA ← sr4	
	SBCD		word	0 1 1 1 0 0 0 0	0 0 0 1 1 1 1 0	Low Adrs	High Adrs	20	(word) ← C, (word+1) ← B	
	SDED		word		0 0 1 0 1 1 1 0			20	(word) ← E, (word+1) ← D	
	SHLD		word		0 0 1 1 1 1 1 0			20	(word) ← L, (word+1) ← H	
	SSPD		word		0 0 0 0 1 1 1 0			20	(word) ← SP_L, (word+1) ← SP_H	
	STEAX		rpa3	0 1 0 0 1 0 0 0	1 0 0 1 C_3 C_2 C_1 C_0	Data (*2)		14/20	(rpa3) ← EAL, (rpa3+1) ← EAH	
	LBCD		word	0 1 1 1 0 0 0 0	0 0 0 1 1 1 1 1	Low Adrs	High Adrs	20	C ← (word), B ← (word+1)	
	LDED		word		0 0 1 0 1 1 1 1			20	E ← (word), D ← (word+1)	
	LHLD		word		0 0 1 1 1 1 1 1			20	L ← (word), H ← (word+1)	
	LSPD		word		0 0 0 0 1 1 1 1			20	SP_L ← (word), SP_H ← (word+1)	
	LDEAX		rpa3	0 1 0 0 1 0 0 0	1 0 0 0 C_3 C_2 C_1 C_0	Data (*2)		14/20	EAL ← (rpa3), EAH ← (rpa3+1)	
	PUSH		rp1	1 0 1 1 0 Q_2 Q_1 Q_0				13	(SP−1) ← $rp1_H$, (SP−2) ← $rp1_L$ SP ← SP−2	
	POP		rp1	1 0 1 0 0 Q_2 Q_1 Q_0				10	$rp1_L$ ← (SP), $rp1_H$ ← (SP+1) SP ← SP+2	
	LXI	•	rp2, word	0 P_2 P_1 P_0 0 1 0 0	Low Byte	High Byte		10	rp2 ← word	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
	TABLE		01001000	10101000			17	C ← (PC+3+A) B ← (PC+3+A+1)	
8-BIT ARITHMETIC (REGISTER)	ADD	A, r	01100000	11000 R_2 R_1 R_0			8	A ← A+r	
		r, A		01000 R_2 R_1 R_0			8	r ← r+A	
	ADC	A, r		11010 R_2 R_1 R_0			8	A ← A+r+CY	
		r, A		01010 R_2 R_1 R_0			8	r ← r+A+CY	
	ADDNC	A, r		10100 R_2 R_1 R_0			8	A ← A+r	No Carry
		r, A		00100 R_2 R_1 R_0			8	r ← r+A	No Carry
	SUB	A, r		11100 R_2 R_1 R_0			8	A ← A−r	
		r, A		01100 R_2 R_1 R_0			8	r ← r−A	
	SBB	A, r		11110 R_2 R_1 R_0			8	A ← A−r−CY	
		r, A		01110 R_2 R_1 R_0			8	r ← r−A−CY	
	SUBNB	A, r		10110 R_2 R_1 R_0			8	A ← A−r	No Borrow
		r, A		00110 R_2 R_1 R_0			8	r ← r−A	No Borrow
	ANA	A, r		10001 R_2 R_1 R_0			8	A ← A ∧ r	
		r, A		00001 R_2 R_1 R_0			8	r ← r ∧ A	
	ORA	A, r		10011 R_2 R_1 R_0			8	A ← A ∨ r	
		r, A		00011 R_2 R_1 R_0			8	r ← r ∨ A	
	XRA	A, r		10010 R_2 R_1 R_0			8	A ← A ∀ r	
		r, A		00010 R_2 R_1 R_0			8	r ← r ∀ A	
	GTA	A, r		10101 R_2 R_1 R_0			8	A−r−1	No Borrow
		r, A		00101 R_2 R_1 R_0			8	r−A−1	No Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
8-BIT ARITHMETIC (REG.)	LTA	A, r	01100000	10111 R_2 R_1 R_0			8	A−r	Borrow
		r, A		00111 R_2 R_1 R_0			8	r−A	Borrow
	NEA	A, r		11101 R_2 R_1 R_0			8	A−r	No Zero
		r, A		01101 R_2 R_1 R_0			8	r−A	No Zero
	EQA	A, r		11111 R_2 R_1 R_0			8	A−r	Zero
		r, A		01111 R_2 R_1 R_0			8	r−A	Zero
	ONA	A, r		11001 R_2 R_1 R_0			8	A ∧ r	No Zero
	OFFA	A, r		11011 R_2 R_1 R_0			8	A ∧ r	Zero
8-BIT ARITHMETIC (MEMORY)	ADDX	rpa	01110000	11000 A_2 A_1 A_0			11	A ← A+ (rpa)	
	ADCX	rpa		11010 A_2 A_1 A_0			11	A ← A+ (rpa)+CY	
	ADDNCX	rpa		10100 A_2 A_1 A_0			11	A ← A+ (rpa)	No Carry
	SUBX	rpa		11100 A_2 A_1 A_0			11	A ← A− (rpa)	
	SBBX	rpa		11110 A_2 A_1 A_0			11	A ← A− (rpa)−CY	
	SUBNBX	rpa		10110 A_2 A_1 A_0			11	A ← A− (rpa)	No Borrow
	ANAX	rpa		10001 A_2 A_1 A_0			11	A ← A ∧ (rpa)	
	ORAX	rpa		10011 A_2 A_1 A_0			11	A ← A ∨ (rpa)	
	XRAX	rpa		10010 A_2 A_1 A_0			11	A ← A ∀ (rpa)	
	GTAX	rpa		10101 A_2 A_1 A_0			11	A− (rpa)−1	No Borrow
	LTAX	rpa		10111 A_2 A_1 A_0			11	A− (rpa)	Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	NEI *	A, byte	01100111	← Data →			7	A−byte	No Zero
		r, byte	01110100	01101 R_2 R_1 R_0	Data		11	r−byte	No Zero
		sr2, byte	0110 ↓	S_3 1101 S_2 S_1 S_0	↓		14	sr2−byte	No Zero
	EQI *	A, byte	01110111	← Data →			7	A−byte	Zero
		r, byte	01110100	01111 R_2 R_1 R_0	Data		11	r−byte	Zero
		sr2, byte	0110 ↓	S_3 1111 S_2 S_1 S_0	↓		14	sr2−byte	Zero
	ONI *	A, byte	01000111	← Data →			7	A ∧ byte	No Zero
		r, byte	01110100	01001 R_2 R_1 R_0	Data		11	r ∧ byte	No Zero
		sr2, byte	0110 ↓	S_3 1001 S_2 S_1 S_0	↓		14	sr2 ∧ byte	No Zero
	OFFI *	A, byte	01010111	← Data →			7	A ∧ byte	Zero
		r, byte	01110100	01011 R_2 R_1 R_0	Data		11	r ∧ byte	Zero
		sr2, byte	0110 ↓	S_3 1011 S_2 S_1 S_0	↓		14	sr2 ∧ byte	Zero
WORKING REGISTER	ADDW	wa	01110100	11000000	Offset		14	A ← A+(V.wa)	
	ADCW	wa		1101			14	A ← A+(V.wa)+CY	
	ADDNCW	wa		1010			14	A ← A+(V.wa)	No Carry
	SUBW	wa		1110			14	A ← A−(V.wa)	
	SBBW	wa		1111			14	A ← A−(V.wa)−CY	
	SUBNBW	wa		1011 ↓			14	A ← A−(V.wa)	No Borrow
	ANAW	wa		10001000			14	A ← A ∧ (V.wa)	
	ORAW	wa	↓ ↓	1001 ↓	↓		14	A ← A ∨ (V.wa)	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
WORKING REGISTER	XRAM	wa	01110100	10010000	Offset		14	A ← A ∨ (V.wa)	
	GTAW	wa		10101000			14	A−(V.wa)−1	No Borrow
	LTAW	wa		1011			14	A−(V.wa)	Borrow
	NEAW	wa		1110			14	A−(V.wa)	Nr Zero
	EQAW	wa		1111			14	A−(V.wa)	Zero
	ONAW	wa		1100			14	A ∧ (V.wa)	No Zero
	OFFAW	wa	↓ ↓	1101 ↓	↓		14	A ∧ (V.wa)	Zero
	ANIW *	wa, byte	00000101	← Offset →	Data		19	(V.wa) ← (V.wa) ∧ byte	
	ORIW *	wa, byte	0001				19	(V.wa) ← (V.wa) ∨ byte	
	GTIW *	wa, byte	0010				13	(V.wa)−byte−1	No Borrow
	LTIW *	wa, byte	0011				13	(V.wa)−byte	Borrow
	NEIW *	wa, byte	0110				13	(V.wa)−byte	No Zero
	EQIW *	wa, byte	0111				13	(V.wa)−byte	Zero
	ONIW *	wa, byte	0100				13	(V.wa) ∧ byte	No Zero
	OFFIW *	wa, byte	0101 ↓	↓	↓		13	(V.wa) ∧ byte	Zero
16-BIT ARITHMETIC	EADD	EA, r2	01110000	010000 R_1 R_0			11	EA ← EA+r2	
	DADD	EA, rp3	0100	110001 P_1 P_0			11	EA ← EA+rp3	
	DADC	EA, rp3		1101			11	EA ← EA+rp3+CY	
	DADDNC	EA, rp3		1010 ↓			11	EA ← EA+rp3	No Carry
	ESUB	EA, r2	↓ 0000	011000 R_1 R_0			11	EA ← EA−r2	

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	NEAX		rpa	01110000	11101 A_2 A_1 A_0			11	A– (rpa)	No Zero
	EQAX		rpa		11111 A_2 A_1 A_0			11	A– (rpa)	Zero
	ONAX		rpa		11001 A_2 A_1 A_0			11	A ∧ (rpa)	No Zero
	OFFAX		rpa	↓	11011 A_2 A_1 A_0			11	A ∧ (rpa)	Zero
	ADI	*	A, byte	01000110	← Data →			7	A ← A+byte	
			r, byte	01110100	01000 R_2 R_1 R_0	Data		11	r ← r+byte	
			sr2, byte	0110 ↓	S_3 1000 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	
	ACI	*	A, byte	01010110	← Data →			7	A ← A+byte+CY	
			r, byte	01110100	01010 R_2 R_1 R_0	Data		11	r ← r+byte+CY	
			sr2, byte	0110 ↓	S_3 1010 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte+CY	
	ADINC	*	A, byte	00100110	← Data →			7	A ← A+byte	No Carry
			r, byte	01110100	00100 R_2 R_1 R_0	Data		11	r ← r+byte	No Carry
			sr2, byte	0110 ↓	S_3 0100 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	No Carry
	SUI	*	A, byte	01100110	← Data →			7	A ← A–byte	
			r, byte	01110100	01100 R_2 R_1 R_0	Data		11	r ← r–byte	
			sr2, byte	0110 ↓	S_3 1100 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte	
	SBI	*	A, byte	01110110	← Data →			7	A ← A–byte–CY	
			r, byte	01110100	01110 R_2 R_1 R_0	Data		11	r ← r–byte–CY	
			sr2, byte	0110 ↓	S_3 1110 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte–CY	

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	SUINB	*	A, byte	00110110	← Data →			7	A ← A–byte	No Borrow
			r, byte	01110100	00110 R_2 R_1 R_0	Data		11	r ← r–byte	No Borrow
			sr2, byte	0110 ↓	S_3 0110 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte	No Borrow
	ANI	*	A, byte	00000111	← Data →			7	A ← A ∧ byte	
			r, byte	01110100	00001 R_2 R_1 R_0	Data		11	r ← r ∧ byte	
			sr2, byte	01100100	S_3 0001 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∧ byte	
	ORI	*	A, byte	00010111	← Data →			7	A ← A ∨ byte	
			r, byte	01110100	00011 R_2 R_1 R_0	Data		11	r ← r ∨ byte	
			sr2, byte	0110 ↓	S_3 0011 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨ byte	
	XRI	*	A, byte	00010110	← Data →			7	A ← A ∨̄ byte	
			r, byte	01110100	00010 R_2 R_1 R_0	Data		11	r ← r ∨̄ byte	
			sr2, byte	0110 ↓	S_3 0010 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨̄ byte	
	GTI	*	A, byte	00100111	← Data →			7	A–byte–1	No Borrow
			r, byte	01110100	00101 R_2 R_1 R_0	Data		11	r–byte–1	No Borrow
			sr2, byte	0110 ↓	S_3 0101 S_2 S_1 S_0	↓		14	sr2–byte–1	No Borrow
	LTI	*	A, byte	00110111	← Data →			7	A–byte	Borrow
			r, byte	01110100	00111 R_2 R_1 R_0	Data		11	r–byte	Borrow
			sr2, byte	0110 ↓	S_3 0111 S_2 S_1 S_0	↓		14	sr2–byte	Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
16-BIT ARITHMETIC	DSUB	EA, rp3	01110100	111001 P_1 P_0			11	EA ← EA−rp3	
	DSBB	EA, rp3		1111			11	EA ← EA−rp3−CY	
	DSUBNB	EA, rp3		1011			11	EA ← EA−rp3	No Borrow
	DAN	EA, rp3		100011 P_1 P_0			11	EA ← EA ∧ rp3	
	DOR	EA, rp3		1001			11	EA ← EA ∨ rp3	
	DXR	EA, rp3		100101 P_1 P_0			11	EA ← EA ∨̄ rp3	
	DGT	EA, rp3		101011 P_1 P_0			11	EA−rp3−1	No Borrow
	DLT	EA, rp3		1011			11	EA−rp3	Borrow
	DNE	EA, rp3		1110			11	EA−rp3	No Zero
	DEQ	EA, rp3		1111			11	EA−rp3	Zero
	DON	EA, rp3		1100			11	EA ∧ rp3	No Zero
	DOFF	EA, rp3		1101			11	EA ∧ rp3	Zero
MULTIP/DIVIDE	MUL	r2	01001000	001011 R_1 R_0			32	EA ← A X r2	
	DIV	r2		0011			59	EA ← EA÷r2, r2 ← surplus	
INCREMENT/DECREMENT	INR	r2	010000 R_1 R_0				4	r2 ← r2+1	Carry
	INRW *	wa	00100000	← Offset →			16	(V.wa) ← (V.wa)+1	Carry
	INX	rp	00 P_1 P_0 0010				7	rp ← rp+1	
		EA	10101000				7	EA ← EA+1	
	DCR	r2	010100 R_1 R_0				4	r2 ← r2−1	Borrow
	DCRW *	wa	00110000	← Offset →			16	(V.wa) ← (V.wa)−1	Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
ROTATE AND SHIFT	DCX	rp	00 P_1 P_0 0011				7	rp ← rp−1	
		EA	10101001				7	EA ← EA−1	
	RLL	r2	01001000	001101 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow CY$, $CY \leftarrow r2_7$	
	RLR	r2		00 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow CY$, $CY \leftarrow r2_0$	
	SLL	r2		001001 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	
	SLR	r2		00 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	
	SLLC	r2		000001 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	Carry
	SLRC	r2		00 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	Carry
	DRLL	EA	10110100				8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow CY$, $CY \leftarrow EA_{15}$	
	DRLR	EA		0000			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow CY$, $CY \leftarrow EA_0$	
	DSLL	EA	10100100				8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow 0$, $CY \leftarrow EA_{15}$	
	DSLR	EA		0000			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow 0$, $CY \leftarrow EA_0$	
	DAA		01100001				4	Decimal Adjust Accumulator	
	STC		01001000	00101011			8	CY ← 1	
	CLC			00101010			8	CY ← 0	
	NEGA			00111010			8	A ← A+1	
	RLD		01001000	00111000			17	Rotate Left Digit	
	RRD			1001			17	Rotate Right Digit	

3

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
JUMP	JMP *	word	01010100	← Low Adrs →	High Adrs		10	PC ← word	
	JB		00100001				4	PC_H ← B, PC_L ← C	
	JR	word	11 ← jdispl →				10	PC ← PC+1+jdispl	
	JRE *	word	0100111 ←	jdisp →			10	PC ← PC+2+jdispl	
	JEA		01001000	00101000			8	PC ← EA	
CALL	CALL *	word	01000000	← Low adrs →	High Adrs		16	$(SP-1) \leftarrow (PC+3)_H$, $(SP-2) \leftarrow (PC+3)_L$, PC ← word, SP ← SP−2	
	CALB		01001000	00101001			17	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$, PC_H ← B, SP ← SP−2, PC_L ← C	
	CALF *	word	01111 ←	fa →			13	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$, PC_{15-11} ← 00001, PC_{10-0} ← fa, SP ← SP−2	
	CALT	word	100 ← ta →				16	$(SP-1) \leftarrow (PC+1)_H$, $(SP-2) \leftarrow (PC+1)_L$, $PC_L \leftarrow (128+2ta)$, $PC_H \leftarrow (129+2ta)$, SP ← SP−2	
	SOFTI		01110010				16	$(SP-1) \leftarrow PSW$, $(SP-2) \leftarrow (PC+1)_H$, $(SP-3) \leftarrow (PC+1)_L$, PC ← 0060H, SP ← SP−3	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
RETURN	RET		10111000				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, SP ← SP+2	
	RETS		1001				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, SP ← SP+2, PC ← PC+n	
	RETI		01100010				13	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, PSW ← (SP+2), SP ← SP+3	Unconditional Skip
SKIP	SK	f	01001000	00001 F_2 F_1 F_0			8	Skip if f=1	f=1
	SKN	f		0001			8	Skip if f=0	f=0
	SKIT	irf		010 I_4 I_3 I_2 I_1 I_0			8	Skip if irf=1, then reset irf	irf=1
	SKNIT	irf		011 I_4 I_3 I_2 I_1 I_0			8	Skip if irf=0 Reset irf, if irf=1	irf=0
CPU CONTROL	NOP		00000000				4	No Operation	
	EI		10101010				4	Enable Interrupt'	
	DI		10111010				4	Disable Interrupt	
	HLT		01001000	00111011			11	Halt	

Notes:

(*1): B2(Data) : rpa2 = D+byte, H+byte
(*2): B3(Data) : rpa3 = D+byte, H+byte
(*3): right side of slash (/) in states indicates case rpa2, rpa3 = D+byte, H+A, H+B, H+EA, H+byte
(*4): in the case of skip condition, the idle states are as follows

1-byte instruction : 4 states
2-byte instruction : 8 states
3-byte instruction : 11 states
2-byte instruction (with *) : 7 states
3-byte instruction (with *) : 10 states
4-byte instruction : 14 states

Additional instruction for μPD78C10/C11/C14:

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
	STOP		01001000	10111011			12	Stop	

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

Parameter	Symbol	Test Condition	Ratings	Unit
Power Supply Voltage	V_{DD}		−0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD} + 0.5	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to V_{DD} +0.5	V
Output Voltage	V_O		−0.5 to V_{DD} +0.5	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−2.0	mA
		All Output Pin Total	−50	mA
Reference Input Voltage	V_{AREF}		−0.5 to AV_{DD} +0.3	V
Operating Temperature	T_{opt}	$f_{XTAL} \leq$ 12MHz	−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OPERATING CONDITION

OSC frequency \ Parameter	Ta	V_{DD}, AV_{DD}
$f_{XTAL} \leq$ 15MHZ	−40°C to +85°C	+5.0V ± 10%

CAPACITANCE

(T_a = 25°C, V_{DD} = V_{SS} = 0V)

Paramater	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Input Capacitance	C_I	f_C = 1MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	C_{IO}				20	pF

3

(T_a = −40 to +85 °C, V_{DD} = AV_{DD} = 5V ± 10%, V_{SS} = AV_{SS} = 0V, V_{DD} − 0.8V ≤ AV_{DD} ≤ V_{DD}, 3.4V ≤ V_{AREF} ≤ AV_{DD})

OSCILLATION CHARACTERISTICS

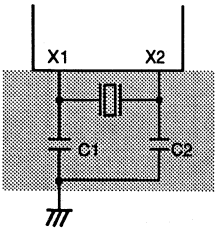
Resonator	Recommended Circuit	Parameters	Test Conditions	MIN	TYP	MAX	UNIT
Ceramic*1 Resonator or XTAL*2	(*3)	Oscillation Frequency (f_{XX})	A/D Converter Not used	4		15	MHz
			A/D Converter Used	5.8		15	MHz
External Clock	(*4)	X1 Input Frequency (f_X)	A/D Converter Not used	4		15	MHz
			A/D Converter Used	5.8		15	MHz
		X1 Input Rise, Fall Time (t_r,t_f)		0		20	ns
		X1 Input High, Low Level Width (t_H, T_L)		20		250	ns

* 1: Recommended ceramic resonators and external capacitance, as follows.

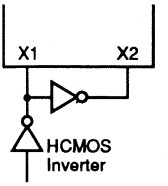
	Manufacturer	Product name	Recommended circuit constants (pF)	
			C1	C2
15 MHz	Murata	CSA15.0X3	22	22
		CSA12.0MT	30	30
		CST12.0MT	On-chip	On-chip
		CSA10.0MT	30	30
		CST10.0MT	On-chip	On-chip
		CSA6.00MG	30	30
		SCT6.00MG	On-chip	On-chip
	TDK	FCR12.0MC	On-chip	On-chip
12 MHz	Murata	CSA12.0MT18	30	30
		CST12.0MT18	On-chip	On-chip

* 2: For XTAL, the following external capacitances are recommended:
C1 = C2 = 10 pF

* 3:



* 4:



Note 1: Oscillator circuti should be in the nearest area from X1 and X2 pins.
Note 2: Do not place other signal lines in the range of ▨.

(T_a = -40°C to +85°C, V_{DD} = +5.0V±10%, V_{SS} = 0V)

DC CHARACTERISTICS

Parameter	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL1}	All except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT 1, TI, AN4 to 7	0		0.8	V
	V_{IL2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to 7	0		$0.2V_{DD}$	V
Input High Voltage	V_{IH1}	All except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to 7, X1, X2	2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to 7, X1, X2	$0.8V_{DD}$		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	V_{DD}-1.0			V
		I_{OH} = -100μA	V_{DD}-0.5			V
Input Current	I_I	INT1, TI (PC3); $0V \leq V_I \leq V_{DD}$			±200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3), $0V \leq V_I \leq V_{DD}$			±10	μA
Output Leakage Current	I_{LO}	$0V \leq V_O \leq V_{DD}$			±10	μA
AV_{DD} Supply Current	AI_{DD}			0.5	1.3	mA
AV_{DD} Supply Current	AI_{DD2}	STOP MODE		10	20	μA
V_{DD} Supply Current	I_{DD1}	Operation mode f=15MHz		16	30	mA
	I_{DD2}	HALT MODE f=15 MHz		8	15	mA
Data Retention Voltage	V_{DDDR}	Hardware/Software STOP MODE	2.5			V
Data Retention Current	I_{DDDR}	Hardware/Software STOP Mode, V_{DDDR} = 2,5V		1	15	μA
		V_{DDDR} = 5V±10%		10	50	μA

3

AC CHARACTERISTICS (T_a = -40°C to +85°C, V_{DD} = + 5.0 V ± 10%, V_{SS} = 0V)

READ/WRITE OPERATION

Parameter	Symbol	Test Condition	MIN	MAX	Unit
X1 Input Cycle Time	t_{CYC}		66	250	ns
Address Setup to ALE↓	t_{AL}	*3, *4	30		ns
Adress Hold after ALE↓	t_{LA}	*3, *4	35		ns
Adress to $\overline{RD}$↓ Delay Time	t_{AR}	*3, *4	100		ns
$\overline{RD}$↓ to Address Floating	t_{AFR}	*4		20	ns
Adress to Data Input	t_{AD}	*3, *4		250	ns
ALE↓ to Data Input	t_{LDR}	*3, *4		135	ns
$\overline{RD}$↓ to Data Input	t_{RD}	*3, *4		120	ns
ALE to $\overline{RD}$↓ Delay Time	t_{LR}	*3, *4	15		ns
Data Hold after $\overline{RD}$↑	t_{RDH}	*4	0		ns
$\overline{RD}$↑ to ALE↑ Delay Time	t_{RL}	*3, *4	80		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read, *3, *4	215		ns
		OP code Fetch, *3, *4	415		ns
ALE Width High	t_{LL}	*3, *4	90		ns
$\overline{M1}$ Setup time to ALE↓	t_{ML}	*3	30		ns
$\overline{M1}$ Hold Time after ALE↓	t_{LM}	*3	35		ns
$\overline{IO}$/M Setup Time to ALE↓	t_{IL}	*3	30		ns
$\overline{IO}$/M Hold Time after ALE↓	t_{LI}	*3	35		ns
Address to $\overline{WR}$↓ Delay	t_{AW}	*3, *4	100		ns
ALE↓ to Data Output	t_{LDW}	*3, *4		180	ns
$\overline{WR}$↓ to Data Output	t_{WD}	*4		100	ns
ALE to $\overline{WR}$↓ Delay	t_{LW}	*3, *4	15		ns
Data Setup Time to $\overline{WR}$↑	t_{DW}	*3, *4	165		ns
Data Hold Time after $\overline{WR}$↑	t_{WDH}	*3, *4	60		ns
$\overline{WR}$↑ to ALE ↑ Delay Time	t_{WL}	*3, *4	80		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *4	215		ns

AC CHARACTERISTICS
SERIAL OPERATION

Parameter	Symbol	Test Condition		MIN	MAX	UNIT
$\overline{SCK}$ Cycle Time	tCYK	$\overline{SCK}$ Input	*5	800		ns
			*6	400		ns
		$\overline{SCK}$ Output		1.6		μs
$\overline{SCK}$ Width Low	tKKL	$\overline{SCK}$ Input	*5	335		ns
			*6	160		ns
		$\overline{SCK}$ Output		700		ns
$\overline{SCK}$ Width High	tKKH	$\overline{SCK}$ Input	*5	335		ns
			*6	160		ns
		$\overline{SCK}$ Output		700		ns
RxD Setup Time to $\overline{SCK}$↑	tRXK	*5		80		ns
RxD Hold Time After $\overline{SCK}$↑	tKRX	*5		80		ns
$\overline{SCK}$↓ to TxD Delay Time	tKTX	*5			210	ns

A/D CONVERTER
CHARACTERISTICS

(T_a = −40°C to +85°C, V_{DD} = 5.0V ± 10%, AV_{DD} = +5.0V ± 10%, V_{SS} = AV_{SS} = 0V, V_{DD} −0.5V ≤ AV_{DD} ≤ V_{DD}, 3.4V ≤ VA_{REF} ≤ AV_{DD})

Parameter	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Resolution			8			Bits
Absolute Accuracy *1		3.4V ≤ VA_{REF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.8	%FSR
		4.0V ≤ VA_{REF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.6	%FSR
		T_a = −10 to +70°C, 4.0V ≤ VA_{REF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.4	%FSR
Conversion time	t_{CONV}	66ns ≤ t_{CYC} ≤ 110ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling Time	t_{SAMP}	66ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
Reference Voltage	V_{AREF}		3.4		AV_{DD}	V
V_{AREF} Current	I_{AREF1}	Operation mode		1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} Supply Current	AI_{DD1}	Operation mode, f_{XX} = 15MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA

*1: Except quantization error (i.e. ±1/2 LSB).

3

ZERO-CROSS CHARACTERISTICS

(T_a = -40°C to +85°C, V_{DD} = +5.0V±10%, V_{SS} = 0V)

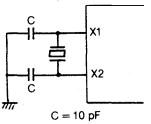
Parameter	Symbol	Test Condition	MIN	MAX	UNIT
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60Hz Sine Wave		±135	mV
Zero-Cross Detection Input Frequency	f_{ZX}		0.05	1	kHz

OTHER OPERATIONS

(T_a = -40°C to +85°C, V_{DD} = +5.0V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	MIN	MAX	UNIT
TI width high, low	t_{TIH}, t_{TIL}		6		t_{CYC}
CI width high, low	t_{CI1H}, t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ width high, low	t_{NIH}, t_{NIL}		10		μs
INT1 width high, low	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ width high, low	t_{I2H}, t_{I2L}		36		t_{CYC}
$\overline{RESET}$ width high, low	t_{RSH}, t_{RSL}		10		μs

*1. For XTAL oscillation, following circuit is recommended.



C = 10 pF

*2. T_a = +25°C, V_{DD} = 5 V

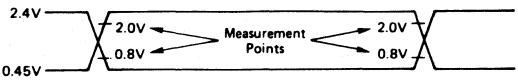
*3. f_{XTAL} = 15MHZ

*4. Load Capacitance: C_L = 150pF

*5. x1 Clock Rate in Asynchronous Mode, Synchronous Mode, I/O Interface Mode

*6. x16, x64 Clock Rate in Asynchronous Mode

AC TIMING MEASUREMENT POINT



BUS TIMING DEPENDING ON t_{CYC}

Symbol	Calculating Expression	MIN./MAX.	units
t_{AL}	2T - 100	MIN	ns
t_{LA}	T - 30	MIN	ns
t_{AR}	3T - 100	MIN	ns
t_{AD}	7T - 220	MAX	ns
t_{LDR}	5T - 200	MAX	ns
t_{RD}	4T - 150	MAX	ns
t_{LR}	T - 50	MIN	ns
t_{RL}	2T - 50	MIN	ns
t_{RR}	4T - 50 (Data Read)	MIN	ns
	7T - 50 (OP Code Fetch)		
t_{LL}	2T - 40	MIN	ns
t_{ML}	2T - 100	MIN	ns
t_{LM}	T - 30	MIN	ns
t_{IL}	2T - 100	MIN	ns
t_{LI}	T - 30	MIN	ns
t_{AW}	3T - 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T - 50	MIN	ns
t_{DW}	4T - 100	MIN	ns
t_{WDH}	2T - 70	MIN	ns
t_{WL}	2T - 50	MIN	ns
t_{WW}	4T - 50	MIN	ns
t_{CYK}	12T ($\overline{SCK}$ Input) *1	MIN	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	5T + 5 ($\overline{SCK}$ Input) *1	MIN	ns
	12T - 100 ($\overline{SCK}$ Output)		
t_{KKH}	5T + 5 ($\overline{SCK}$ Input) *2	MIN	ns
	12T - 100 ($\overline{SCK}$ Output)		

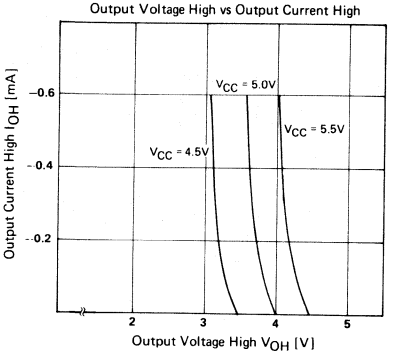
Note 1. In case of x1 clock rate in asynchronous mode, synchronous mode, or I/O interface mode.
2. $T = t_{CYC} = 1/f_{XTAL}$
3. Parameters which can't be found in this table don't depend on oscillation frequency (f_{XTAL}).

3

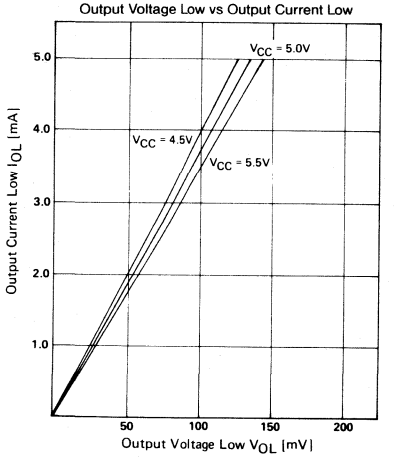
CHARACTERISTICS CURVE
— REFERENCE —

(T_a = 25°C)

Output Voltage High vs Output Current High

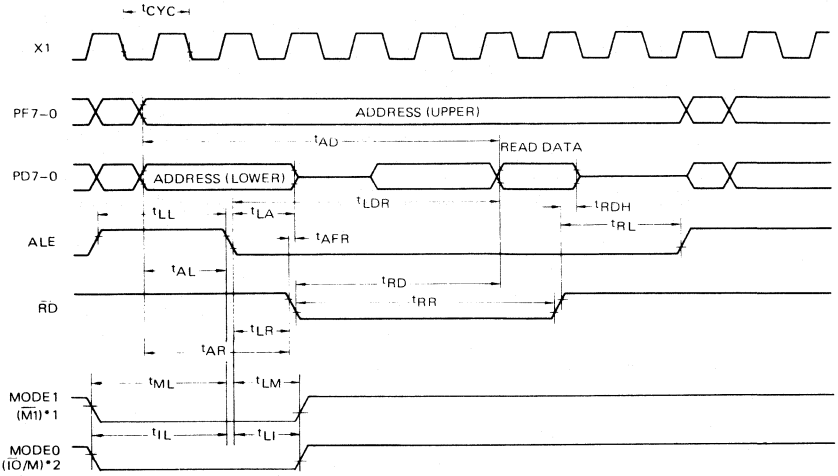


Output Voltage Low vs Output Current Low



TIMING WAVEFORM

Read Operation



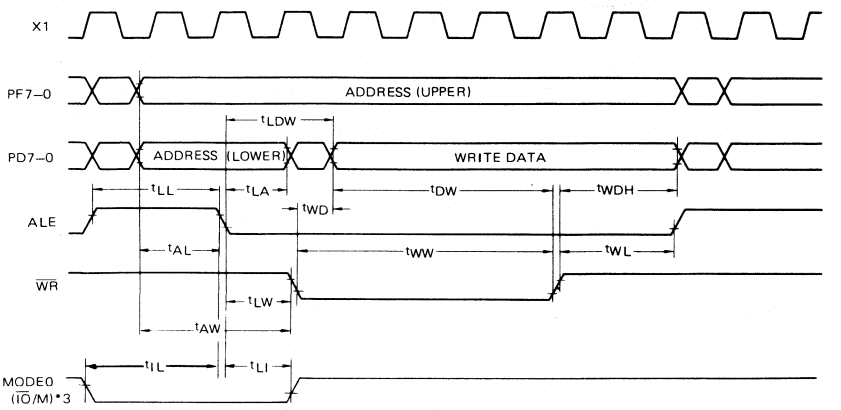
*1 $\overline{M1}$ is output at the fetech cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

*2 $\overline{IO}$/M is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

3

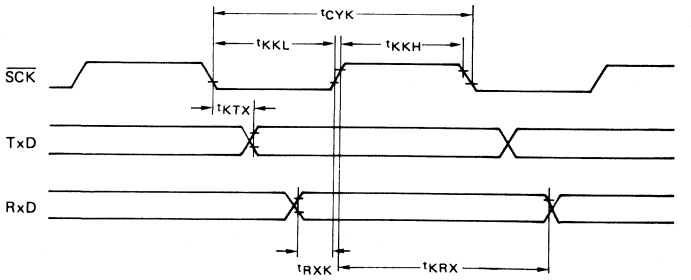
TIMING WAVEFORM

Write Operation

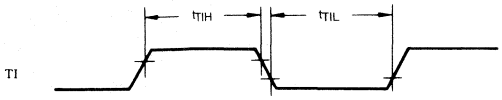


*3 $\overline{IO}$/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Serial Operation

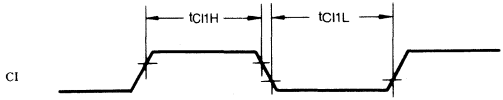


TIMER INPUT TIMING

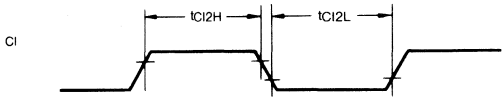


TIMER/EVENT COUNTER INPUT TIMING

EVENT COUNT MODE

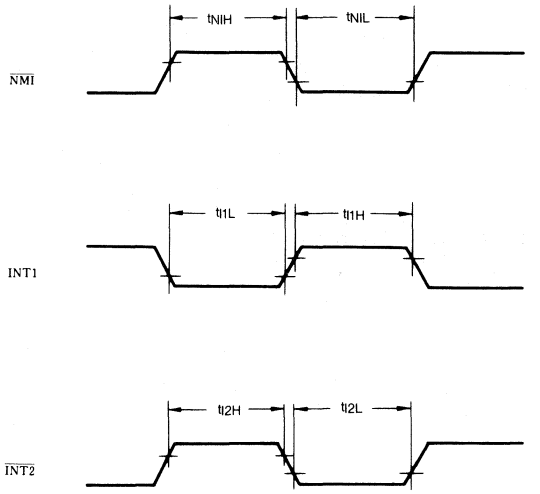


PULSE WIDTH MEASUREMENT MODE

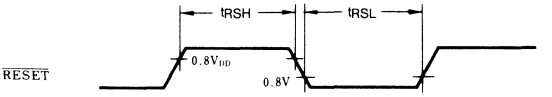


3

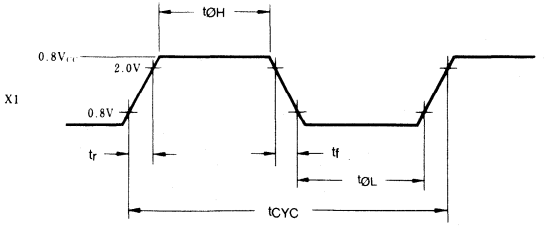
INTERRUPT INPUT TIMING



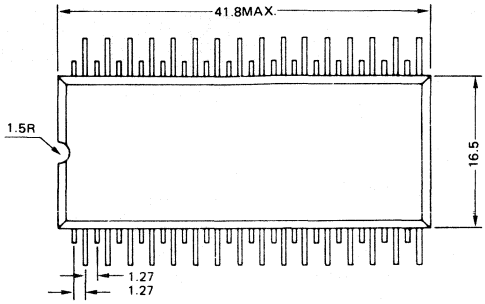
RESET INPUT TIMING

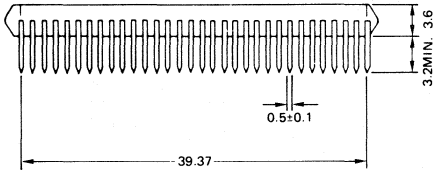


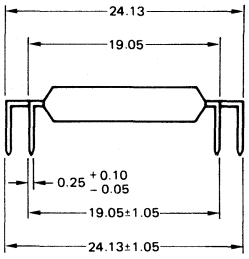
EXTERNAL CLOCK TIMING



64 PIN PLASTIC QUIP (Bent Leads)
OUTLINE (Units: mm)
μPD78C10G/μPD78C11G/μPD78C14G

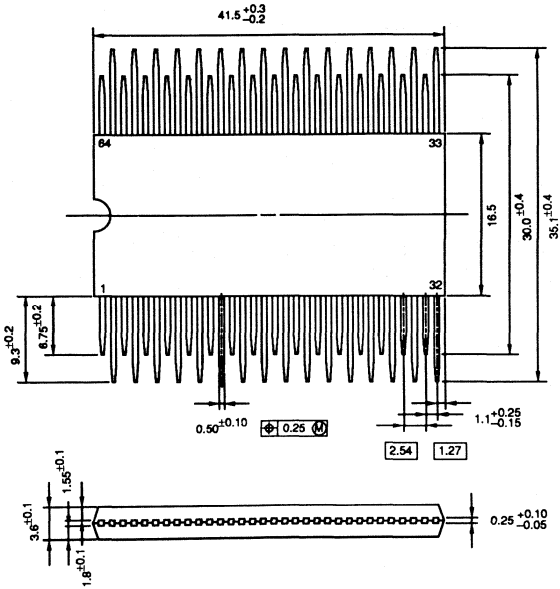




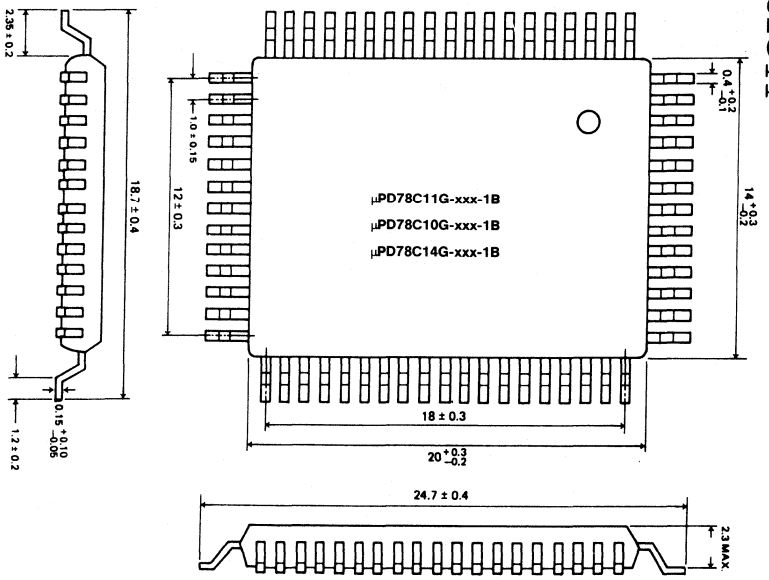


When ordering this package, specify as follows:
μPD78C10G-36
μPD78C11G-xxx-36
μPD78C14G-xxx-36

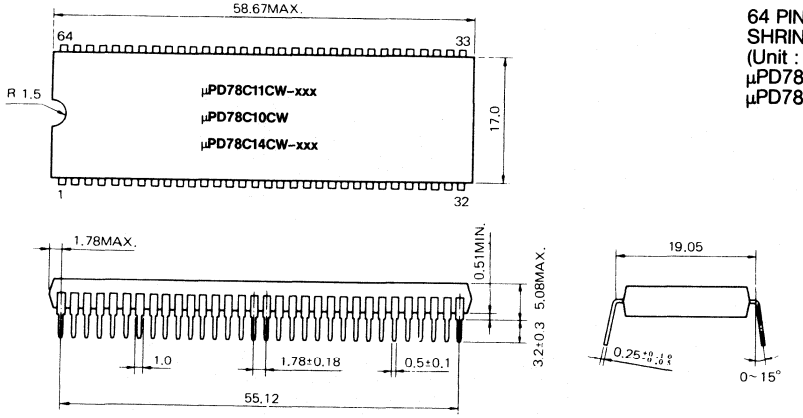
64 PIN PLASTIC QUIP STRAIGHT LEADS PACKAGE DIMENSIONS (Units: mm)



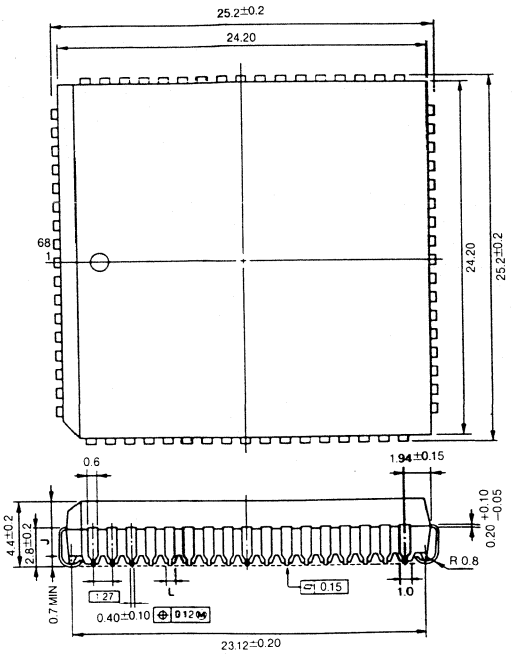
64 PIN PLASTIC
FLAT PACK OUTLINE
(Unit : mm)
μPD78C10G/C11G
μPD78C14G



64 PIN PLASTIC
SHRINK DIP OUTLINE
(Unit : mm)
μPD78C10CW/C11CW
μPD78C14CW



68 PIN PLASTIC LCC
PACKAGE OUTLINE
μPD78C10L/C11L/C14L



3

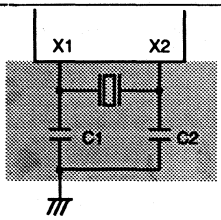
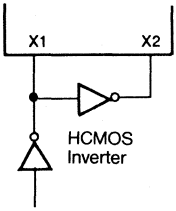
Electrical Characteristics

Absolute Maximum Ratings (Ta = 25 °C)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply voltage	V_{DD}		−0.5 ~ +7.0	V
	AV_{DD}		AV_{SS} ~ V_{DD} + 0.5	V
	AV_{SS}		−0.5 ~ + 0.5	V
Input voltage	V_I		−0.5 ~ V_{DD} + 0.5	V
Output voltage	V_O		−0.5 ~ V_{DD} + 0.5	V
Low-level output current	I_{OL}	All output pins	4.0	mA
		Total of all output pins	100	mA
High-level output current	I_{OH}	All output pins	−2.0	mA
		Total of all output pins	−50	mA
A/D converter reference voltage	V_{AREF}		−0.5 ~ AV_{DD} + 0.3	V
Operating temperature	T_{opt}		−40 ~ +85	°C
Storage temperature	T_{stg}		−65 ~ +150	°C

Oscillator Characteristics

(T_a = −40 to 85 °C, V_{DD} = AV_{DD} = +5.0V ± 10%, V_{SS} = AV_{SS} = 0V, V_{DD} − 0.8V ≤ AV_{DD} ≤ V_{DD}, 3.4V ≤ V_{AREF} ≤ AV_{DD})

Oscillator	Recommended circuit	Item	Condition	MIN.	MAX.	Unit
Ceramic oscillatior*1 or crystal oscillator*2		Oscillation frequency (fxx)	A/D Converter is not used.	4	15	MHZ
			A/D Converter is used.	5.8	15	MHz
External Clock		X1 input frequency (fx)	A/D Converter is not used.	4	15	MHz
			A/D Converter is used.	5.8	15	MHz
		X1 input rise time and fall time (t_r and t_f)		0	20	ns
		X1 input high and low level width (t_{OH} and t_{OL})		20	250	ns

*1. Locate the oscillator circuit as close to the X1 and X2 pin as possible.
*2. Do not wire any other signal lines in the shaded area ▨.

Note 1. The following ceramic oscillators and external capacitors are recommandeds:

For μPD78C14A

	Manufacturer	Product Name	Recommended constants	
			C1 pF	C2 pF
15-MHz product	Murata Mfg. Co., Ltd.	CSA15.0MX3	22	22
		CSA12.0MT	30	30
		CST12.0MT	not required	not required
		CSA10.0MT	30	30
		CST10.0MT	not required	not required
		CSA6.00MG	30	30
		CST6.00MG	not required	not required
	TDK	FCR12.0MC	not required	not required
12-MHz product	Murata Mfg. Co.,Ltd.	CAS12.0MT18	30	30
		CST12.0MT18	not required	not required

For 78C10A, 78C11A and 78C12A:

Manufacturer	Product name	Recommended circuit constants (pF)	
		C1	C2
Murata	CSA15.00MX001	15	15
	CSA12.0MT	30	30
	CST12.0MT	Not required	Not required
	CSA7.37MT	30	30
	CST7.37MT	Not required	Not required

Note 2. The recommended capacitance of the external capacitor is as follows when the crystal oscillator is used:
C1 = C2 = 10 pF

Capacitance (Ta = 25°C, $V_{DD} = V_{SS} = 0V$)

Item	Symbol	Condition	MIN	TYP	MAX	UNIT
Input capacitance	C_I	f_c = 1MHz Pins other than measured pins are at 0V			10	pF
Output capacitance	C_O				20	pF
Input/Output capacitance	C_{IO}				20	pF

DC Characteristics (Ta = −40 to +85°C, $V_{DD} = AV_{DD} = +5.0V \pm 10\%$; $V_{SS} = AV_{SS} = 0V$)

Item	Symbol	Condition	MIN	TYP	MAX	UNIT
Low-level input voltage	V_{IL1}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1 T1, and AN4-AN7 are excepted	0		0.8	V
	V_{IL2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1 T1, AN4-AN7	0		$0.2V_{DD}$	V
High-level input voltage	V_{IH1}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1 T1, AN4-AN7, X1, and X2 are excepted	2.2		V_{DD}	V
	V_{IH2}	RESET, STOP, NMI, SCK, INT1 T1, AN4-AN7, X1, and X2	$0.8V_{DD}$		V_{DD}	V
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
High-level output voltage	V_{OH}	I_{OH} = −1.0 mA VDD −1.0	V_{DD} −1.0			V
		I_{OH} = −100μA VDD −0.5	V_{DD} −0.5			V
Input current	I_I	INT1*1, TI (PC3) *2; $0V \le V_I \le V_{DD}$			±200	μA
Input leakage current	I_{LI}	Except INT1, TI (PC3) ; $0V \le V_I \le V_{DD}$			±10	μA
Output leakage current	I_{LO}	$0V \le V_O \le V_{DD}$			±10	μA
AV_{DD} supply current	AI_{DD1}	Operation mode f_{XX} = 15 MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA
V_{DD} suplly current *4	I_{DD1}	Operation mode f_{XX} = 15 MHz		13	25	mA
	I_{DD2}	HALT mode f_{XX} = 15 MHz		7	13	mA
Data retention voltage	V_{DDDR}	Hardware/Software STOP mode	2.5			V
Data retention current*4	I_{DDDR}	Hardware/Software: V_{DDDR} = 2.5V		1	15	μA
		STOP mode*3: V_{DDDR} = 5V±10%		10	50	μA
Pull-up resistance *5	R_L	Port A, B, C $3.5V \le V_{DD} \le 5.5V$; V_I = 0V	17	27	75	kΩ

Note
1. When generation of self-bias is specified by the ZCM register
2. When control mode is specified by the MCC register and generation of self-bias is specified by the ZCM register
3. When self-bias is not generated.
4. Current flowing into the internal pull-up resistor is not included.
5. μPD78C11A, C12A C14A have Mask Option on Port A, B, C.

AC Characteristics (Ta = –40 to +85°C, $V_{DD} = AV_{DD} = +5.0V \pm 10\%$; $V_{SS} = AV_{SS} = 0V$)
Read/Write Operation

Item	Symbol	Condition	MIN	MAX	UNIT
X1 input cycle time	t_{CYC}		66	250	ns
Address setup time (vs. ALE ↓)	t_{AL}	f_{XX} = 15 MHz, C_L = 100pF	30		ns
Address hold time (vs. ALE ↓)	t_{LA}		35		ns
Address → RD↓ delay time	t_{AR}		100		ns
RD↓ → address float time	t_{AFR}	C_L = 100 pF		20	ns
Address → data input time	t_{AD}	f_{XX} = 15 MHz, C_L = 100pF		250	ns
ALE↓ → data input time	t_{LDR}			135	ns
RD↓ → data input time	t_{RT}			120	ns
ALE↓ → RD↓ delay time	t_{LR}		15		ns
Data hold time (vs. RD↓)	t_{RDH}	C_L = 100 pF	0		ns
RD↓ → ALE ↓ delay time	t_{RL}	f_{XX} = 15 MHz, C_L = 100pF	80		ns
RD low level width	t_{RR}	When reading data f_{XX} = 15 MHz, C_L = 100pF	215		ns
		When fetching opcode f_{XX} = 15 MHz, C_L = 100pF	415		ns
ALE high-level width	t_{LL}	f_{XX} = 15 MHz, C_L = 100pF	90		ns
M1 setup time (vs. ALE↓)	t_{ML}	f_{XX} = 15 MHz	30		ns
M1 hold time (vs. ALE ↓)	t_{LM}		35		ns
IO/M setup time (vs. ALE↓)	t_{IL}		30		ns
IO/M hold time (vs. ALE↓)	t_{LI}		35		ns
Address → WR ↓ delay time	t_{AW}	f_{XX} = 15 MHz, C_L = 100pF	100		ns
ALE↓ → data output time	t_{LDW}			180	ns
WR↓ → data output time	t_{WD}	C_L = 100 pF		100	ns
ALE↓ → WR↓ delay time	t_{LW}	f_{XX} = 15 MHz, C_L = 100pF	15		ns
Data setup time (vs. WR↑)	t_{DW}		165		ns
Data hold time (vs. WR↑)	t_{WDH}		60		ns
WR↑ → ALE ↑ delay time	t_{WL}		80		ns
WR low-level width	t_{WW}		215		ns

DC Characteristics (Ta = −40 to +85°C, $V_{DD} = AV_{DD} = +5.0V \pm 10\%$; $V_{SS} = AV_{SS} = 0V$)

Serial Operation

Item	Symbol	Condition		MIN	MAX	UNIT
SCK cycle time	t_{CYK}	SCK input	See Note 1.	800		ns
			See Note 2.	400		ns
		SCK output		1.6		ns
SCK low-level width	t_{KKL}	SCK input	See Note 1.	335		ns
			See Note 2.	160		ns
		SCK output		700		ns
SCK high-level width	t_{KKH}	SCK input	See Note 1.	335		ns
			See Note 2.	160		ns
		SCK output		700		ns
RxD setup time (vs. SCK↑)	t_{RXK}	See Note 1.		80		ns
RxD hold time (vs. SCK↑)	t_{KRX}	See Note 1.		80		ns
SCK↓ → TxD delay time	t_{KTX}	See Note 1.			210	ns

Note: 1. In asynchronous mode with clock rate of X1, or synchronous or I/O interface mode.
2. In asynchronous mode with clock rate of X16 or X64

Zero Crossover Characteristics

Item	Symbol	Condition	MIN	MAX	UNIT
Zero crossover detection input	V_{ZX}	AC coupling 60-Hz sine wave	1	1.8	VAC_{P-P}
Zero crossover accuracy	A_{ZX}			±135	mV
Zero crossover detection input frequency	f_{ZX}		0.05	1	kHz

Other Operations

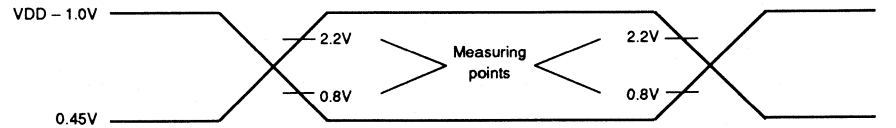
Item	Symbol	Condition	MIN	MAX	UNIT
TI high- and low-level widths	t_{TIH}, t_{TIL}		6		t_{CYC}
CI high- and low-level widths	t_{CI1H}, t_{CI1L}	Event counter mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse width measuring mode	48		t_{CYC}
NMI high- and low-level widths	t_{NIH}, t_{NIL}		10		μs
INT1 high- and low-level widths	t_{I1H}, t_{I1L}		36		t_{CYC}
INT2 high- and low-level widths	t_{I2H}, t_{I2L}		36		t_{CYC}
RESET high- and low-level widths	t_{RSH}, t_{RSL}		10		μs

A/D Converter Characteristics
(Ta = – 40 to +85°C, V_{DD} = + 5.0V ± 10%; V_{SS} = AV_{SS} = 0V V_{DD} -0.5V ≤ AV_{DD} ≤ V_{DD}, 3.4V ≤ V_{AREF} ≤ AV_{DD})

Item	Symbol	Condition	MIN	TYP	MAX	UNIT
Resolution			8			Bits
Absolute accuracy (See Note.)		3.4V ≤ V_{AREF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.8%	FSR
		4.0V ≤ V_{AREF} ≤ AV_{DD} 66ns ≤ t_{CYC} ≤ 170ns			±0.6%	FSR
		Ta = -10 ~ +170 °C, 4.0V ≤ V_{AREF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.4%	FSR
Conversion time		66ns ≤ t_{CYC} ≤ 110ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling time		66ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	72			t_{CYC}
Analog input voltage	V_{IAN}		0		V_{AREF}	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	V_{AREF}		3.4		AV_{DD}	V
V_{AREF} current	I_{AREF1}	Operation mode		1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} supply current	AI_{DD1}	Operation mode f_{XX} = 15MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA

Note: Quantization error (±1/2LSB) is not included.

AC Timing Points



Formular for calculation of AC characteristics dependet on t_{CYC}

Item	Formula	MIN/MAX	UNIT
t_{AL}	2T — 100	MIN	ns
t_{LA}	T — 30	MIN	ns
t_{AR}	3T — 100	MIN	ns
t_{AD}	7T — 220	MAX	ns
t_{LDR}	5T — 200	MAX	ns
t_{RD}	4T — 150	MAX	ns
t_{LR}	T — 50	MIN	ns
t_{RL}	2T — 50	MIN	ns
t_{RR}	4T — 50 (when reading data)	MIN	ns
	7T — 50 (when fetching opcode)		
t_{LL}	2T — 40	MIN	ns

Formular for calculation of AC characteristics dependet on t_{CYC} (Continued)

Item	Formula	MIN/MAX	UNIT
t_{ML}	2T — 100	MIN	ns
t_{LM}	T — 30	MIN	ns
t_{IL}	2T — 100	MIN	ns
t_{LI}	T — 30	MIN	ns
t_{AW}	3T — 100	MIN	ns
t_{LDW}	T + 110	MIN	ns
t_{LW}	T — 50	MIN	ns
t_{DW}	4T — 100	MIN	ns
t_{WDH}	2T — 70	MIN	ns
t_{WL}	2T — 50	MIN	ns
t_{WW}	4T — 50	MIN	ns
t_{CYK}	12T ($\overline{SCK}$ input) *	MIN	ns
	24T ($\overline{SCK}$ output)		
t_{KKL}	5T + 5 ($\overline{SCK}$ input) *	MIN	ns
	12T — 100 ($\overline{SCK}$ output)		
t_{KKH}	5T + 5 ($\overline{SCK}$ input) *	MIN	ns
	12T — 100 ($\overline{SCK}$ output)		

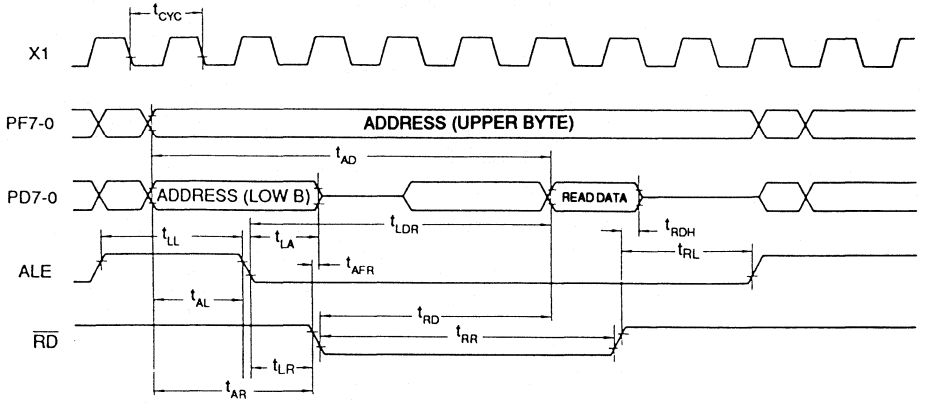
Note: In asynchronous mode with clock rate of X1, or in syncronous or I/O interface mode.

Remarks:

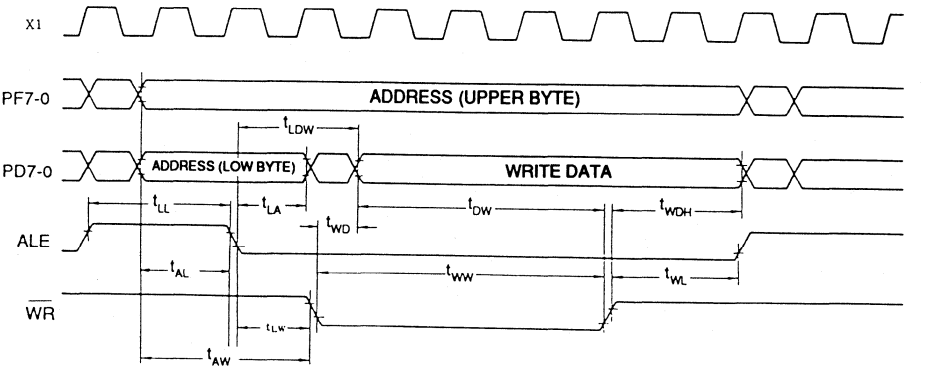
1. $T = t_{CYC} = 1/f_{XX}$
2. Items not shown here are not dependent on oscillation frequency f_{XX}.

3

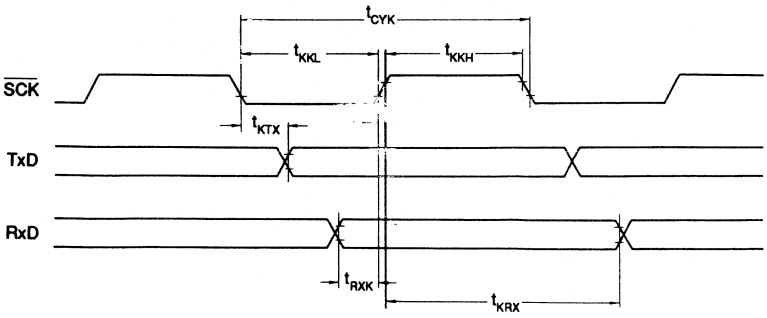
TIMING WAVEFORM
Read Operation



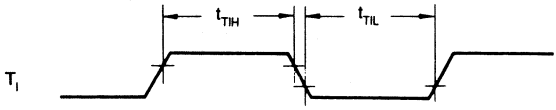
Write Operation



Serial Operation

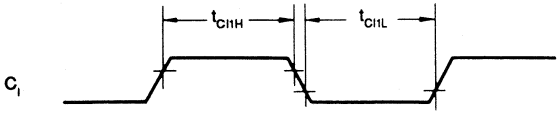


Timer Input Timing

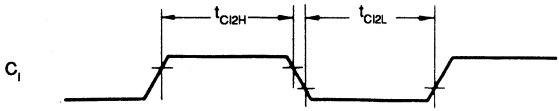


TIMER/EVENT COUNTER INPUT TIMING

Event Counter Mode

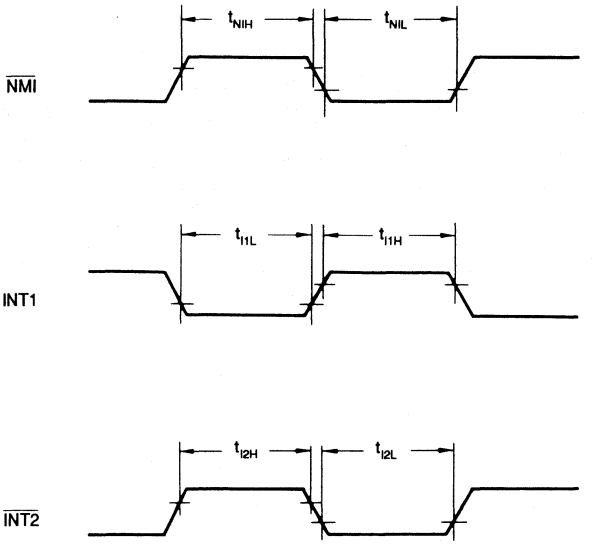


Pulse width measuring Mode

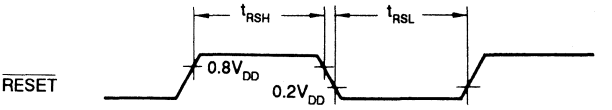


3

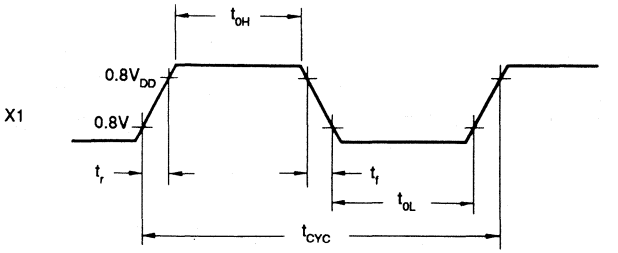
Interrupt Input Timing



Reset Input Timing



External Clock Timing

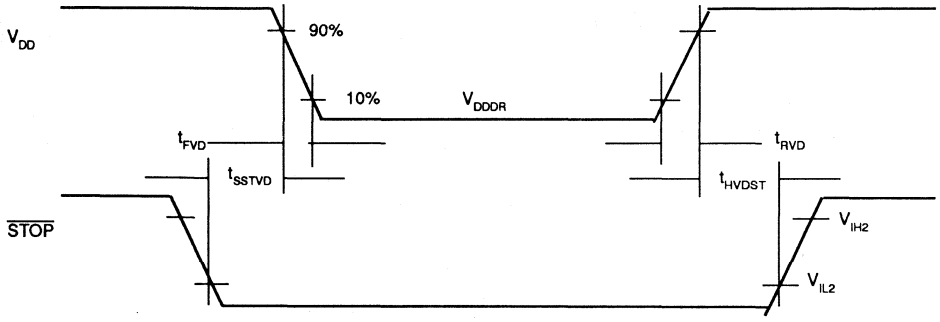


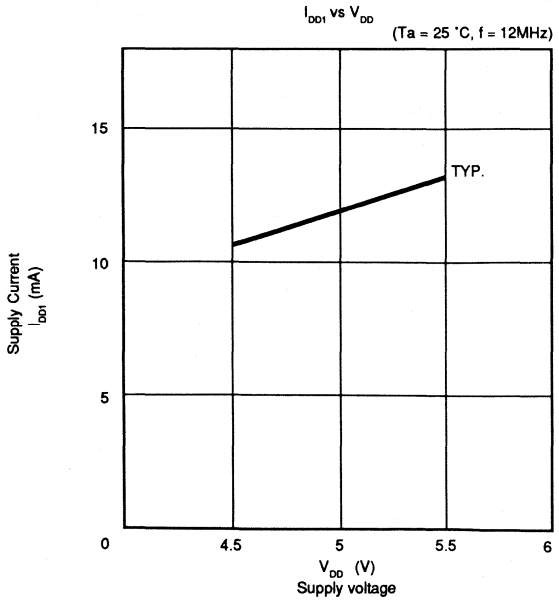
Data retention characteristics of low supply-voltage, data memory data retention STOP mode (Ta = -40 to +85 °C)

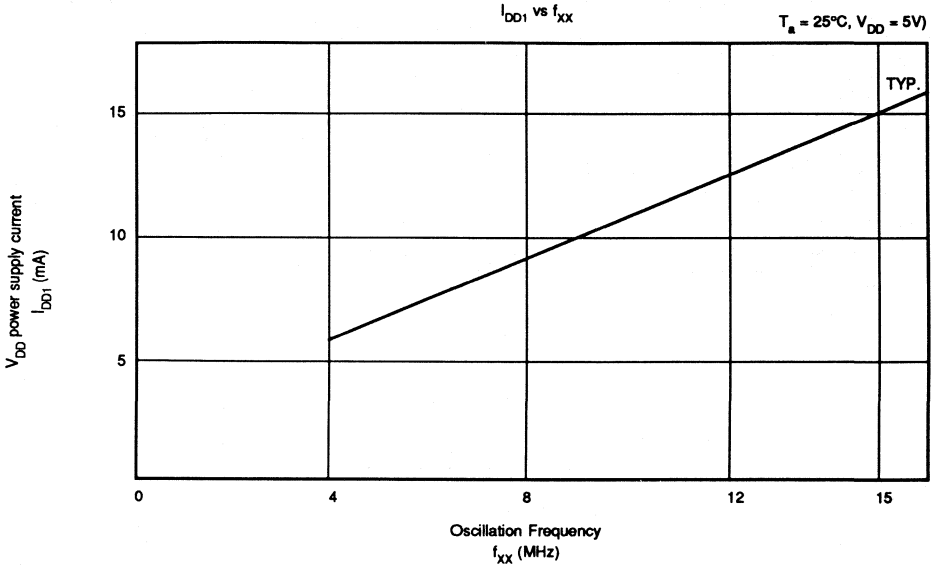
Item	Symbol	Condition	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}		2.5		5.5	V
Data retention supply voltage	I_{DDDR}	V_{DDDR} = 2.5V		1	15	μA
		V_{DDDR} = 5V ± 10%		15	50	μA
V_{DD} rise and fall times	t_{RVD}, t_{FVD}		200			μs
$\overline{STOP}$ setup time (vs. V_{DD})	t_{SSTVD}		12T + 0.5			μs
$\overline{STOP}$ hold time (vs. V_{DD})	t_{HVDST}		12T + 0.5			μs

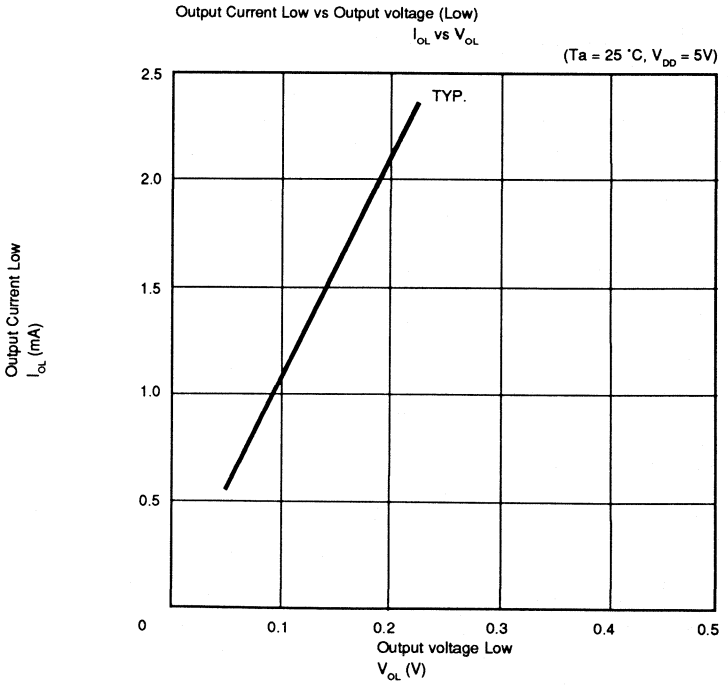
Remarks: $T = t_{CYC} = 1/f_{XX}$

Data retention Timing

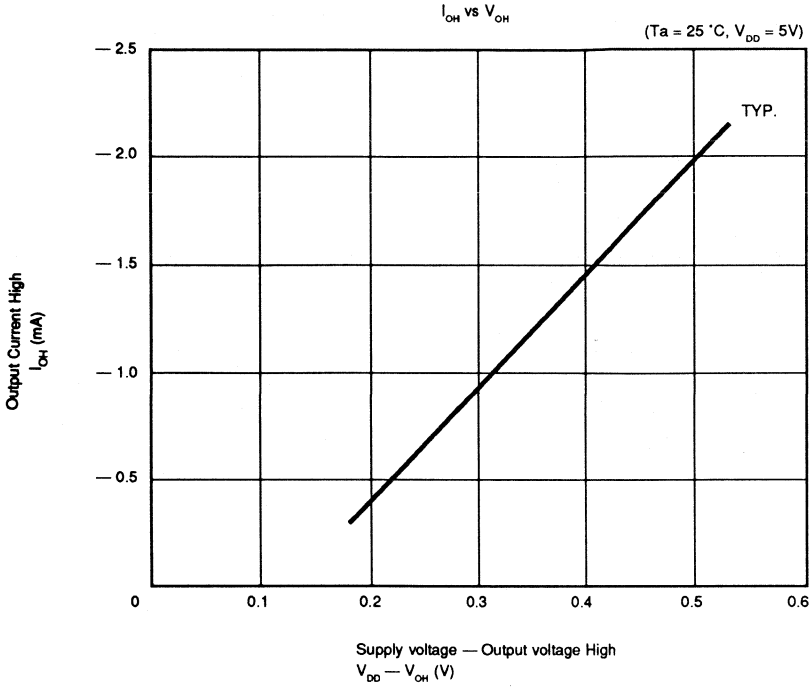





I_{DD1} vs f_{XX}
T_a = 25°C, V_{DD} = 5V)
TYP.
15
10
5
0
4
8
12
15
V_{DD} power supply current
I_{DD1} (mA)
Oscillation Frequency
f_{XX} (MHz)


Output Current Low vs Output voltage (Low)
I_{OL} vs V_{OL}
(Ta = 25 °C, V_{DD} = 5V)
TYP.
2.5
2.0
1.5
1.0
0.5
0
0.1
0.2
0.3
0.4
0.5
Output Current Low
I_{OL} (mA)
Output voltage Low
V_{OL} (V)

Output Current High vs Output voltage high



3

DIFFERENCE BETWEEN μCOM-87AD CMOS FAMILY PRODUCTS

Item \ Product	μPD78C12A	μPD78C14A	μPD78C14	μPD78C11	μPD87C10
Program capacity (ROM)	8K x 8 bits	16K x 8 bits	6K x 8 bits	4K x 8 bits	–
External memory area	56K bytes max.	48K bytes max.	48K bytes max.	60K bytes max.	64K bytes max.
I/O lines	44 bits	44 bits	44 bits	44 bits	32 bits
Pull-up resistor option	Can be internally provided (ports A, B, C)			None	

ELECTRICAL SPECIFICATIONS FOR AUTOMOTIVE TEMPERATURE RANGE

ABSOLUTE MAXIMUM (T_a = 25 °C)

PARAMETER	SYMBOL	TEST CONDITION	RATINGS	UNIT
Power Supply Voltage	V_{DD}		−0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD}+0.5	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to V_{DD}+0.5	V
Output Voltage	V_O		−0.5 to V_{DD}+0.5	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−2.0	mA
		All Output Pin Total	−50	mA
Reference Input Voltage	V_{AREF}		−0.5 to AV_{DD}+0.3	V
Operating Temperature	T_{OPT}	$f_{XTAL} \leqq 12$ MHz	−40 to +110	°C
Storage Temperature	T_{STG}		−65 to +150	°C

OPERATING CONDITION

PARAMETER / OSC. FREQ.	T_a	V_{DD}, AV_{DD}
$f_{XTAL} \leqq 12$ MHz	−40 to 110 °C	+5.0 V ±10 %

3

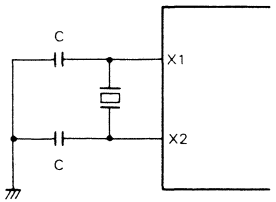
CAPACITANCE (T_a = 25 °C, V_{DD} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_I	f_C = 1 MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins are			20	pF
I/O Capacitance	C_{IO}	connected to 0V			20	pF

DC CHARACTERISTICS (T_a = −40 to +110 °C, V_{DD} = +5.0 V ±10 %, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Voltage Low	V_{IL1}	Except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7		0		0.7	V
	V_{IL2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7		0		0.2 V_{DD}	V
Input Voltage High	V_{IH1}	Except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7, X1, X2		2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7, X1, X2 *1		0.8 V_{DD}		V_{DD}	V
Output Voltage Low	V_{OL}	I_{OL}=2.0 mA				0.45	V
Output Voltage High	V_{OH}	I_{OH}=−0.9 mA		V_{DD}−1.0			V
		I_{OH}=−100 μA		V_{DD}−0.5			V
Input Current	I_I	INT1, T1 (PC3); 0 V ≦ V_I ≦ V_{DD}				±200	μA
Input Leakage Current	I_{L1}	Except INT1, TI (PC3); 0 V ≦ V_I ≦ V_{DD}				±10	μA
Output Leakage Current	I_{LO}	0 V ≦ V_O ≦ V_{DD}				±10	μA
AV_{DD} Supply Current	AI_{DD1}				0.3	1.0	mA
	AI_{DD2}	STOP mode			10	20	μA
V_{DD} Supply Current	I_{DD1}	Operating mode f=12 MHz			12 *2	20	mA
	I_{DD2}	HALT mode f=12 MHz			5 *2	10	mA
Data Retention Voltage	V_{DDDR}	Hardware/software STOP mode		2.5			V
Data Retention Current	I_{DDDR}	Hardware/ software STOP mode	V_{DDDR}=2.5 V		1	75	μA
			V_{DDDR}=5 V±10 %		10	250	μA

*1 The following oscillation circuit using crystal is recommended.



C=10 pF

*2 T_a = +25 °C, V_{DD} = 5 V

AC CHARACTERISTICS

(T_a=−40 to +110 °C, V_{DD}=+5.0 V±10 %, V_{SS}=0 V, f_{XTAL}=12 MHz)

READ/WRITE OPERATION

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
X1 Input Cycle Time	t_{CYC}	*1	83	250	ns
Address Setup to ALE↓	t_{AL}	*2	65		ns
Address Hold from ALE↓	t_{LA}	*2	50		ns
Address to $\overline{RD}$↓ Delay Time	t_{AR}	*2	150		ns
$\overline{RD}$↓ to Address Floating	t_{AFR}	*2		20	ns
Address to Data Input	t_{AD}	*2		360	ns
ALE↓ to Data Input	t_{LDR}	*2		215	ns
$\overline{RD}$↓ to Data Input	t_{RD}	*2		180	ns
ALE↓ to $\overline{RD}$↓ Delay Time	t_{LR}	*2	35		ns
Data Hold Time from $\overline{RD}$↑	t_{RDH}	*2	0		ns
$\overline{RD}$↑ to ALE↑ Delay Time	t_{RL}	*2	115		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read, *2	280		ns
		OP Code Fetch, *2	530		ns
ALE Width High	t_{LL}	*2	125		ns
$\overline{M1}$ Setup Time to ALE↓	t_{ML}		65		ns
$\overline{M1}$ Hold Time from ALE↓	t_{LM}		50		ns
$\overline{IO}$/M Setup Time to ALE↓	t_{IL}		65		ns
$\overline{IO}$/M Hold Time from ALE↓	t_{LI}		50		ns
Address to $\overline{WR}$↓ Delay	t_{AW}	*2	150		ns
ALE↓ to Data Output	t_{LDW}	*2		195	ns
$\overline{WR}$↓ to Data Output	t_{WD}	*2		100	ns
ALE↓ to $\overline{WR}$↓ Delay	t_{LW}	*2	35		ns
Data Setup Time to $\overline{WR}$↑	t_{DW}	*2	230		ns
Data Hold Time from $\overline{WR}$↑	t_{WDH}	*2	95		ns
$\overline{WR}$↑ to ALE↑ Delay Time	t_{WL}	*2	115		ns
$\overline{WR}$ Width Low	t_{WW}	*2	280		ns

*1 Cycle time $t_{CYC} = 1/f_{XTAL}$

*2 Load capacitance: C_L = 100 pF

3

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*1	1		μs
			*2	500		ns
		$\overline{SCK}$ Output		2		ns
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*1	420		ns
			*2	200		ns
		$\overline{SCK}$ Output		900		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*1	420		ns
			*2	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$↑	t_{RXK}	*1		80		ns
RxD Hold Time from $\overline{SCK}$↑	t_{KRX}	*1		80		ns
$\overline{SCK}$↓ to TxD Delay Time	t_{KTX}	*1			210	ns

*1 1 x Baud rate in asynchronous, synchronous, I/O interface mode

*2 16 x, 64 x Baud rate in asynchronous

A/D CONVERTER CHARACTERISTICS

(T_a = −40 to +110 °C, V_{DD} = +5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V
V_{DD}−0.5 V ≦ AV_{DD} ≦ V_{DD}, 4.0 V ≦ V_{AREF} ≦ AV_{DD})

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Resolution			8			Bits
Absolute Accuracy		T_a=−10 to +70 °C, ns ≦ t_{CYC} ≦ 170 ns			0.4 %±1/2	LSB
		83 ns ≦ t_{CYC} ≦ 170 ns, T_a=−40 to +85 °C			0.6 %±1/2	LSB
		3.4 V ≦ V_{AREF} ≦ AV_{DD}, 83 ns ≦ t_{CYC} ≦ 170 ns			0.8 %±1/2	LSB
Conversion Time	t_{CONV}	83 ns ≦ t_{CYC} ≦ 110 ns	576			t_{CYC}
		110 ns ≦ t_{CYC} ≦ 170 ns	432			t_{CYC}
Sampling Time	t_{SAMP}	83 ns ≦ t_{CYC} ≦ 110 ns	96			t_{CYC}
		110 ns ≦ t_{CYC} ≦ 170 ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1 000		MΩ
Reference Voltage	V_{AREF}		AV_{CC}−0.5		AV_{CC}	V
V_{AREF} Current	I_{AREF1}			1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} Current	I_{AVDD1}			0.3	1.0	mA
	I_{AVDD2}	STOP mode		10	20	μA

ZERO-CROSS CHARACTERISTICS

(T_a=−40 to +110 °C, V_{CC}=+5.0 V±10 % V_{SS}=0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		±135	mV
ZERO-Cross Detection Input Frequency	f_{ZX}		0.05	1	kHz

OTHER OPERATIONS

(T_a=−40 °C to +110 °C, V_{CC}=+5.0 V±10 %, V_{SS}=0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
TI Width High, Low	t_{TIH},t_{TIL}		6		t_{CYC}
CI Width High, Low	t_{CI1H},t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H},t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ Width High, Low	t_{NIH},t_{NIL}		10		t_{CYC}
INT1 Width High, Low	t_{I1H},t_{I1L}		36		t_{CYC}
INT2 Width High, Low	t_{I2H},t_{I2L}		36		t_{CYC}
RESET Width High, Low	t_{RSH},t_{RSL}		10		t_{CYC}

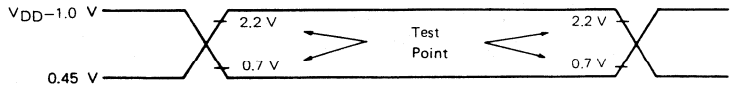
3

EXTERNAL CLOCK TIMING

(T_a=−40 °C to +110 °C, V_{DD}=+5.0 V±10 %, V_{SS}=0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
X1 Input Width High	$t_{\phi H}$		30	250	ns
X1 Input Width Low	$t_{\phi L}$		30	250	ns
X1 Input Rise Time	t_r		0	30	ns
X1 Input Fall Time	t_f		0	30	ns

AC TIMING MESURMENT POINT



BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNIT
t_{AL}	2T – 100	MIN.	ns
t_{LA}	T – 30	MIN.	ns
t_{AR}	3T – 100	MIN.	ns
t_{AD}	7T – 220	MAX.	ns
t_{LDR}	5T – 200	MAX.	ns
t_{RD}	4T – 150	MAX.	ns
t_{LR}	T – 50	MIN.	ns
t_{RL}	2T – 50	MIN.	ns
t_{RR}	4T – 50 (Data Read)	MIN.	ns
	7T – 50 (OP Code Fetch)		
t_{LL}	2T – 40	MIN.	ns
t_{ML}(1)	2T – 100	MIN.	ns
t_{LM}(1)	T – 30	MIN.	ns
t_{IL}(2)	2T – 100	MIN.	ns
t_{LI}(2)	T – 30	MIN.	ns
t_{AW}	3T – 100	MIN.	ns
t_{LDW}	T + 110	MAX.	ns
t_{LW}	T – 50	MIN.	ns
t_{DW}	4T – 100	MIN.	ns
t_{WDH}	2T – 70	MIN.	ns
t_{WL}	2T – 50	MIN.	ns
t_{WW}	4T – 50	MIN.	ns
t_{CYK}	12T ($\overline{SCK}$ Input)(3)	MIN.	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	5T + 5($\overline{SCK}$ Input)(3)	MIN.	ns
	12T – 100 ($\overline{SCK}$ Output)		
t_{KKH}	5T + 5($\overline{SCK}$ Input)(3)	MIN.	ns
	12T – 100 ($\overline{SCK}$ Output)		

NOTE: (1) MODE0, MODE1 pins are connected to V_{CC} through R.

(2) MODE0, MODE1 pins are connected to V_{CC} thorugh R in μPD7810.

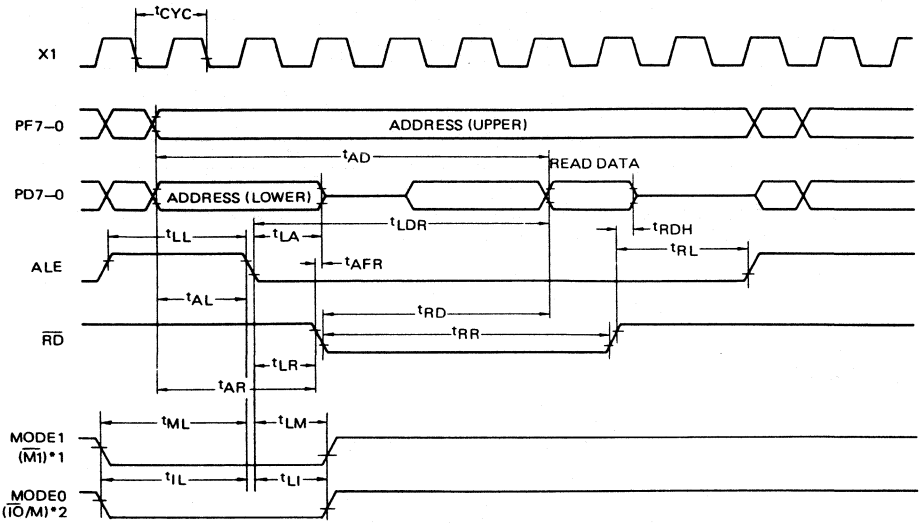
(3) 1x Baud Rate in Asynchronous, Synchronous, I/O interface Mode

(4) $T = t_{CYC} = 1/f_{XTAL}$

(5) The items not in this table are not dependent on f_{XTAL}.

TIMING WAVEFORM

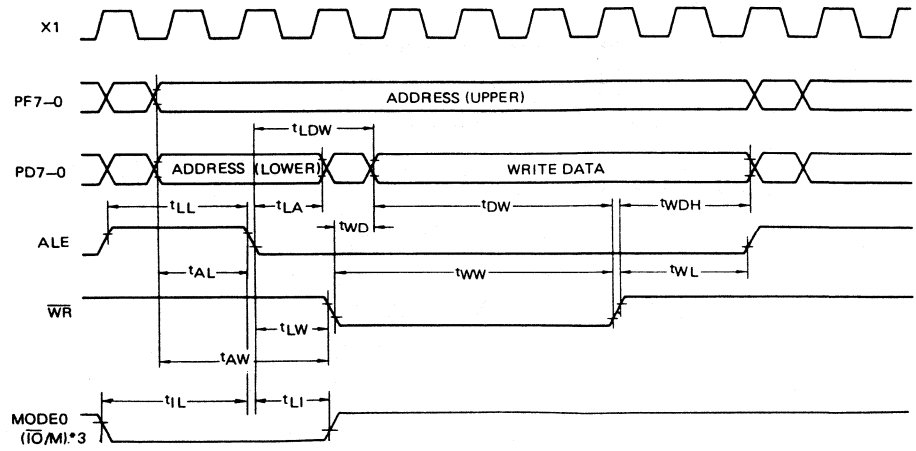
Read Operation



*1 $\overline{M1}$ is output at the fetch cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

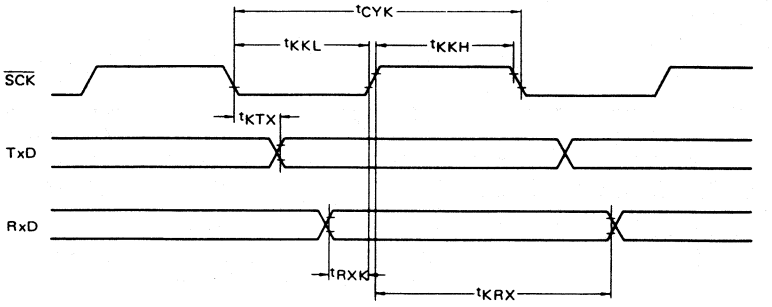
*2 $\overline{IO}$/M is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Write Operation

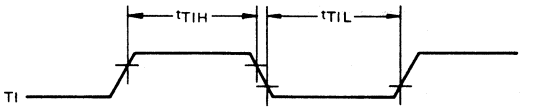


*3 $\overline{IO}$/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Serial Operation

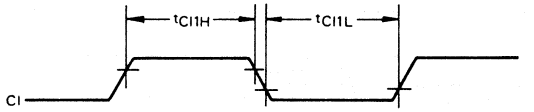


Timer Input Timing

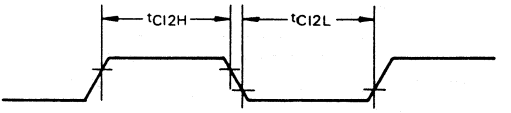


Timer/Event Counter Input Timing

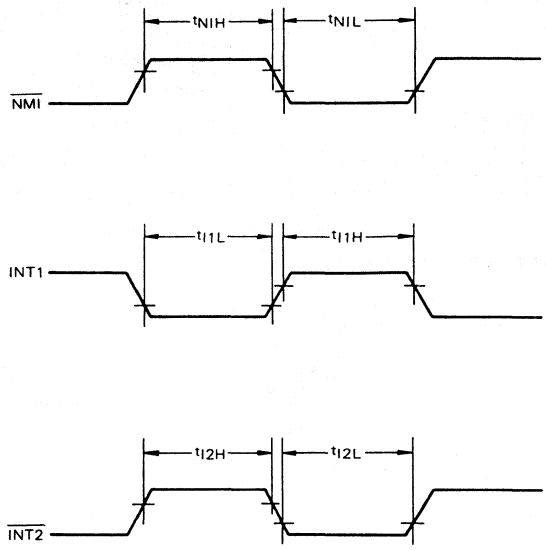
Event Count Mode:



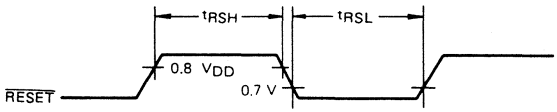
Pulse Width Measurement Mode:



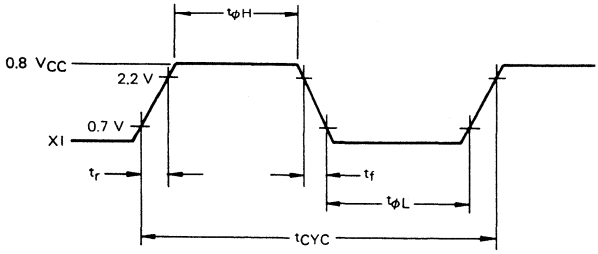
Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



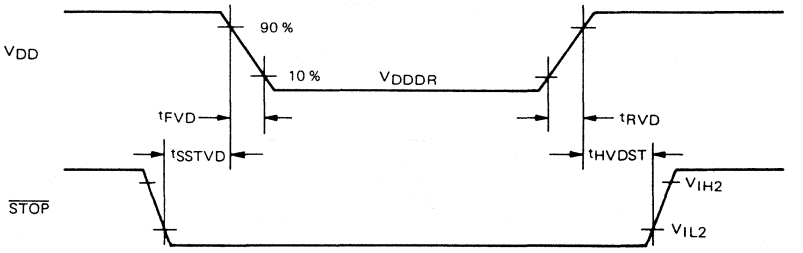
External Clock Timing



STOP MODE LOW VOLTAGE DATA RETENTION CHARACTERISTICS (T_a=−40 to +110 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	V_{DDDR}		2.5		5.5	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR}=2.5 V		1	75	μA
		V_{DDDR}=5 V ±10 %		15	250	μA
V_{DD} Rise and Fall Time	t_{RVD}, t_{FVD}		200			μs
$\overline{STOP}$ Setup Time to V_{DD}↓	t_{SSTVD}		12T+0.5			μs
$\overline{STOP}$ Hold Time after V_{DD}↑	t_{HVDST}		12T+0.5			μs

DATA RETENTION MODE TIMING



ELECTRICAL SPECIFICATIONS FOR AUTOMOTIVE TEMPERATURE RANGE

ABSOLUTE MAXIMUM (T_a = 25 °C)

PARAMETER	SYMBOL	TEST CONDITION	RATINGS	UNIT
Power Supply Voltage	V_{DD}		−0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD}+0.5	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to V_{DD}+0.5	V
Output Voltage	V_O		−0.5 to V_{DD}+0.5	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−2.0	mA
		All Output Pin Total	−50	mA
Reference Input Voltage	V_{AREF}		−0.5 to AV_{DD}+0.3	V
Operating Temperature	T_{OPT}	$f_{XTAL} \leqq 12$ MHz	−40 to +85	°C
Storage Temperature	T_{STG}		−65 to +150	°C

OPERATING CONDITION

PARAMETER / OSC. FREQ.	T_a	V_{DD}, AV_{DD}
$f_{XTAL} \leqq 12$ MHz	−40 to 85 °C	+5.0 V ±10 %

3

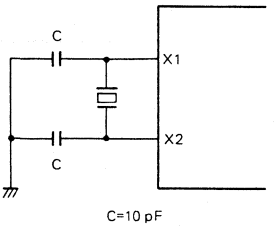
CAPACITANCE (T_a = 25 °C, V_{DD} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_I	f_C = 1 MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins are			20	pF
I/O Capacitance	C_{IO}	connected to 0V			20	pF

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = +5.0 V ±10 %, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Voltage	V_{IL1}	Except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7		0		0.8	V
	V_{IL2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7		0		0.2 V_{DD}	V
Input Voltage High	V_{IH1}	Except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7, X1, X2		2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7, X1, X2 *1		0.8 V_{DD}		V_{DD}	V
Output Voltage Low	V_{OL}	I_{OL}=2.0 mA				0.45	V
Output Voltage High	V_{OH}	I_{OH}=−1.0 mA		V_{DD}−1.0			V
		I_{OH}=−100 μA		V_{DD}−0.5			V
Input Current	I_I	INT1, T1 (PC3); 0 V ≦ V_I ≦ V_{DD}				±200	μA
Input Leakage Current	I_{LI}	Except INT1, T1 (PC3) 0 V ≦ V_I ≦ V_{DD}				±10	μA
Output Leakage Current	I_{LO}	0 V ≦ V_O ≦ V_{DD}				±10	μA
AV_{DD} Supply Current	AI_{DD1}	f=15 MHz			0.5	1.3	mA
	AI_{DD2}	STOP mode			10	20	μA
V_{DD} Supply Current	I_{DD1}	Operating mode f = 12 MHz			16 *2	30	mA
	I_{DD2}	HALT mode f = 12 MHz			8 *2	15	mA
Data Retention Voltage	V_{DDDR}	Hardware/software STOP mode		2.5			V
Data Retention Current	I_{DDDR}	Hardware/ software STOP mode	V_{DDDR}=2.5 V		1	15	μA
			V_{DDDR}=5 V±10 %		10	50	μA

*1 The following oscillation circuit using crystal is recommended.



C=10 pF

*2 T_a = +25 °C, V_{DD} = 5 V

AC CHARACTERISTICS

(T_a=−40 to +85 °C, V_{DD}=+5.0 V±10 %, V_{SS}=0 V, f_{XTAL}=12 MHz)

READ/WRITE OPERATION

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
X1 Input Cycle Time	t_{CYC}	*1	66	250	ns
Address Setup to ALE↓	t_{AL}	*2	30		ns
Address Hold from ALE↓	t_{LA}	*2	35		ns
Address to $\overline{RD}$↓ Delay Time	t_{AR}	*2	100		ns
$\overline{RD}$↓ to Address Floating	t_{AFR}	*2		20	ns
Address to Data Input	t_{AD}	*2		250	ns
ALE↓ to Data Input	t_{LDR}	*2		135	ns
$\overline{RD}$↓ to Data Input	t_{RD}	*2		120	ns
ALE↓ to $\overline{RD}$↓ Delay Time	t_{LR}	*2	15		ns
Data Hold Time from $\overline{RD}$↑	t_{RDH}	*2	0		ns
$\overline{RD}$↑ to ALE↑ Delay Time	t_{RL}	*2	80		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read, *2	215		ns
		OP Code Fetch, *2	415		ns
ALE Width High	t_{LL}	*2	90		ns
$\overline{M1}$ Setup Time to ALE↓	t_{ML}		30		ns
$\overline{M1}$ Hold Time from ALE↓	t_{LM}		35		ns
$\overline{IO}$/M Setup Time to ALE↓	t_{IL}		30		ns
$\overline{IO}$/M Hold Time from ALE↓	t_{LI}		35		ns
Address to $\overline{WR}$↓ Delay	t_{AW}	*2	100		ns
ALE↓ to Data Output	t_{LDW}	*2		180	ns
$\overline{WR}$↓ to Data Output	t_{WD}	*2		100	ns
ALE↓ to $\overline{WR}$↓ Delay	t_{LW}	*2	15		ns
Data Setup Time to $\overline{WR}$↑	t_{DW}	*2	165		ns
Data Hold Time from $\overline{WR}$↑	t_{WDH}	*2	60		ns
$\overline{WR}$↑ to ALE↑ Delay Time	t_{WL}	*2	80		ns
$\overline{WR}$ Width Low	t_{WW}	*2	215		ns

*1 Cycle time $t_{CYC} = 1/f_{XTAL}$

*2 Load capacitance: C_L = 150 pF

3

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*1	800		ns
			*2	400		ns
		$\overline{SCK}$ Output		1.6		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*1	335		ns
			*2	160		ns
		$\overline{SCK}$ Output		700		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*1	335		ns
			*2	160		ns
		$\overline{SCK}$ Output		700		ns
RxD Setup Time to $\overline{SCK}$↑	t_{RXK}	*1		80		ns
RxD Hold Time from $\overline{SCK}$↑	t_{KRX}	*1		80		ns
$\overline{SCK}$↓ to TxD Delay Time	t_{KTX}	*1			210	ns

*1 1 x Baud rate in asynchronous, synchronous, I/O interface mode

*2 16 x, 64 x Baud rate in asynchronous

A/D CONVERTER CHARACTERISTICS

(T_a = −40 to +85 °C, V_{DD} = +5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V

V_{DD}−0.5 V ≦ AV_{DD} ≦ V_{DD}, 3.4 V ≦ V_{AREF} ≦ AV_{DD})

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Resolution			8			Bits
Absolute Accuracy		T_a=−10 to +70 °C 4.0 ≦ V_{AREF} ≦ AV_{DD} 66 ns ≦ t_{CYC} ≦ 170 ns			0.4 %±1/2	LSB
		66 ns ≦ t_{CYC} ≦ 170 ns 4.0 V ≦ V_{AREF} ≦ AV_{DD}			0.6 %±1/2	LSB
		66 ns ≦ t_{CYC} ≦ 170 ns			0.8 %±1/2	LSB
Conversion Time	t_{CONV}	66 ns ≦ t_{CYC} ≦ 110 ns	576			t_{CYC}
		110 ns ≦ t_{CYC} ≦ 170 ns	432			t_{CYC}
Sampling Time	t_{SAMP}	66 ns ≦ t_{CYC} ≦ 110 ns	96			t_{CYC}
		110 ns ≦ t_{CYC} ≦ 170 ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1 000		MΩ
Reference Voltage	V_{AREF}		3.4		AV_{CC}	V
V_{AREF} Current	I_{AREF}	Operating mode		1.5	3.0	mA
		Stop mode		0.7	1.5	mA

ZERO-CROSS CHARACTERISTICS

(T_a=−40 to +85 °C, V_{CC}=+5.0 V±10 %, V_{SS}=0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		±135	mV
ZERO-Cross Detection Input Frequency	f_{ZX}		0.05	1	kHz

OTHER OPERATIONS

(T_a=−40 °C to +85 °C, V_{CC}=+5.0 V±10 %, V_{SS}=0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
TI Width High, Low	t_{TIH},t_{TIL}		6		t_{CYC}
CI Width High, Low	t_{CI1H},t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H},t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ Width High, Low	t_{NIH},t_{NIL}		10		t_{CYC}
INT1 Width High, Low	t_{I1H},t_{I1L}		36		t_{CYC}
INT2 Width High, Low	t_{I2H},t_{I2L}		36		t_{CYC}
RESET Width High, Low	t_{RSH},t_{RSL}		10		t_{CYC}

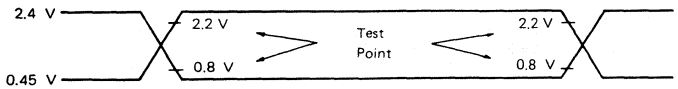
3

EXTERNAL CLOCK TIMING

(T_a=−40 °C to +85 °C, V_{DD}=+5.0 V±10 %, V_{SS}=0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
X1 Input Width High	$t_{\phi H}$		20	250	ns
X1 Input Width Low	$t_{\phi L}$		20	250	ns
X1 Input Rise Time	t_r		0	20	ns
X1 Input Fall Time	t_f		0	20	ns

AC TIMING MESURMENT POINT



BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNIT
t_{AL}	2T – 100	MIN.	ns
t_{LA}	T – 30	MIN.	ns
t_{AR}	3T – 100	MIN.	ns
t_{AD}	7T – 220	MAX.	ns
t_{LDR}	5T – 200	MAX.	ns
t_{RD}	4T – 150	MAX.	ns
t_{LR}	T – 50	MIN.	ns
t_{RL}	2T – 50	MIN.	ns
t_{RR}	4T – 50 (Data Read)	MIN.	ns
	7T – 50 (OP Code Fetch)		
t_{LL}	2T – 40	MIN.	ns
t_{ML}	2T – 100	MIN.	ns
t_{LM}	T – 30	MIN.	ns
t_{IL}	2T – 100	MIN.	ns
t_{LI}	T – 30	MIN.	ns
t_{AW}	3T – 100	MIN.	ns
t_{LDW}	T + 110	MAX.	ns
t_{LW}	T – 50	MIN.	ns
t_{DW}	4T – 100	MIN.	ns
t_{WDH}	2T – 70	MIN.	ns
t_{WL}	2T – 50	MIN.	ns
t_{WW}	4T – 50	MIN.	ns
t_{CYK}	12T ($\overline{SCK}$ Input)(1)	MIN.	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	5T + 5($\overline{SCK}$ Input)(1)	MIN.	ns
	12T – 100 ($\overline{SCK}$ Output)		
t_{KKH}	5T + 5($\overline{SCK}$ Input)(1)	MIN.	ns
	12T – 100 ($\overline{SCK}$ Output)		

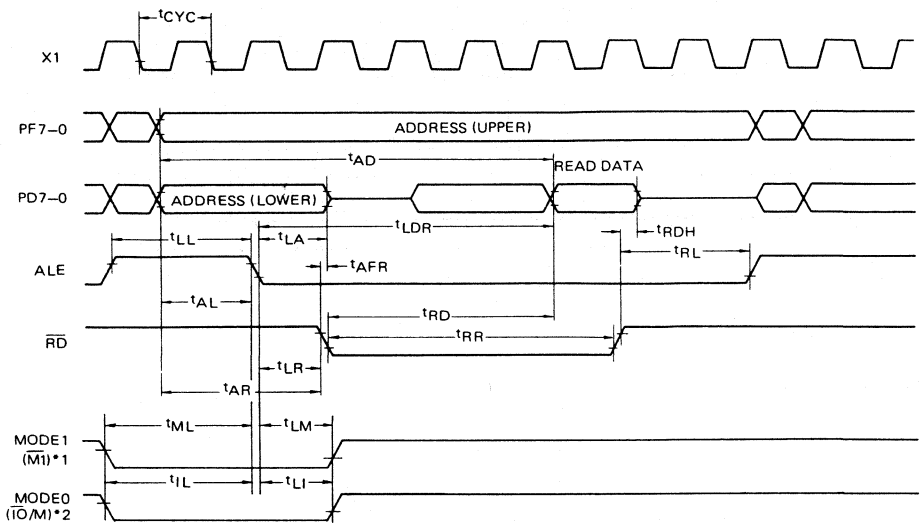
NOTE: (1) 1x Baud Rate in Asynchronous, Synchronous, I/O interface Mode

(2) $T = t_{CYC} = 1/f_{XTAL}$

(3) The items **not in** this table are not dependent on f_{XTAL}.

TIMING WAVEFORM

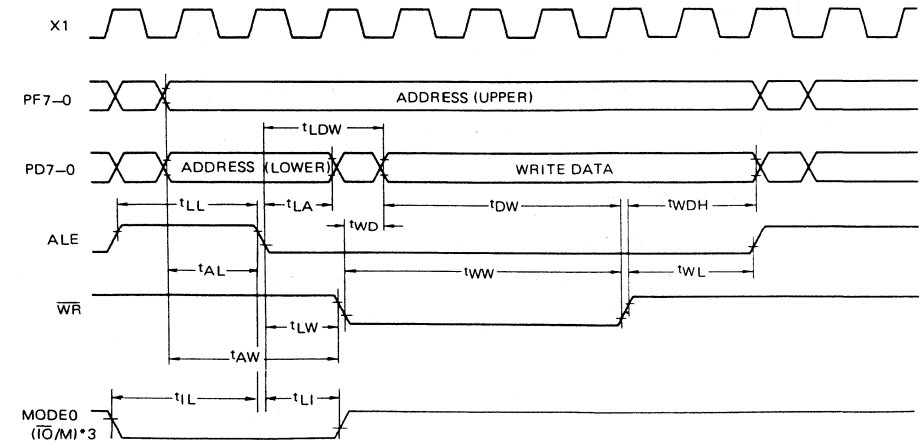
Read Operation



*1 $\overline{M_1}$ is output at the fetech cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

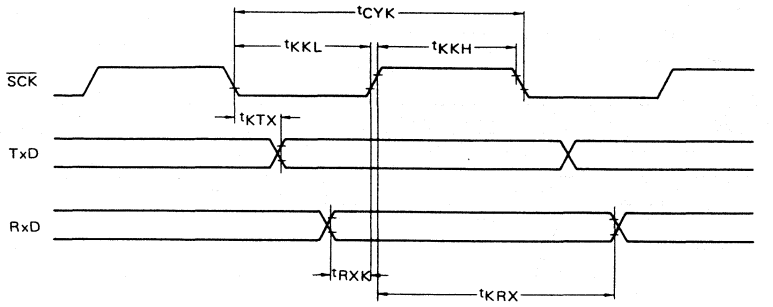
*2 $\overline{IO}$/M is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Write Operation

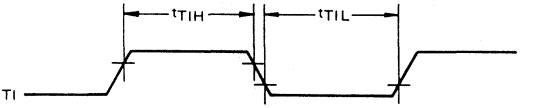


*3 $\overline{IO}$/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Serial Operation

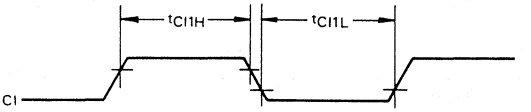


Timer Input Timing

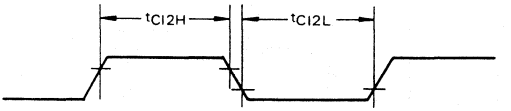


Timer/Event Counter Input Timing

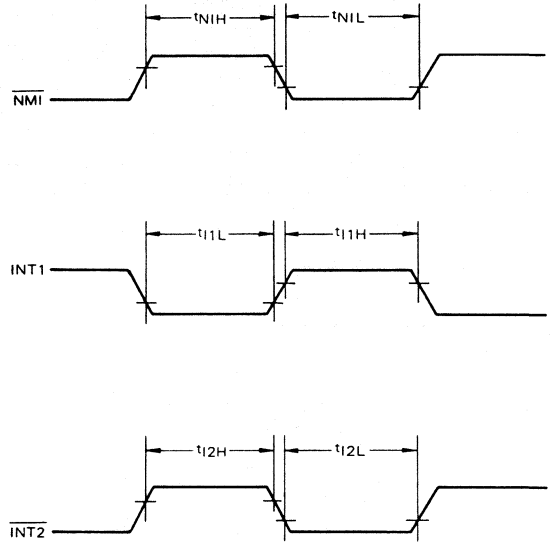
Event Count Mode:



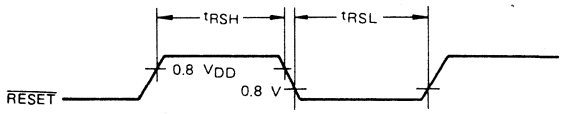
Pulse Width Measurement Mode:



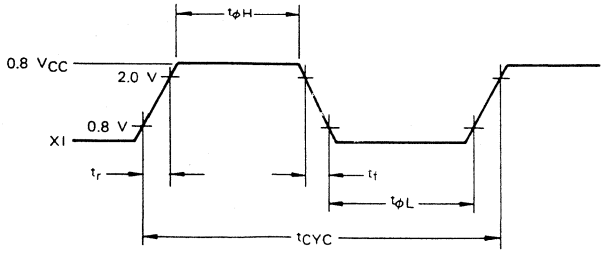
Interrupt Input Timing



RESET Input Timing



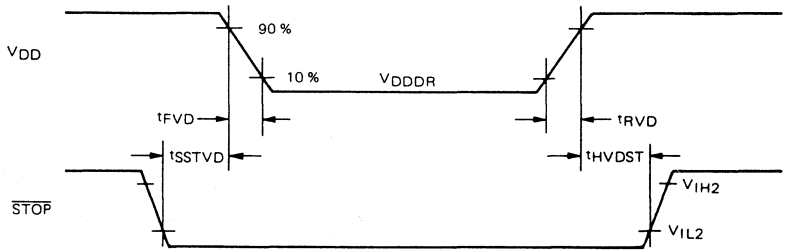
External Clock Timing



STOP MODE LOW VOLTAGE DATA RETENTION CHARACTERISTICS (T_a=−40 to +85 °C)

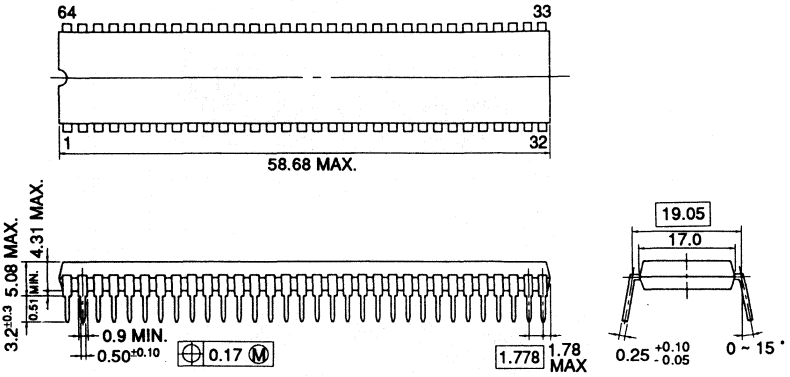
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	V_{DDDR}		2.5		5.5	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR}=2.5 V		1	15	μA
		V_{DDDR}=5 V ±10 %		15	50	μA
V_{DD} Rise and Fall Time	t_{RVD}, t_{FVD}		200			μs
$\overline{STOP}$ Setup Time to V_{DD}↓	t_{SSTVD}		12T+0.5			μs
$\overline{STOP}$ Hold Time after V_{DD}↑	t_{HVDST}		12T+0.5			μs

DATA RETENTION MODE TIMING

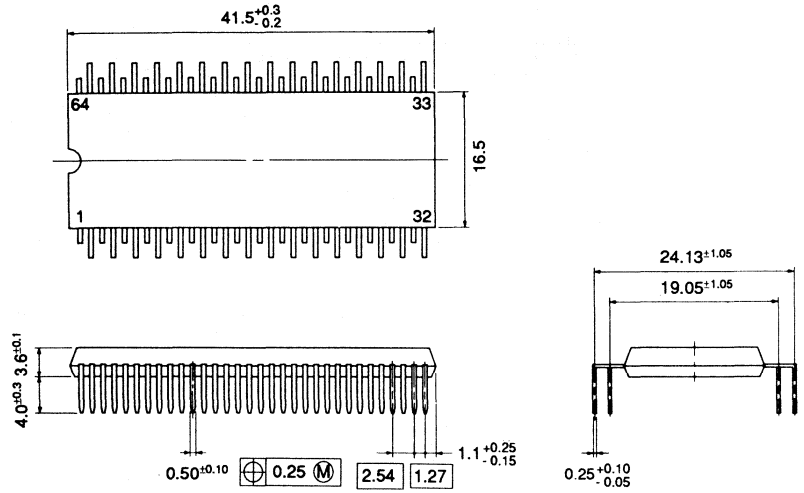


Package Dimensions

64 - Pin SDIP

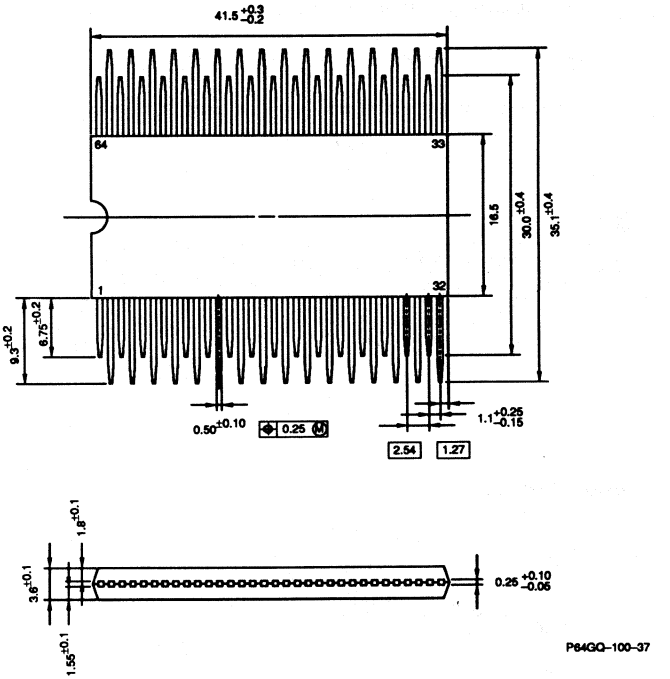


64 - Pin QUIP (Bent Leads)

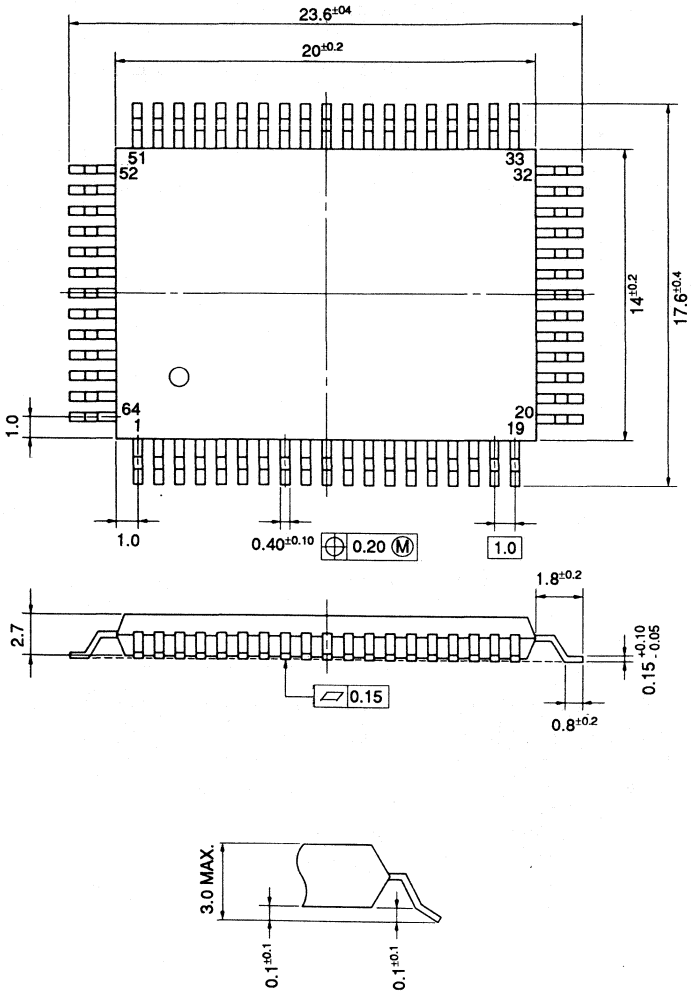


3

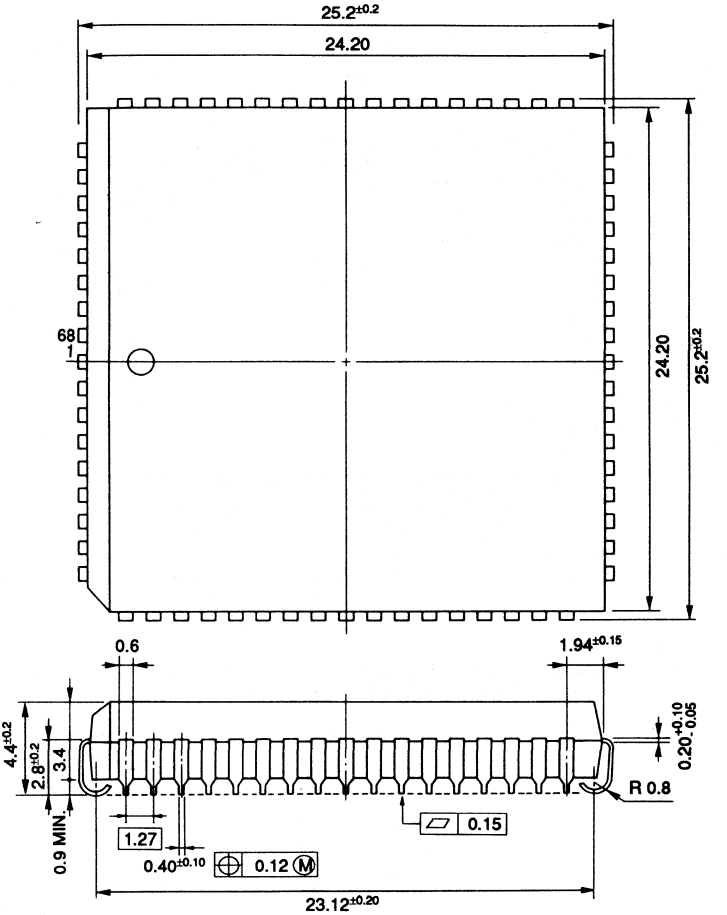
64 PIN PLASTIC
QUIP STRAIGHT LEADS
PACKAGE DIMENSIONS
(Units: mm)



64 - Pin FLAT PACK



68 - Pin PLCC

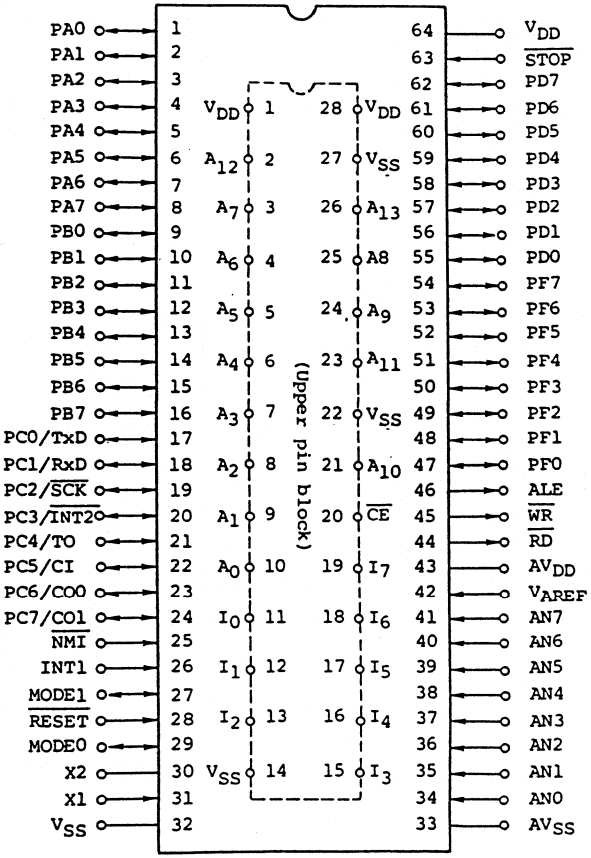

25.2±0.2
24.20
68
1
24.20
25.2±0.2
0.6
1.94±0.15
4.4±0.2
2.8±0.2
3.4
0.9 MIN.
0.20+0.10 -0.05
R 0.8
1.27
0.40±0.10
0.12 M
0.15
23.12±0.20

The μPD78CG14 is an 8-bit microcomputer that can mount a standard EPROM (27C256/27C256A) in a piggyback configuration for program memory.
The μPD78CG14 is pin-compatible with the QUIP-version μPD78C11G/78C14G single-chip, 8-bit microcomputer that has on-chip mask-programable ROM.

Features

- ❒ Compatible with μPD78C11G/78C14G (QUIP version).
- ❒ Piggyback memory options are available from 4K to 16K byte by software.
- ❒ Program memory addressing Space: 65280 X 8 bits.
- ❒ Internal RAM capacity: 256 X 8 bits.
- ❒ Standby function: HALT mode, hardware/software STOP mode.
- ❒ CMOS
- ❒ Single + 5V power supply (5V ±10%)

Pin Configuration (Top view)



3

DIFFERENCE BETWEEN μPD78CG14 AND μPD78C1x/78C1xA

Item	μPD78CG14	μPD78C14	μPD78C11	μPD78C11A	μPD78C12A
Internal ROM capacity		• Mask ROM • 0000H-3FFFH • 16, 384 x 8 bits	• Mask ROM • 0000H-0FFFH • 4, 096 x 8 bits		• Mask ROM • 0000H-1FFFH • 8, 192 x 8 bits
External memory area	Up to 65, 536 x 8 bits (however, area of 16, 384 x 8 bits is piggyback EPROM)	Up to 48, 752 x 8 bits	Up to 61, 440 x 8 bits		Up to 57, 344 x 8 bits
MM register	• 8-bit • EPROM capacitance can be switched by upper two bits.	• 4-bit • Not provided with the corresponding to upper two bits (MM7) and MM6 bit) in μPD78CG14.			
Low supply voltage data holt function	Not provided	Provided			
Pull-up resistor mask option (PA, PB, PC)	Not provided	Not provided		Not provided	
Package	64-pin piggyback QUIP (the lower pin block is compatible with μPD78C14/C11)	64-pin plastic shrink DIP 64-pin plastic QUIP 64-pin plastic QUIP 64-pin plastic flatpack (bent leads)			

Note: For detail of the μPD78CG14 CPU functions and internal hardware, refer to the μCOM-87AD, μPD78C11 User's Manuals, etc.

Electrical Characteristics

Absolute Maximum Ratings (Ta = 25 °C)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Power Supply Voltage	V_{DD}		−0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD} + 0.5	V
	AV_{SS}		−0.5 to + 0.5	V
Input Voltage	V_I		−0.5 to V_{DD} + 0.5	V
Output Voltage	V_O		−0.5 to V_{DD} + 0.5	V
Output Current Low	I_{OL}	All Output Pins	4.0	mA
		All Output Pins Total	100	mA
Output Current High	I_{OH}	All Output Pins	−2.0	mA
		All Output Pins Total	−50	mA
Reference Input Voltage	V_{AREF}		−0.5 to AV_{DD} + 0.3	V
Operating Temperature	T_{opt}	$f_{XTAL} \leq$ 12MHz	−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

Recommended Operating Conditions:

Parameter / OSC frequency	Ta	V_{DD}, AV_{DD}
$f_{XTAL} \leq$ 15MHz	−40 °C to + 85 °C	+ 5.0V ±10%

DC Characteristics (T_a = −40 to +85°C, V_{DD} = AV_{DD} = +5.0V ± 10%; V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL1}	All except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$ $\overline{SCK}$, INT1, T1, and AN4-AN7	0		0.8	V
	V_{IL2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1 T1, and AN4-AN7	0		$0.2V_{DD}$	V
Input High Voltage	V_{IH1}	All except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, and AN4-AN7, X1, and X2	2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1 T1, and AN4-AN7, X1, and X2	$0.8V_{DD}$		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = 2.0 mA	V_{DD} −1.0			V
		I_{OH} = −100μA	V_{DD} −0.5			V
Input Current	I_{I1}	INT1*1, TI (PC3); 0V ≤ V_I ≤ V_{DD}			±200	μA
	I_{I2}	I0-I7 (Upper I/P pin) V_I = 0			−300	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3); 0V ≤ V1 ≤ V_{DD}			±10	μA
Output Leakage Current	I_{LO}	0V ≤ V1 ≤ V_{DD}			±10	μA
AV_{DD} Supply Current	AI_{DD1}	f = 15 MHz		0.5	1.3	mA
V_{DD} Supply Current	I_{DD1}	Operation Mode f = 15 MHz		16	30	mA
	I_{DD2}	HALT Mode f = 15 MHz		8	15	mA
Data Retention Voltage	V_{DDDR}	Hardware/Software STOP Mode,	2.5			V
Data Retention Current	I_{DDDR}	Hardware/Software STOP mode **see Note; V_{DDR} =2.5V		1	15	μA
		Hardware/Software STOP mode **see Note; V_{DDDR}=5V±10%		10	50	μA
Supply Current	AI_{DD2}	STOP Mode		10	20	μA

Note: When Self-Bias not generated.

3

AC Characteristics (T_a = −40 to +85°C, V_{DD} = +5.0V ± 10%; V_{SS} = 0V)
Read/Write Operation

Item	Symbol	Condition	MIN	MAX	UNIT
X1 Input Cycle Time	t_{CYC}		66	250	ns
Address Setup to ALE ↓	t_{AL}	*3, *4	30		ns
Address Hold after ALE↓	t_{LA}	*3, *4	35		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*3, *4	100		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*4		20	ns
Address to Data Input	t_{AD}	*3, *4		250	ns
ALE ↓ to Data Input	tL_{DR}	*3, *4		135	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*3, *4		120	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*3, *4	15		ns
Data Hold after $\overline{RD}$ ↑	t_{RDH}	*4	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*3, *4	80		ns
$\overline{RD}$ with low	t_{RR}	Data Read, *3, *4	215		ns
		OP code Fetch, *3, *4	415		ns
ALE high-level width	t_{LL}	*3, *4	90		ns
$\overline{M1}$ Setup Time ALE ↓	t_{ML}	*3	30		ns
$\overline{M1}$ Hold Time after ALE ↓	t_{LM}	*3	35		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*3	30		ns
$\overline{IO}$/M Hold Time after ALE ↓	t_{LI}	*3	35		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*3, *4	100		ns
ALE ↓ to Data Output	t_{LDW}	*3, *4		180	ns
$\overline{WR}$ ↓ to Data Ouput	t_{WD}	*4		100	ns
ALE to $\overline{WR}$ ↓ Delay	t_{LW}	*3, *4	15		ns
Data Setup Time to $\overline{WR}$ ↑	t_{LW}	*3, *4	165		ns
Data Hold Time to $\overline{WR}$ ↑	t_{DW}	*3, *4	60		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*3, *4	80		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *4	215		ns
Data Input Delay Time from Address	t_{ACC}	*4		250	ns
Data Input Hold Time from Address	t_{IH}	*4	0		ns

Serial Operation

Parameter	Symbol	Condition		MIN	MAX	UNIT
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ input	*5	800		ns
			*6	400		ns
		$\overline{SCK}$ output		1.6		ns
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ input	*5	335		ns
			*6	160		ns
		$\overline{SCK}$ output		700		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ input	*5	335		ns
			*6	160		ns
		$\overline{SCK}$ output		700		ns
RxD Setup Time to $\overline{SCK}\uparrow$	t_{RXK}	*5		80		ns
RxD Hold Time to $\overline{SCK}\uparrow$	t_{KRX}	*5		80		ns
$\overline{SCK}\downarrow$ TxD Delay Time	t_{KTX}	*5			210	ns

A/D Converter Characteristics

(T_a = −40°C to +85°C, V_{DD} = 5.0V ± 10%, AV_{DD} = +5.0V ± 10%, V_{SS} = AV_{SS} = 0V, V_{DD} −0.5V ≤ AV_{DD} ≤ V_{DD}, 3.4V ≤ VA_{REF} ≤ AV_{DD})

Parameter	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Resolution			8			Bits
Absolute Accuracy *1		3.4V ≤ VA_{REF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.8	%FSR
		4.0V ≤ VA_{REF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.6	%FSR
		T_a = −10 to +70°C, 4.0V ≤ VA_{REF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.4	%FSR
Conversion time	t_{CONV}	66ns ≤ t_{CYC} ≤ 110ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling Time	t_{SAMP}	66ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
Reference Voltage	V_{AREF}		3.4		AV_{DD}	V
V_{AREF} Current	I_{AREF1}	Operation mode		1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} Supply Current	AI_{DD1}	Operation mode, f_{XX} = 15MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA

*1: Quantization Error (±1/2 LSB) is not included.

3

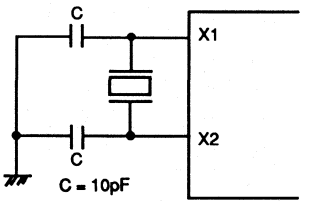
Zero Crossover Characteristics (T_a = −40 °C to +85 °C, V_{DD} = +5V ± 10%, V_{SS} = 0V)

Item	Symbol	Condition	MIN	MAX	UNIT
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{P-P}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		±135	mV
Zero-Cross Detection Input Frequency	f_{ZX}		0.05	1	kHz

Other Operations (T_a = −40 °C to +85 °C, V_{DD} = +5V ± 10%, V_{SS} = 0V)

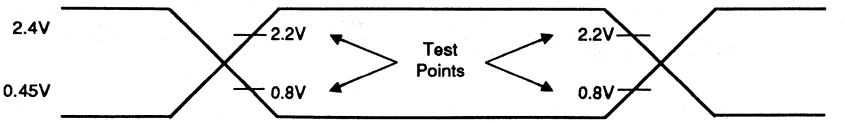
Item	Symbol	Condition	MIN	MAX	UNIT
TI high- and low-level widths	t_{TIH}, t_{TIL}		6		t_{CYC}
CI high- and low-level widths	t_{CI1H}, t_{CI1L}	Event counter mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse width measuring mode	48		t_{CYC}
$\overline{NMI}$ high- and low-level widths	t_{NIH}, t_{NIL}		10		μs
$\overline{INT1}$ high- and low-level widths	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ high- and low-level widths	t_{I2H}, t_{I2L}		36		t_{CYC}
$\overline{RESET}$ high- and low-level widths	t_{RSH}, t_{RSL}		10		μs

*1. For XTAL oscillation, following circuit is recommended.



*2. Ta = +25 °C, V_{DD} = 5V
*3. f_{XTAL} = 15 MHz
*4. Load Capacitance: C_L = 150pF
*5. x1 Clock Rate in Asynchronous Mode, Synchronous Mode, I/O Interface Mode
*6. x16, x64 Clock Rate in Asynchronous Mode

AC Timing Test Points



External Clock Timing (T_A = −40 °C to +85 °C, V_{DD} = +5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	MIN	MAX	UNIT
X1 input width high	t_{OH}		20	250	ns
X1 input width low	t_{OL}		20	250	ns
X1 input rise time	t_r		0	20	ns
X1 input fall time	t_f		0	20	ns

Bus Timing depending on t_{CYC}

Symbol	Calculating Expression	MIN./MAX.	UNIT
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220	MAX	ns
t_{LDR}	5T − 200	MAX	ns
t_{RD}	4T − 150	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read)	MIN	ns
	T − 50 (OP Code Fetch)		
t_{ML}	2T − 100	MIN	ns
t_{LM}	T − 30	MIN	ns
t_{IL}	2T − 100	MIN	ns
t_{LI}	T − 30	MIN	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50	MIN	ns
t_{CYK}	12T − (SCK Input) *1)	MIN	ns
	24T − (SCK Output)		
t_{KKL}	5T + 5 (SCK Input) *1	MIN	ns
	12T − 100 (SCK Output)		
t_{KKH}	5T + 5 (SCK Input) *2	MIN	ns
	12T − 100 (SCK Output)		
t_{ACC}	7T − 220	MAX	ns

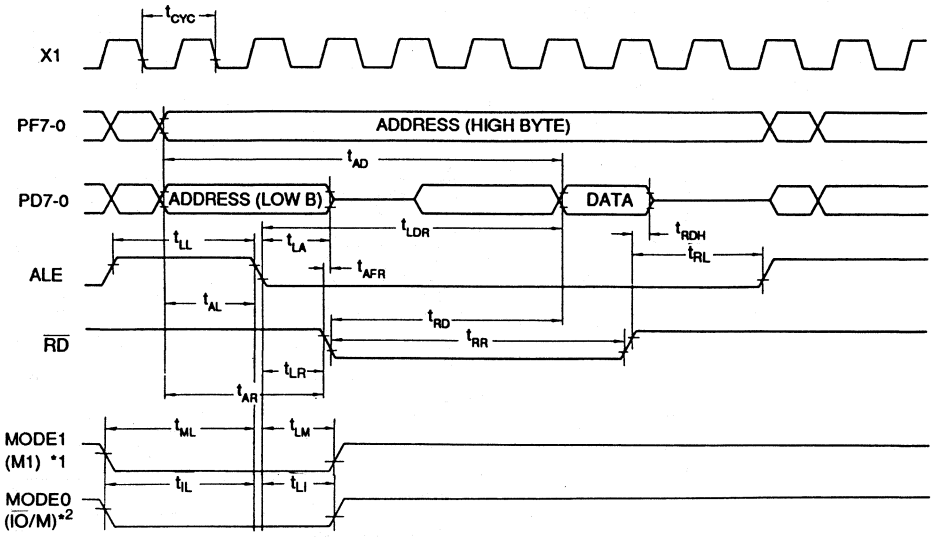
Note 1. In case of X1 clock rate in asynchronous mode, synchronous mode, or I/O interface mode.

2. $T = t_{CYC} = 1/f_{XTAL}$

3. Parameters which can't be found in this table don't depend on oscillation freuquency (f_{XTAL}).

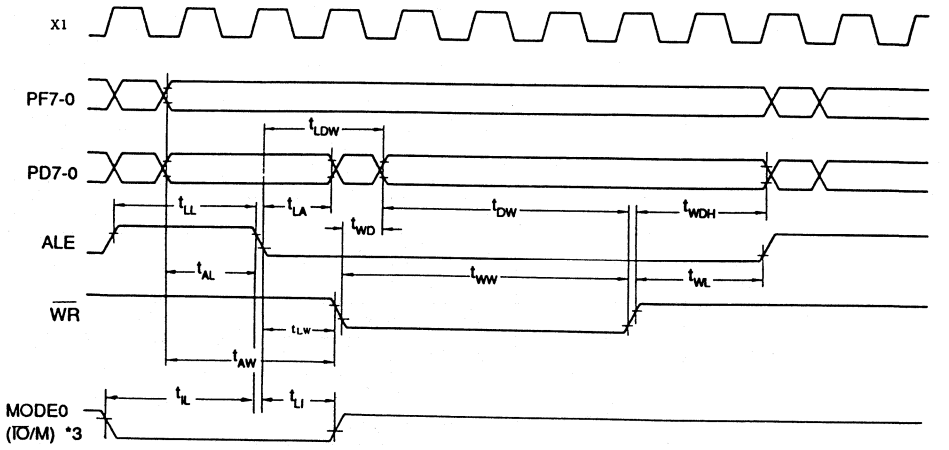
3

TIMING WAVEFORM
Read Operation



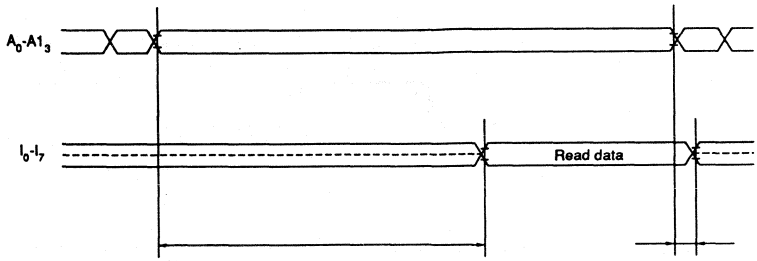
NOTE: 1. The $\overline{M1}$ signal is output through the MODE1 pin in the first opcode fetch cycle, if the MODE1 pin is pulled up.
2. The $\overline{IO/M}$ signal is output through the MODE0 pin in the sr to sr2 register read cycle, if the MODE0 pin is pulled up.

Write Operation

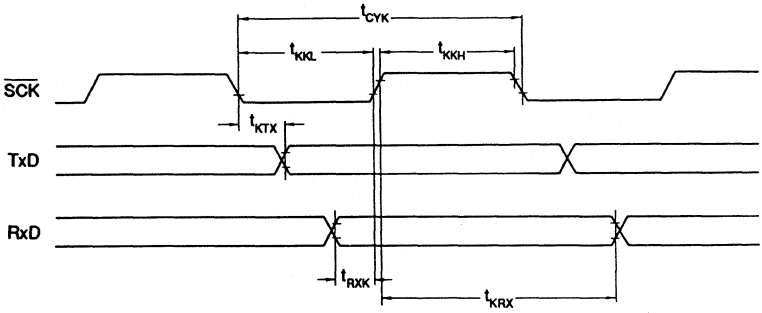


NOTE: 3. The $\overline{IO/M}$ signal is output through the MODE0 pin in the sr to sr2 register read cycle, if the MODE0 pin is pulled up.

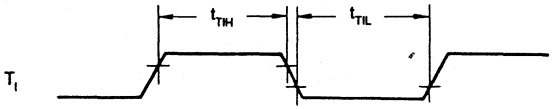
EPROM Read Timing



Serial Operation

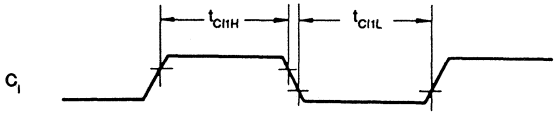


Timer Input Timing

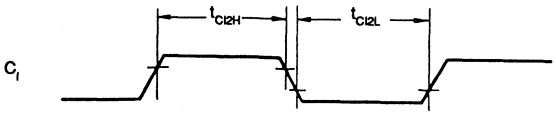


TIMER/EVENT COUNTER INPUT TIMING

Event Counter Mode

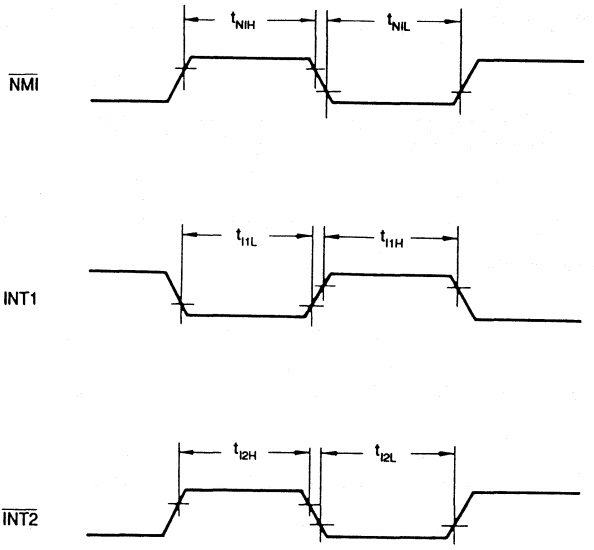


Pulse width measering Mode

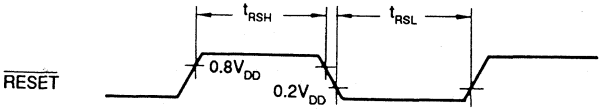


3

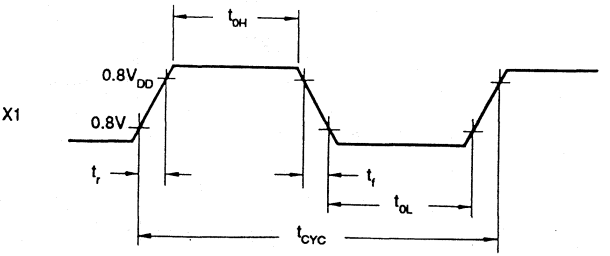
Interrupt Input Timing



Reset Input Timing

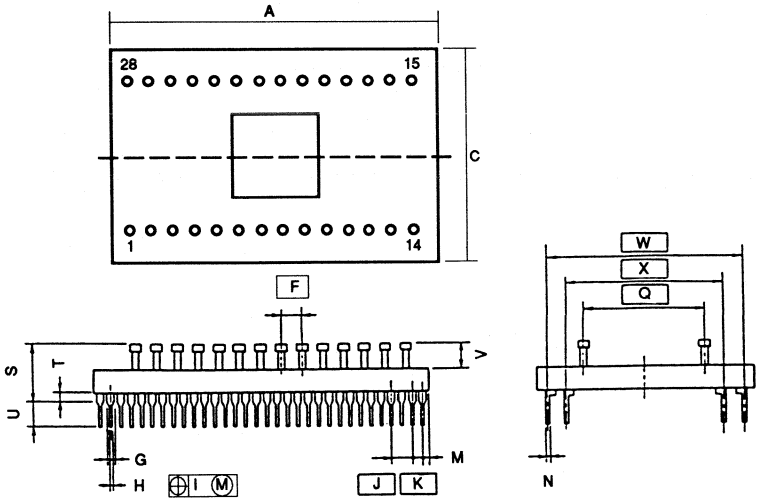


External Clock Timing



Package Outlines

64-Pin Ceramic Piggyback Package



NOTE
Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	41.91 MAX.	1.650 MAX.
C	$26.67^{\pm 0.4}$	$1.050^{\pm 0.016}$
F	2.54	0.100
G	0.92	0.036 MIN.
H	$0.46^{\pm 0.05}$	$0.018^{\pm 0.002}$
I	0.25	0.010
J	2.54 (T.P.)	0.100 (T.P.)
K	1.27 (T.P.)	0,050 (T.P.)
M	1.27 MAX.	0.050 MAX.
N	$0.25^{\pm 0.05}$	$0.010^{+0.002}_{-0.003}$
Q	15.24	0.600
S	8.03 MAX.	0.316 MAX.
T	1.0 MIN.	0.039 MIN.
U	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
V	3.9 MAX.	0.154 MAX.
W	24.13	0.950
X	19.05	0.750

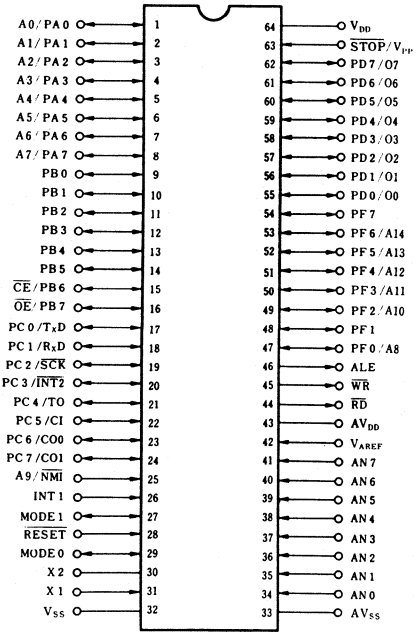
3

The μPD78CP14 is a single chip Microcomputer with on chip 16K — programmable ROM. The μPD78CP14 can be used for final evaluation and prototyping of μPD78C11/12/14
The μPD78CP14 is available in a Ceramic package (for testing) and in a plastic package as an OTP Version for preproduction.

Features

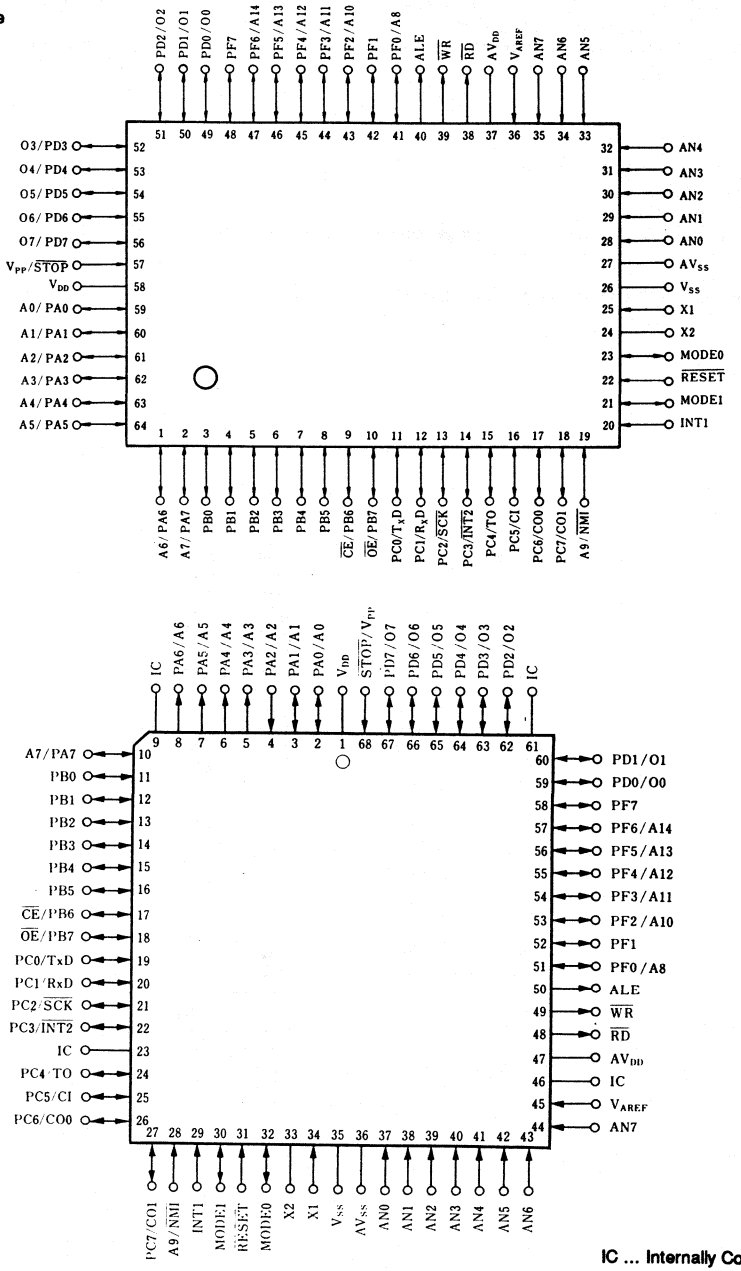
- Compatible with μPD78C11/12/14
- Internal EPROM:
  16384 words x 8 bits
  The internal EPROM capacity can be changed conforming to the μPD78C11/12/14 by using software.
- PROM programming characteristics:
  μPD27C256A compatible.
  PROM can be written by using a general purpose PROM writer.
- Single power supply:
  5V ± 10%

Pin Configuration
Shrink DIP, QUIP



3

Pin Configuration
Flat, PLCC package



IC ... Internally Connected

Pin Functions

1) Port Functions

Pin name	I/O	Function
PA7-0 (Port A)	I/O	8-bit input/output port. Input or output can be specified for each bit.
PB7-0 (Port B)		
PC7-0 (Port C)		
PD7-0 (Port D)		8-bit input/output port. Input or output can be specified for each byte.
PF7-0 (Port F)		8-bit input/output port. Input or output can be specifeid for each bit.

Remarks: In these port pins, there are dual function pins described in 2 (at normal operation) and 3 (at EPROM writing/verify/reading)

2) Functions Other than Ports (During Normal Operation)

Pin name	I/O	Other uses	Function
TxD (Transmit data)	O	PC0	Serial data output pin.
RxD (Receive data)	I	PC1	Serial data input pin.
$\overline{SCK}$ (Serial clock)	I/O	PC2	Serial clock input/output pin. When the internal clock is used, this line functions as an output and when an external clock source is used, this line functions as an input.
$\overline{INT2}$ (Interrupt request)	I	PC3	Maskable interrupt input (rising-edge triggered.)
TI (Timer input)	I		Timer external clock input pin.
Zero-cross	I		Zero cross detection pin of AC input.
TO (Timer output)	O	PC4	Square wave with pulse width on one internal clock cycle for timer count reference used as a half-cycle output.
CI (Counter input)	I	PC5	External pulse input pin to timer/event counter.
CO0, 1 (Counter output 0, 1)	I	PC6, 7	Programmable square wave output according to timer/event counter.
AD7-0 (Address/data bus 7-0)	I/O	PD7-0	These lines are used as a multiplexed address/data bus with external memory.
AB15-8 (Address bus 15-8)	O	PF7-0	These lines are used as an address bus with external memory.
$\overline{WR}$ (Write strobe)	O		Store signal output for external memory write operation. This signal is HIGH except during external memory data write cycles. When the $\overline{RESET}$ signal is LOW or the hardware STOP mode is engaged, this line is placed in a high-impedance state.
$\overline{RD}$ (Read strobe)	O		Store signal output for external memory read operation. This signal is HIGH except during external memory read cycles. When the $\overline{RESET}$ signal is LOW or the hardware STOP mode is engaged, this line is placed in a high-impedance state.
ALE (Address latch enable)	O		This line is used for the strobe signal to externally latch the lower-order address on the PD7-0 lines for external memory access. When the $\overline{RESET}$ signal is LOW or the hardware STOP mode is engaged, this line is placed in a high-impedance state.
MODE0 MODE1 (Mode)	I I/O		Set the MODE0 pin to 0 (low level) and the MODE1 pin to 1 (high level) (Note 1.)
$\overline{NMI}$ (Non-maskable interrupt)	I		Nonmaskable interrupt input (falling-edge triggered).
$\overline{INT1}$ (Interrupt request)	I		Maskable interrupt input (rising-edge triggered.) This line can also be used for AC input zero cross detection.

2) Functions Other than Ports (During Normal Operation) (Cont'd)

Pin name	I/O	Other uses	Function
AN7-0 (Analog input)	I		8-line analog input to A/D converter. Lines AN7-AN4 provided edge falling-edge detection input.
V_{AREF} (Reference voltage)	I		For use as both A/D converter reference voltage and A/D converter operation control.
AV_{DD} (Ananlog V_{SS})			Power supply line A/D converter.
AV_{SS} (Analog V_{SS})			GND potential for A/D converter.
X1, X2 (Crystal)			Crystal-oscillator input for system clock timing. When an external clock source is used, the timing pulses are input on X1. The X1 inversion signal is input to X2.
$\overline{RESET}$ (Reset)	I		System reset (active-low) input. Input line for hardware STOP mode control signal. When a low level is input, oscillation stops.
$\overline{STOP}$ (Stop)	I		Input line for hardware STOP mode control signal. When a low level is input, oscillation stops.
V_{DD}			+5 V power supply line.
V_{SS}			GND potential line.

Note: Pull-up resistance R has range $4k\Omega \leq R \leq 0.4\ t_{CYC}\ (k\Omega)$ [t_{CYC}: ns]

3) Functions Other than Ports (During EPROM Write, Verify, Read)

Pin name	I/O	Other uses	Function
A7-0	I	PA7-0	Low-order eight-bit input pins of address
$\overline{CE}$	I	PB6	Chip enable signal input pin.
$\overline{OE}$	I	PB7	Output enable signal input pin.
O7-0	I/O	PD7-0	Data input/output pins.
A14-10, A6	I	PF6-2, PF0	High-order 7-bit input pins address.
A9	I	NMI	
MODE0, MODE1	I		Set the MODE0 pin to 1 (high) and the MODE1 pin to 0 (low).
$\overline{RESET}$	I		Set the RESET pin to 0 (low).
V_{PP}		STOP	High voltage apply pin. When EPROM is read, high level (1) is input.

ELECTRICAL CHARACTERISTICS

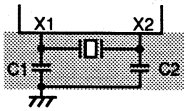
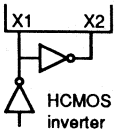
Absolute Maximum Ratings (Ta = 25 °C)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply voltage	V_{DD}		— 0.5 ~ +7.	V
	AV_{DD}		AV_{SS} ~ V_{DD} + 0.5	V
	AV_{SS}		— 0.5 ~ + 0.5	V
	V_{PP}		— 0.5 ~ + 13.5	V
Input voltage	V_I	except $\overline{NMI}$/A9 pins	— 0.5 ~ V_{DD} + 0.5	V
		$\overline{NMI}$/A9 pins in programming mode	−0.5 ~ +13.5	V
Output voltage	V_O		— 0.5 ~ V_{DD} + 0.5	V
Low-level output current	I_{OL}	All output pins	4.0	mA
		Total of all output pins	100	mA
High-level output current	I_{OH}	All output pins	— 2,0	mA
		Total of all output pins	— 50	mA
A/D converter reference voltage	V_{AREF}		—0.5 ~ AV_{DD} + 0.3	V
Operating temperature	T_{opt}		— 40 ~ + 85	°C
Storage temperature	T_{stg}		— 65 ~ + 150	°C

3

Oscillator Characteristics

(T_a = −40 to 85°C, V_{DD} = AV_{DD} = +5.0V ± 10%, V_{SS} = AV_{SS} = 0V, V_{DD} − 0.8V ≤ AV_{DD} ≤ V_{DD}, 3.4V ≤ V_{AREF} ≤ AV_{DD})

Oscillator	Recommended circuit	Item	Condition	MIN.	MAX.	Unit
Ceramic oscillator *1 or crystal oscillator*2		Oscillation frequency (f_{XX})		6	15	MHz
External Clock		X1 input frequency (f_X)		6	15	MHz
		X1 input rise time and fall time (t_r and t_f)		0	10	ns
		X1 input high and low level width (t_{OH} and t_{OL})		20	250	ns

*1: Locate the oscillator circuit as close to the X1 and X2 pin as possible.

*2: Do not wire any other signal lines in the shaded area ▨.

Capacitance (Ta = 25°C, $V_{DD} = V_{SS} = 0V$)

Item	Symbol	Condition	MIN	TYP	MAX	UNIT
Input capacitance	C_I	f_c = 1MHz Pins other than measured pins are at 0V			10	pF
Output capacitance	C_O				20	pF
Input/Output capacitance	C_{IO}				20	pF

DC Characteristics (Ta = −40 to +85°C, $V_{DD} = AV_{DD} = +5.0V \pm 10\%$; $V_{SS} = AV_{SS} = 0V$)

Item	Symbol	Condition		MIN	TYP	MAX	UNIT
Low-level input voltage	V_{IL1}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1 T1, and AN4-AN7 are excepted		0		0.8	V
	V_{IL2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1 T1, AN4-AN7		0		$0.2V_{DD}$	V
High-level input voltage	V_{IH1}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1 T1, AN4-AN7, X1, AND X2 are excepted		2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1 T1, AN1-AN7, X1, and X2		$0.8V_{DD}$		V_{DD}	V
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA				0.45	V
High-level output voltage	V_{OH}	I_{OH} = −1.0 mA	V_{DD} −1.0	V_{DD} −1.0			V
		I_{OH} = −100 μA	V_{DD} −0.5	V_{DD} −0.5			V
Input current	I_I	INT1*1, TI (PC3) *2; $0V \le V_1 \le V_{DD}$				±200	μA
Input leakage current	I_{LI}	Except INT1, TI (PC3); $0V \le V_1 \le V_{DD}$				±10	μA
Output leakage current	I_{LO}	$0V \le V0 \le V_{DD}$				±10	μA
AV_{DD} supply current	AI_{DD1}	Operation mode f_{XX} = 15 MHz			0.5	1.3	mA
	AI_{DD2}	STOP mode			10	20	μA
V_{DD} supply current *4	I_{DD1}	Operation mode f_{XX} = 15 MHz			16	32	mA
	I_{DD2}	HALT mode f_{XX} = 15 MHz			8	15	mA
Data retention voltage	V_{DDDR}	Hardware/Software STOP mode		2.5			V
Data retention voltage	I_{DDDR}	Hardware/ Software STOP mode *3	V_{DDDR} = 2.5V			300	μA
			$V_{DDDR} = 5V \pm 10\%$			1	mA

Note 1. When generation of self-bias is specified by the ZCM register.
2. When control mode is specified by the MCC register and generation of self-bias is specified by the ZCM register.
3. When self-bias is not generated.
4. Current flowing into the internal pull-up resistor is not included.

AC Characteristics (Ta = –40 to +85°C, $V_{DD} = AV_{DD} = +5.0V \pm 10\%$; $V_{SS} = AV_{SS} = 0V$)

Item	Symbol	Condition	MIN	MAX	UNIT
X1 input cycle time	t_{CYC}		66	167	ns
Address setup time (vs. ALE)	t_{LA}	f_{XX} = 15 MHz, C_L = 100pF	30		ns
Address hold time (vs. ALE)	t_{LA}		35		ns
Address RD delay time	t_{AR}		100		ns
RD address float time	t_{AFR}	C_L = 100pF		20	ns
Address data input time	t_{AD}			250	ns
ALE data input time	t_{LDR}			135	ns
RD data input time	t_{RT}			120	ns
ALE RD delay time	t_{LR}		15		ns
Data hold time (vs. RD)	t_{RDH}	C_L = 100pF	0		ns
RD ALE delay time	t_{RL}	f_{XX} = 15 MHz, C_L = 100pF	80		ns
		When reading data f_{XX} = 15 MHz, C_L = 100pF	215		ns
		When fetching opcode f_{XX} = 15 MHz, C_L = 100pF	415		ns
ALE high-level width	t_{LL}	f_{XX} = 15 MHz, C_L = 100pF	90		ns
Address WR delay time	t_{AW}		100		ns
ALE data output time	t_{LDW}			180	ns
WR data output time	t_{WD}	C_L = 100pF		100	ns
ALE WR delay time	t_{LW}	f_{XX} = 15 MHz, C_L = 100pF	15		ns
Data setup time (vs. WR)	t_{DW}		165		ns
Data hold time (vs. WR)	t_{WDH}		60		ns
WR ALE delay time	t_{WL}		80		ns
WR low-level width	t_{WW}		215		ns

3

DC Characteristics (Ta = – 40 to +85°C, $V_{DD} = AV_{DD} = +5.0V \pm 10\%$; $V_{SS} = AV_{SS} = 0V$)

Serial Operation

Item	Symbol	Condition		MIN	MAX	UNIT
SCK cycle time	t_{CYK}	SCK input	See Note 1.	800		ns
			See Note 2.	400		ns
		SCK output		1.6		ns
SCK low-level width	t_{KKL}	SCK input	See Note 1.	335		ns
			See Note 2.	160		ns
		SCK output		700		ns
SCK high-level width	t_{KKH}	SCK input	See Note 1.	335		ns
			See Note 2.	160		ns
		SCK output		700		ns
RxD setup time (vs. SCK)	t_{RXK}	See Note 1.		80		ns
RxD hold time (vs. SCK)	t_{KRX}	See Note 1.		80		ns
SCK TxD delay time	t_{KTX}	See Note 1.			210	ns

Note: 1. In asynchronous mode with clock rate of X1, or synchronous or I/O interface mode.
2. In asynchronous mode with clock rate of X16 or X64

Zero Crossover Characteristics

Item	Symbol	Condition	MIN	MAX	UNIT
Zero crossover detection input	V_{ZX}	AC coupling 60-Hz sine wave	1	1.8	VAC_{P-P}
Zero crossover accuracy	A_{ZX}			±135	mV
Zero crossover detection input frequency	f_{ZX}		0.05	1	kHz

Other Operations

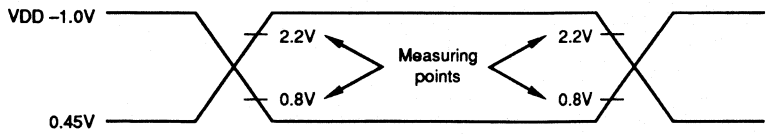
Item	Symbol	Condition	MIN	MAX	UNIT
TI high- and low-level widths	t_{TIH}, t_{TIL}		6		t_{CYC}
CI high- and low-level widths	t_{CI1H}, t_{CI1L}	Event counter mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse width measuring mode	48		t_{CYC}
NMI high- and low-level widths	t_{NIH}, t_{NIL}		10		μs
INT1 high- and low-level widths	t_{I1H}, t_{I1L}		36		t_{CYC}
INT2 high- and low-level widths	t_{I2H}, t_{I2L}		36		t_{CYC}
RESET high- and low-level widths	t_{RSH}, t_{RSL}		10		μs

A/D Converter Characteristics
(Ta = −40 to +85°C, V_{DD} = +5.0V ±10%; V_{SS} = AV_{SS} = 0V, V_{DD} −0.5V ≤ AV_{DD} ≤ V_{DD}, 3.4V ≤ V_{AREF} ≤ AV_{DD})

Item	Symbol	Condition	MIN	TYP	MAX	UNIT
Resolution			8			Bits
Absolute accuracy (See Note.)		3.4V ≤ V_{AREF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.8%	FSR
		4.0V ≤ V_{AREF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.6%	FSR
		Ta = −10 ~ +170°C, 4.0V ≤ V_{AREF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.4%	FSR
Conversion time	t_{CONV}	66ns ≤ t_{CYC} ≤ 110ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling time	t_{SAMP}	66ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	72			t_{CYC}
Analog input voltage	V_{IAN}		0		V_{AREF}	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	V_{AREF}		3.4		AV_{DD}	V
V_{AREF} current	I_{AREF1}	Operation mode		1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} supply current	AI_{DD1}	Operation mode f_{XX} = 15 MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA

Note: Quantization error (±1/2LSB) is not included.

AC Timing Points



Formula for calculation of AC characteristics dependet on t_{CYC}

Item	Formula	MIN/MAX	UNIT
t_{AL}	2T – 100	MIN	ns
t_{LA}	T – 30	MIN	ns
t_{AR}	3T – 100	MIN	ns
t_{AD}	7T – 220	MAX	ns
t_{LDR}	5T – 200	MAX	ns
t_{RD}	4T – 150	MAX	ns
t_{LR}	T – 50	MIN	ns
t_{RL}	2T – 50	MIN	ns
t_{RR}	4T – 50 (when reading data)	MIN	ns
	7T – 50 (when fetching opcode)		
t_{LL}	2T – 40	MIN	ns
t_{AW}	3T – 100	MIN	ns
t_{LDW}	T + 110	MIN	ns
t_{LW}	T – 50	MIN	ns
t_{DW}	4T – 100	MIN	ns
t_{WDH}	2T – 70	MIN	ns
t_{WW}	4T – 50	MIN	ns
t_{CYK}	12T (SCK input)*	MIN	ns
	24T (SCK output)		
t_{KKL}	5T + 5 (SCK input)*	MIN	ns
	12T – 100 (SCK output)		
t_{KKH}	5T + 5 (SCK input)*	MIN	ns
	12T – 100 (SCK output)		

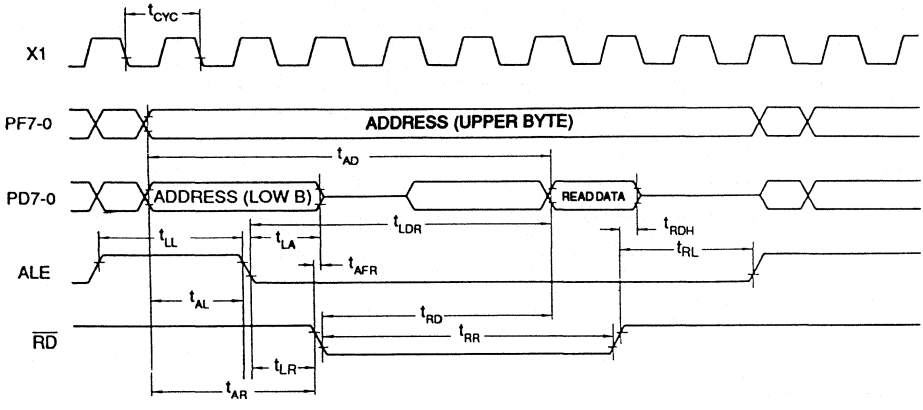
Note: In asynchronous mode with clock rate of X1, or in synchronous or I/O interface mode.

Remarks:

1: $T = t_{CYC} = 1/f_{XX}$

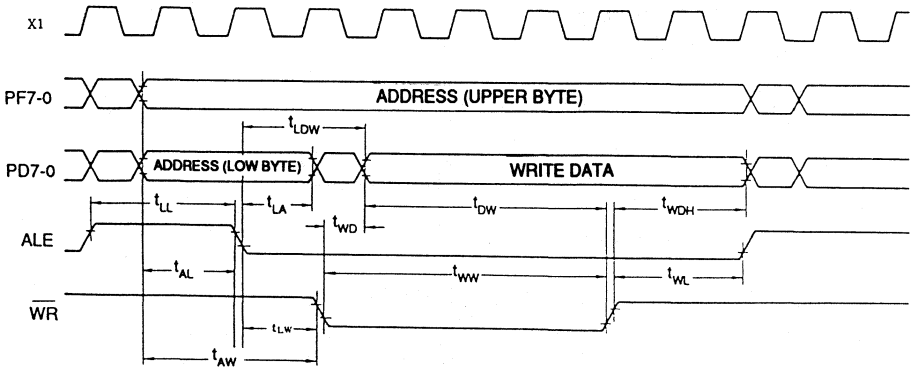
2. Items not shown here are not dependent on oscillation frequency f_{XX}.

TIMING WAVEFORM
Read Operation

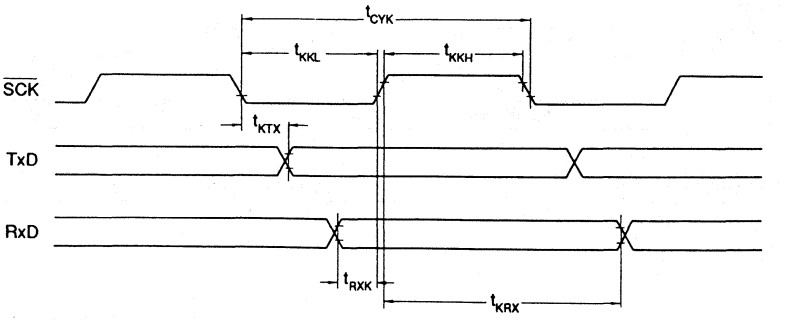


3

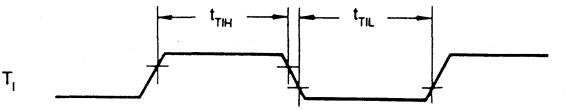
Write Operation



Serial Operation

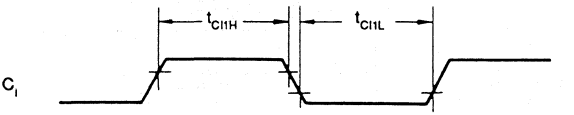


Timer Input Timing

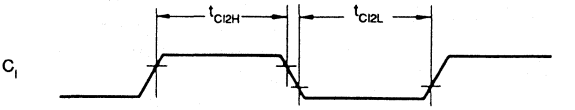


TIMER/EVENT COUNTER INPUT TIMING

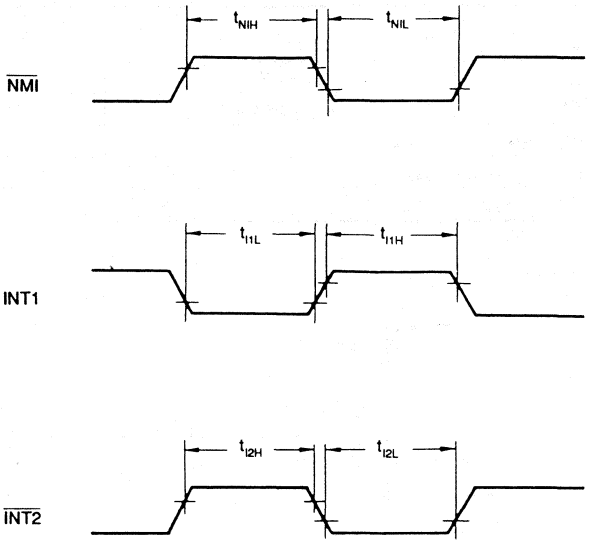
Event Counter Mode



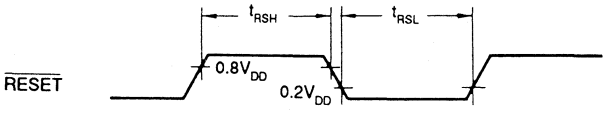
Pulse width measering Mode



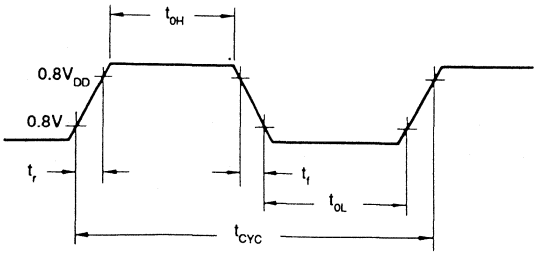
Interrupt Input Timing



Reset Input Timing



External Clock Timing

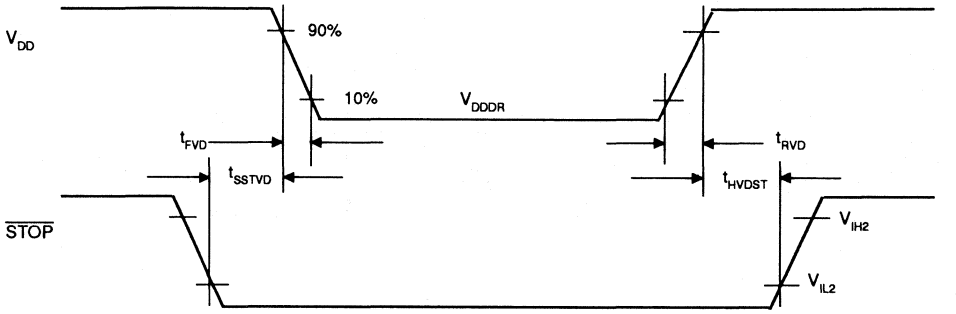


Data retention characteristics of low supply-voltage, data memory data retention STOP mode (Ta = -40 to +85 °C)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}		2.5		5.5	V
Data retention supply voltage	I_{DDDR}	V_{DDDR} = 2.5V			300	μA
		V_{DDDR} = 5V ± 5 %			1	mA
V_{DD} rise and fall times	t_{RVD}, t_{FVD}		200			μs
$\overline{STOP}$ setup time (vs. V_{DD})	t_{SSTVD}		12T + 0.5			μs
$\overline{STOP}$ hold time (vs. V_{DD})	t_{HVDST}		12T + 0.5			μs

Remarks: $T = t_{CYC} = 1/f_{XX}$

Data retention timing



DC Programming Characteristics

T_a = 25°C ± 5°C, MODE1 = V_{IL}, MODE0 = V_{IH}, V_{SS} = 0V)

Parameter	Symbol	Symbol *	Test condition	MIN.	TYP.	MAX.	Unit
Input high voltage	V_{IH}	V_{IH}		2.2		V_{DDP} +0.3	V
Input low voltage	V_{IL}	V_{IL}		–0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	$0 \le V_I \le V_{DDP}$; except for INT1, TI (PC3)			±10	μA
Output high voltage	V_{OH}	V_{OH}	I_{OH} = –1.0 mA	V_{DD} –1.0			V
Output low voltage	V_{OL}	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output leakage current	I_{LO}	—	$0 \le V_O \le V_{DDP}$, $\overline{OE}$ = V_{IH}			±10	μA
V_{DD} power supply voltage	V_{DDP}	V_{DD}	EPROM programming mode	5.75	6.0	6.25	V
			EPROM read mode	4.5	5.0	5.5	V
V_{PP} power supply voltage	V_{PP}	V_{PP}	EPROM programming mode	12.2	12.5	12.8	V
			EPROM read mode	V_{PP} = V_{DDP}			V
V_{DDP} power supply voltage	I_{DD}	I_{DD}	EPROM programming mode			30	mA
			EPROM read mode $\overline{CE}$ = V_{IL}, V_I = V_{IH}			30	mA
V_{PP} power supply voltage	I_{PP}	I_{PP}	EPROM programming mode $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			30	mA
			EPROM read mode		1	100	μA

Note *: Corresponding μPD27C256A symbols.

AC Programming Characteristics

T_a = 25°C ± 5°C, MODE1 = V_{IL}, V_{SS} = 0V)

Parameter	Symbol	Symbol *1	Test condition	MIN.	TYP.	MAX.	Unit
Address setup time to $\overline{CE}$ ↓	t_{SAC}	t_{AS}		2			μs
Data → $\overline{OE}$ ↓ delay time	t_{DDOO}	t_{OES}		2			μs
Input data setup time to $\overline{CE}$ ↓	t_{SIDC}	t_{DS}		2			μs
Address hold time from $\overline{CE}$ ↑	t_{HCA}	t_{AH}		2			μs
Input data hold time from $\overline{CE}$ ↑	t_{HCID}	t_{DH}		2			μs
Output data hold time from $\overline{OE}$ ↑	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} setup time to $\overline{CE}$ ↓	t_{SVPC}	t_{VPS}		2			μs
V_{DDP} setup time to $\overline{CE}$ ↓	t_{SVDC}	t_{VDS}		2			μs
Initial program pulse with	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Added program pulse with	t_{WL2}	t_{OPW}		2.85		78.75	ms
EPROM programming/read mode setup time to $\overline{CE}$ ↓ (*2)	t_{SMC}	—		2			μs

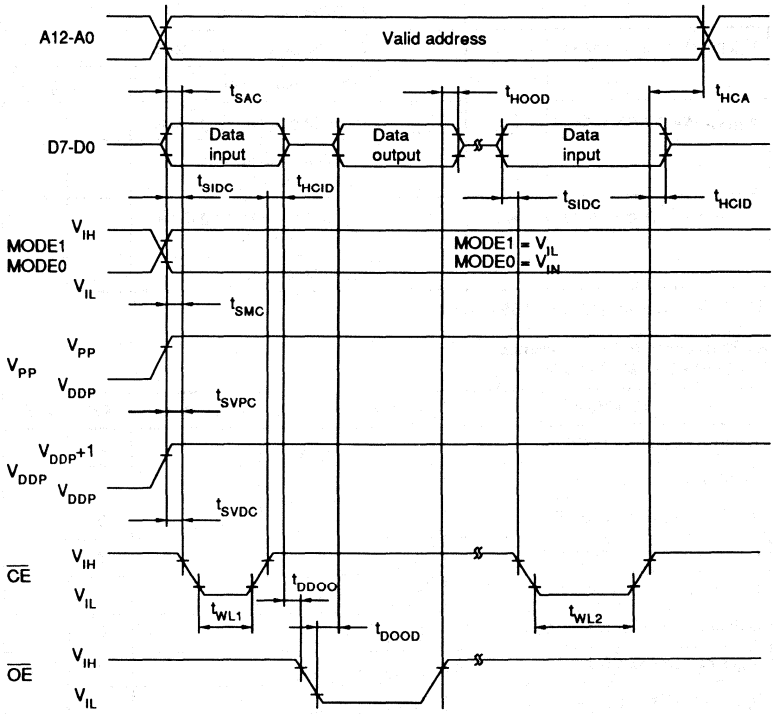
3

AC Programming Characteristics (Cont'd)
T_a = 25°C ± 5°C, MODE1 = V_{IL}, V_{SS} = 0V)

Parameter	Symbol	Symbol *1	Test condition	MIN.	TYP.	MAX.	Unit
Address → data output time	t_{DAOD}	t_{ACC}	$\overline{OE}$ = V_{IL}			2	μs
$\overline{CE}$ ↓ → data output time	t_{DCOD}	t_{CE}				1	μs
$\overline{OE}$ ↓ → data output time	t_{DOOD}	t_{OE}				1	μs
Data hold time from $\overline{OE}$ ↑	t_{HCOD}	t_{DF}		0		130	ns
Data hold time from address	t_{HAOD}	t_{OH}	$\overline{OE}$ = V_{IL}	0			ns

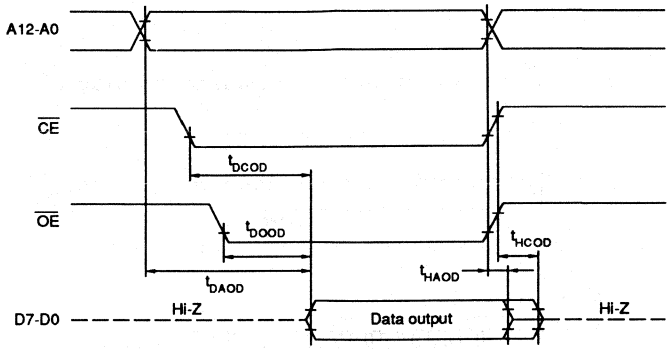
Note *1: Corresponding μPD27C256A symbols.
Note *2: When MODE1 = V_{IL} and MODE0 = V_{IH}.

EPROM Programming Mode Timing



Caution 1: Apply voltage to V_{DDP} before V_{PP} and turn off V_{DDP} after V_{PP}.
Caution 2: Do not apply voltage of 12.8 V or more containing overshoot to V_{PP}.

EPROM Read Mode Timing



Caution 1: To read EPROM within the t_{DAOD} range, the delay time of $\overline{OE}$ input from the $\overline{CE}$ falling edge must be within t_{DAOD}-t_{DOOD}.

Caution 2: t_{HCOD} is the time from the state in which either $\overline{OE}$ or $\overline{CE}$ first becomes V_{IH}.

Differences Between μPD78CP14 and Mask ROM Products

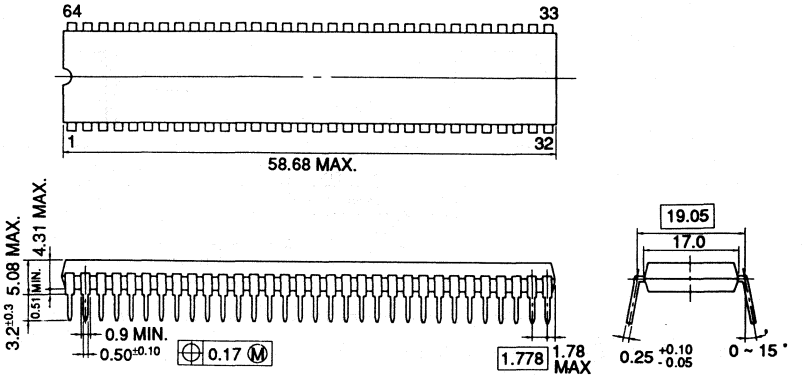
Item	μPD78CP14	μPD78C14/14A *3	μPD78C12A	μPD78C11/11A
Internal program memory	• EPROM • 16348 x 8 bits	• Mask ROM • 16384 x 8 bits	• Mask ROM • 8192 x 8 bits	• Mask ROM • 4096 x 8 bits
Pin	PB7/$\overline{OE}$	PB7		
	PB6/$\overline{CE}$	PB6		
	$\overline{STOP}$/V_{PP}	$\overline{STOP}$		
	$\overline{NMI}$/A9	$\overline{NMI}$		
	PA7-0/A7-0	PA7-0		
	PF6-2/A14-10	PF6-2		
	PF0/A8	PF0		
	PD7-0/O7/0	PD7-0		
Mode set by using MODE pins (when MODE0 is set to 1 and MODE1 to 0)	EPROM programming mode	• Operation as μPD78C10 (ROMless mode) • External memory 16K extension mode		
MODE0 pin input/output function	Input only *1	Input/output		
Emulation mode	Not included	Included		
Specification of internal ROM access range by using MM registrer	Made	Not made		
Package	• 64-pin plastic shrink DIP *2 • 64-pin plastic QUIP *2 • 64-pin plastic flat-pack *2 • 68-pin PLCC *2 • 64-pin ceramic shrink DIP with window • 64-pin ceramic QUIP with window	• 64-pin plastic shrink DIP • 64-pin plastic QUIP • 64-pin plastic flat-pack • 68-pin PLCC		

Note *1: Thus, even if the MODE0 pin is pulled up, emulation control signal is not output.
Note *2: One-time PROM is under development.
Note *3: Only 64-pin plastic quad-flat package is available.

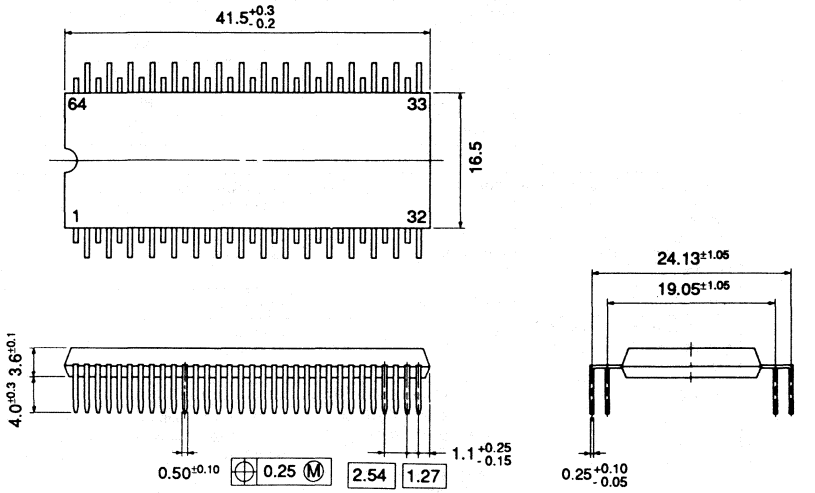
3

Package Dimensions

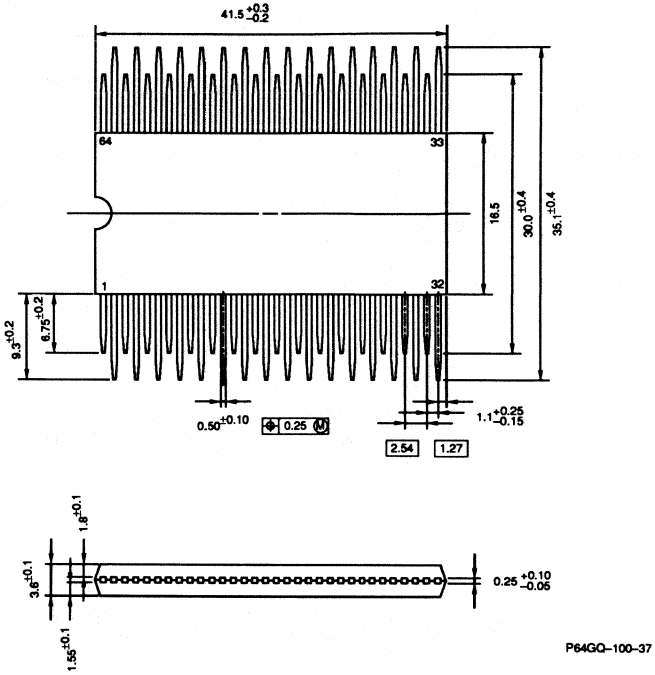
64 - Pin SDIP



64 - Pin QUIP (Bent Leads)

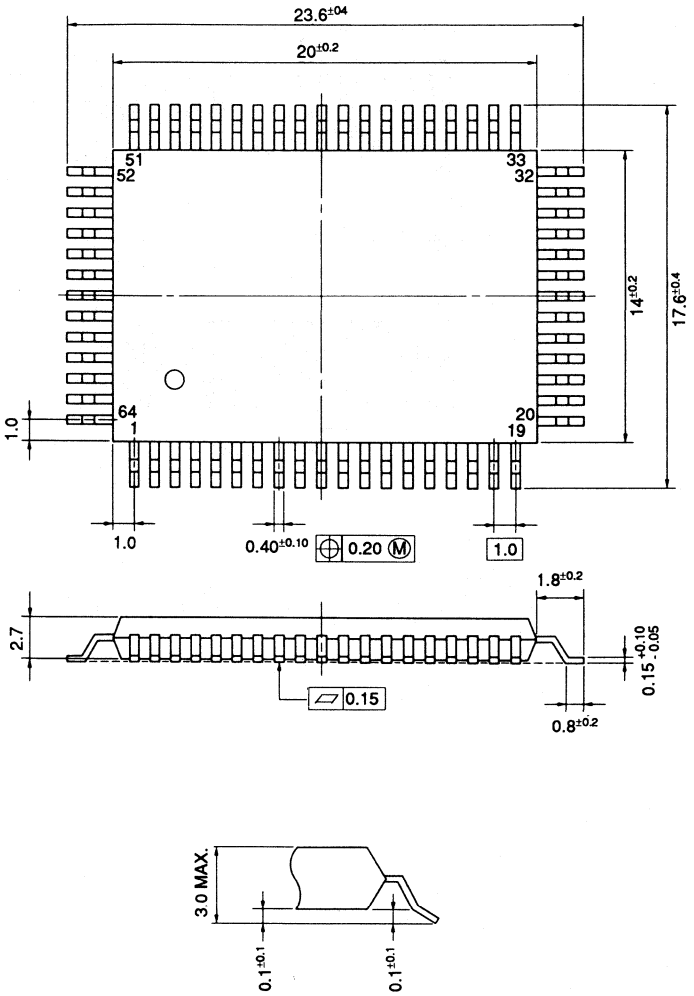


64 PIN PLASTIC
QUIP STRAIGHT LEADS
PACKAGE DIMENSIONS
(Units: mm)

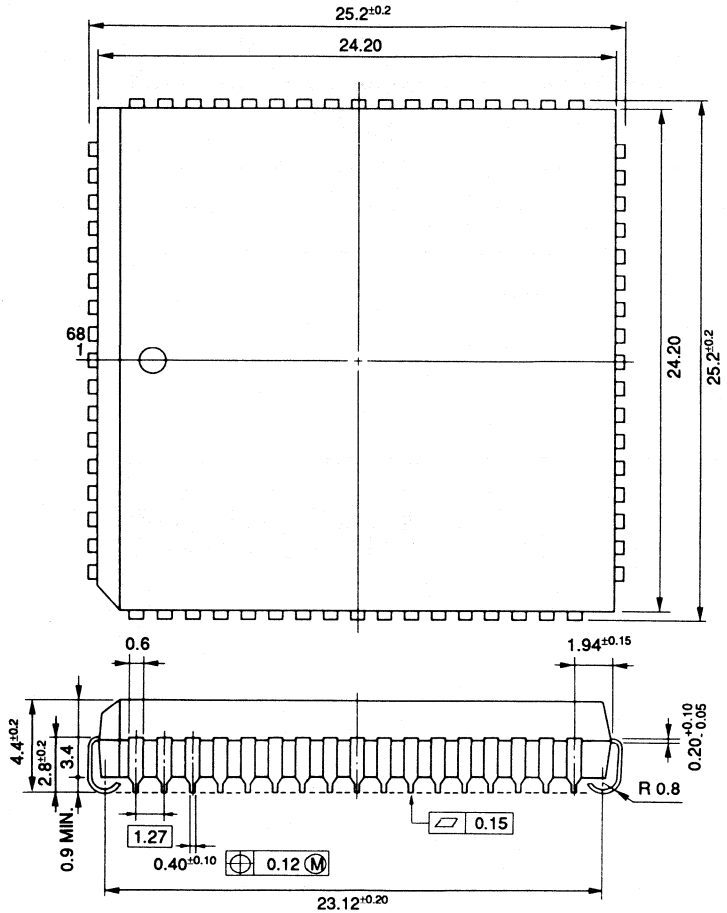


3

64 - Pin FLAT PACK

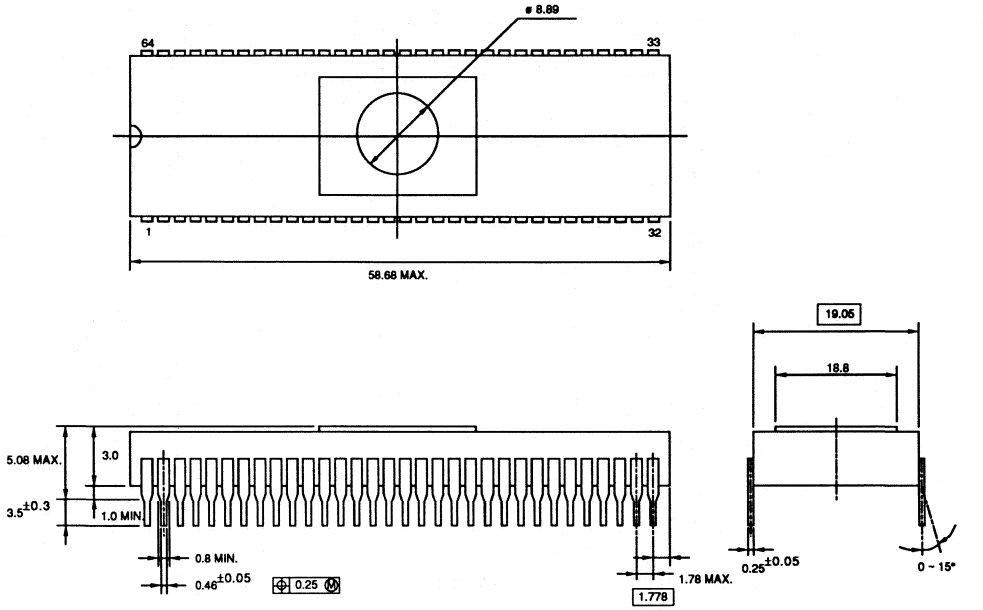


68 - Pin PLCC

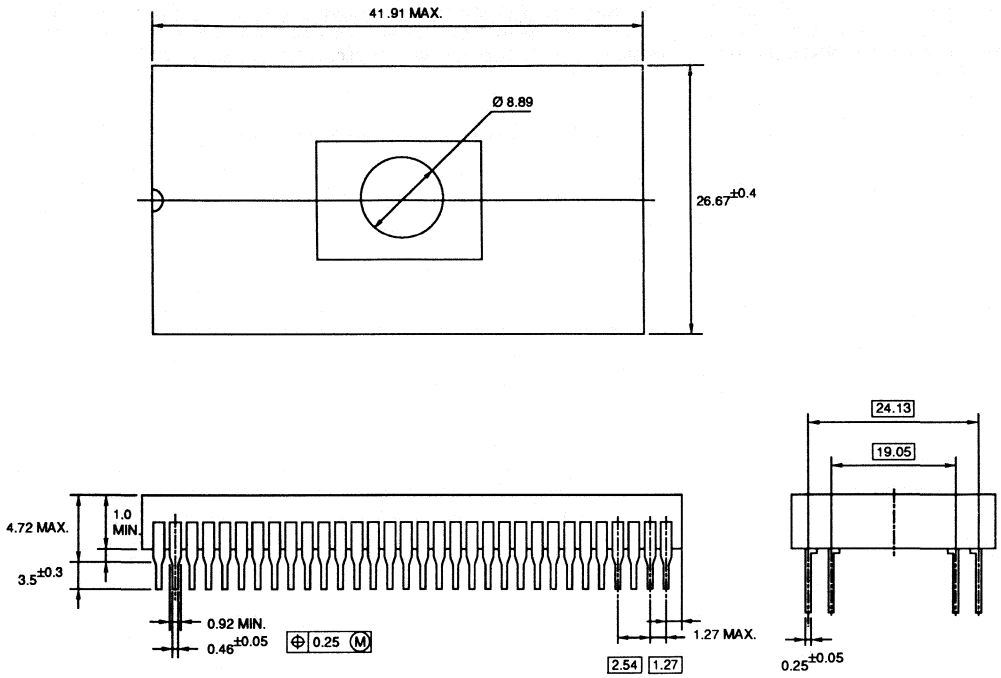

25.2±0.2
24.20
68
1
24.20
25.2±0.2
0.6
1.94±0.15
4.4±0.2
2.8±0.2
3.4
0.9 MIN.
0.20+0.10 −0.05
R 0.8
1.27
0.40±0.10
0.12 M
0.15
23.12±0.20

3

64-PIN SHRINK DIP WITH CERAMIC WINDOW (750 mil) (Unit: mm)



64-PIN CERAMIC
QUAD-IN-LINE (QUIP)
PACKAGE DIMENSIONS
(Unit: mm)



EPROM Erase Procedure (only Products with Ceramic Window)

The EPROM contents can be erased by light rays whose wavelength is shorter than about 400 nm. The programmed EPROM data contents may also be erased if the uncovered window is exposed to direct sunlight or a fluorescent light for several hours. Thus, to protect the data contents, cover the μPD78CP14 with an opaque film so as to prevent ultraviolet rays from entering through the top window.

For normal EPROM erase, place the μPD78CP14 under an ultraviolet light source (254 nm). The minimum amount of radiation exposure required to erase the μPD78CP14 completely is 15 W.s/cm^2 (ultraviolet ray strength x erase time). This corresponds to about 15 to 20 minutes when using a ultraviolet ray lamp of 12000 μW/cm^2. However, note that the erase time may be prolonged by aging of the ultraviolet lamp, dirty package window, etc. The distance between the ultraviolet lamp and the μPD78CP14 should be within 2,5 cm.

CMOS-DESIGN RECOMMENDATIONS

In order to maximize circuit reliability please note the general CMOS design rules.

For example:

1) Don't leave unused pins open, except they are outputs or not connected.

2) Never exceed the max. voltage range.

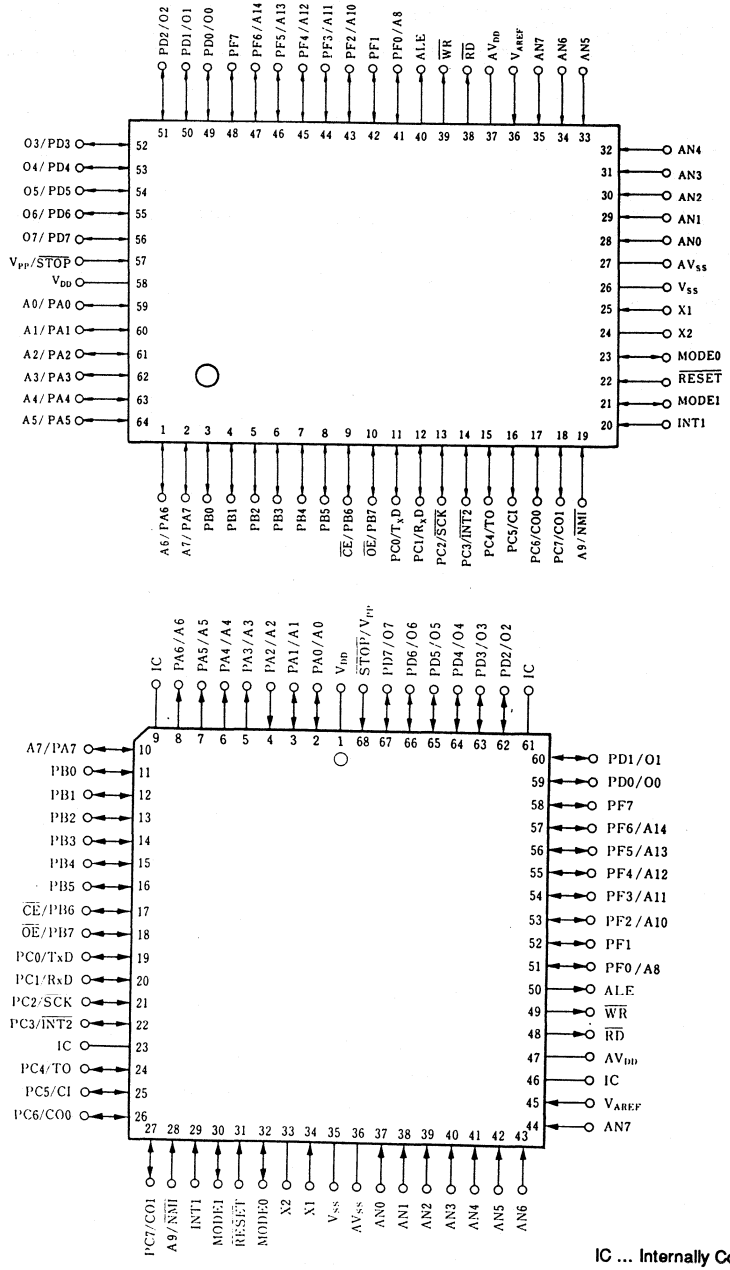
3) Avoid accurance of very fast voltage spikes or transission rate the power supply pin.

The μPD78CP18 is a single chip Microcomputer with on chip 32K–programmable ROM. The μPD78P18 can be used for final evaluation and prototyping of μPD78C11/12/14/18.
The μPD78C18 is available in a Ceramic package (for testing) and in a plastic package as an OTP Version for preproduction.

Features

- Compatible with μPD78C11/12/14/18
- internal EPROM:
  32767 words x 8 bits
  The internal EPROM capacity can be changed conforming to the μPD78C11/12/14/18 by using software.
- PROM programming characteristics:
  μPD27C256A compatible.
  PROM can be written by using a general purpose PROM writer.
- Single power supply:
  5V ± 10%

Pin Configuration
Flat, LCC package



IC ... Internally Connected

Pin Functions

1) Port Functions

Pin name	I/O	Function
PA7-0 (Port A)	I/O	8-bit input/output port. Input or output can be specified for each bit.
PB7-0 (Port B)		
PC7-0 (Port C)		
PD7-0 (Port D)		8-bit input/output port. Input or output can be specified for each byte.
PF7-0 (Port F)		8-bit input/output port. Input or output can be specifeid for each bit.

Remarks: In these port pins, there are dual function pins described in 2 (at normal operation) and 3 (at EPROM writing/verify/reading)

2) Functions Other than Ports (During Normal Operation)

Pin name	I/O	Other uses	Function
TxD (Transmit data)	O	PC0	Serial data output pin.
RxD (Receive data)	I	PC1	Serial data input pin.
$\overline{SCK}$ (Serial clock)	I/O	PC2	Serial clock input/output pin. When the internal clock is used, this line functions as an output and when an external clock source is used, this line functions as an input.
$\overline{INT2}$ (Interrupt request)	I	PC3	Maskable interrupt input (rising-edge triggered.)
TI (Timer input)	I		Timer external clock input pin.
Zero-cross	I		Zero cross detection pin of AC input.
TO (Timer output)	O	PC4	Square wave with pulse width on one internal clock cycle for timer count reference used as a half-cycle output.
CI (Counter input)	I	PC5	External pulse input pin to timer/event counter.
CO0, 1 (Counter output 0, 1)	I	PC6, 7	Programmable square wave output according to timer/event counter.
AD7-0 (Address/data bus 7-0)	I/O	PD7-0	These lines are used as a multiplexed address/data bus with external memory.
AB15-8 (Address bus 15-8)	O	PF7-0	These lines are used as an address bus with external memory.
$\overline{WR}$ (Write strobe)	O		Store signal output for external memory write operation. This signal is HIGH except during external memory data write cycles. When the RESET signal is LOW or the hardware STOP mode is engaged, this line is placed in a high-impedance state.
$\overline{RD}$ (Read strobe)	O		Store signal output for external memory read operation. This signal is HIGH except during external memory read cycles. When the RESET signal is LOW or the hardware STOP mode is engaged, this line is placed in a high-impedance state.
ALE (Address latch enable)	O		This line is used for the strobe signal to externally latch the lower-order address on the PD7-0 lines for external memory access. When the RESET signal is LOW or the hardware STOP mode is engaged, this line is placed in a high-impedance state.
MODE0 MODE1 (Mode)	I I/O		Set the MODE0 pin to 0 (low level) and the MODE1 pin to 1 (high level) (Note 1.)
$\overline{NMI}$ (Non-maskable interrupt)	I		Nonmaskable interrupt input (falling-edge triggered).
$\overline{INT1}$ (Interrupt request)	I		Maskable interrupt input (rising-edge triggered.) This line can also be used for AC input zero cross detection.

2) Functions Other than Ports (During Normal Operation) (Cont'd)

Pin name	I/O	Other uses	Function
AN7-0 (Analog input)	I		8-line analog input to A/D converter. Lines AN7-AN4 provided edge falling-edge detection input.
V_{AREF} (Reference voltage)	I		For use as both A/D converter reference voltage and A/D converter operation control.
AV_{DD} (Ananlog V_{SS})			Power supply line A/D converter.
AV_{SS} (Analog V_{SS})			GND potential for A/D converter.
X1, X2 (Crystal)			Crystal-oscillator input for system clock timing. When an external clock source is used, the timing pulses are input on X1. The X1 inversion signal is input to X2.
$\overline{RESET}$ (Reset)	I		System reset (active-low) input. Input line for hardware STOP mode control signal. When a low level is input, oscillation stops.
$\overline{STOP}$ (Stop)	I		Input line for hardware STOP mode control signal. When a low level is input, oscillation stops.
V_{DD}			+5 V power supply line.
V_{SS}			GND potential line.

Note: Pull-up resistance R has range $4k\Omega \leq R \leq 0.4\ t_{CYC}\ (k\Omega)$ [t_{CYC}: ns]

3) Functions Other than Ports (During EPROM Write, Verify, Read)

Pin name	I/O	Other uses	Function
A7-0	I	PA7-0	Low-order eight-bit input pins of address
$\overline{CE}$	I	PB6	Chip enable signal input pin.
$\overline{OE}$	I	PB7	Output enable signal input pin.
O7-0	I/O	PD7-0	Data input/output pins.
A14-10, A6	i	PF6-2, PF0	High-order 7-bit input pins address.
A9	I	NMI	
MODE0, MODE1	I		Set the MODE0 pin to 1 (high) and the MODE1 pin to 0 (low).
$\overline{RESET}$	I		Set the RESET pin to 0 (low).
V_{PP}		STOP	High voltage apply pin. When EPROM is read, high level (1) is input.

ELECTRICAL CHARACTERISTICS

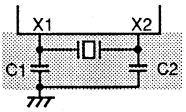
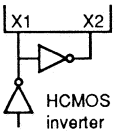
Absolute Maximum Ratings (Ta = 25 °C)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply voltage	V_{DD}		— 0.5 ~ +7.	V
	AV_{DD}		AV_{SS} ~ V_{DD} + 0.5	V
	AV_{SS}		— 0.5 ~ + 0.5	V
	V_{PP}		— 0.5 ~ + 13.5	V
Input voltage	V_I	except $\overline{NMI}$/A9 pins	— 0.5 ~ V_{DD} + 0.5	V
		$\overline{NMI}$/A9 pins in programming mode	−0.5 ~ +13.5	V
Output voltage	V_O		— 0.5 ~ V_{DD} + 0.5	V
Low-level output current	I_{OL}	All output pins	4.0	mA
		Total of all output pins	100	mA
High-level output current	I_{OH}	All output pins	— 2.0	mA
		Total of all output pins	— 50	mA
A/D converter reference voltage	V_{AREF}		—0.5 ~ AV_{DD} + 0.3	V
Operating temperature	T_{opt}		— 40 ~ + 85	°C
Storage temperature	T_{stg}		— 65 ~ + 150	°C

3

Oscillator Characteristics

(T_a = −40 to 85°C, V_{DD} = AV_{DD} = +5.0V ± 10%, V_{SS} = AV_{SS} = 0V, V_{DD} − 0.8V ≤ AV_{DD} ≤ V_{DD}, 3.4V ≤ V_{AREF} ≤ AV_{DD})

Oscillator	Recommended circuit	Item	Condition	MIN.	MAX.	Unit
Ceramic oscillator *1 or crystal oscillator*2		Oscillation frequency (f_{XX})		6	15	MHz
External Clock		X1 input frequency (f_X)		6	15	MHz
		X1 input rise time and fall time (t_r and t_f)		0	10	ns
		X1 input high and low level width (t_{OH} and t_{OL})		20	250	ns

*1: Locate the oscillator circuit as close to the X1 and X2 pin as possible.

*2: Do not wire any other signal lines in the shaded area ▨.

Capacitance (Ta = 25°C, $V_{DD} = V_{SS} = 0V$)

Item	Symbol	Condition	MIN	TYP	MAX	UNIT
Input capacitance	C_I	f_c = 1MHz Pins other than measured pins are at 0V			10	pF
Output capacitance	C_O				20	pF
Input/Output capacitance	C_{IO}				20	pF

DC Characteristics (Ta = −40 to +85°C, $V_{DD} = AV_{DD} = +5.0V \pm 10\%$; $V_{SS} = AV_{SS} = 0V$)

Item	Symbol	Condition		MIN	TYP	MAX	UNIT
Low-level input voltage	V_{IL1}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1 T1, and AN4-AN7 are excepted		0		0.8	V
	V_{IL2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1 T1, AN4-AN7		0		$0.2V_{DD}$	V
High-level input voltage	V_{IH1}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1 T1, AN4-AN7, X1, AND X2 are excepted		2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1 T1, AN1-AN7, X1, and X2		$0.8V_{DD}$		V_{DD}	V
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA				0.45	V
High-level output voltage	V_{OH}	I_{OH} = −1.0 mA	V_{DD} −1.0	V_{DD} −1.0			V
		I_{OH} = −100 μA	V_{DD} −0.5	V_{DD} −0.5			V
Input current	I_I	INT1*1, TI (PC3) *2; $0V \le V_I \le V_{DD}$				±200	μA
Input leakage current	I_{LI}	Except INT1, TI (PC3); $0V \le V_I \le V_{DD}$				±10	μA
Output leakage current	I_{LO}	$0V \le V0 \le V_{DD}$				±10	μA
AV_{DD} supply current	AI_{DD1}	Operation mode f_{XX} = 15 MHz			5)	5)	mA
	AI_{DD2}	STOP mode			5)	5)	μA
V_{DD} supply current *4	I_{DD1}	Operation mode f_{XX} = 15 MHz			5)	5)	mA
	I_{DD2}	HALT mode f_{XX} = 15 MHz			5)	5)	mA
Data retention voltage	V_{DDDR}	Hardware/Software STOP mode		2.5			V
Data retention voltage	I_{DDDR}	Hardware/ Software STOP mode *3	V_{DDDR} = 2.5V			300	μA
			V_{DDDR} = 5V ±10%			1	mA

Note
1. When generation of self-bias is specified by the ZCM register.
2. When control mode is specified by the MCC register and generation of self-bias is specified by the ZCM register.
3. When self-bias is not generated.
4. Current flowing into the internal pull-up resistor is not included.
5. to be measured on final silicon.

AC Characteristics (Ta = –40 to +85°C, $V_{DD} = AV_{DD} = +5.0V \pm 10\%$; $V_{SS} = AV_{SS} = 0V$)

Item	Symbol	Condition	MIN	MAX	UNIT
X1 input cycle time	t_{CYC}		66	167	ns
Address setup time (vs. ALE)	t_{LA}	f_{XX} = 15 MHz, C_L = 100pF	30		ns
Address hold time (vs. ALE)	t_{LA}		35		ns
Address RD delay time	t_{AR}		100		ns
RD address float time	t_{AFR}	C_L = 100pF		20	ns
Address data input time	t_{AD}			250	ns
ALE data input time	t_{LDR}			135	ns
RD data input time	t_{RT}			120	ns
ALE RD delay time	t_{LR}		15		ns
Data hold time (vs. RD)	t_{RDH}	C_L = 100pF	0		ns
RD ALE delay time	t_{RL}	f_{XX} = 15 MHz, C_L = 100pF	80		ns
		When reading data f_{XX} = 15 MHz, C_L = 100pF	215		ns
		When fetching opcode f_{XX} = 15 MHz, C_L = 100pF	415		ns
ALE high-level width	t_{LL}	f_{XX} = 15 MHz, C_L = 100pF	90		ns
Address WR delay time	t_{AW}		100		ns
ALE data output time	t_{LDW}			180	ns
WR data output time	t_{WD}	C_L = 100pF		100	ns
ALE WR delay time	t_{LW}	f_{XX} = 15 MHz, C_L = 100pF	15		ns
Data setup time (vs. WR)	t_{DW}		165		ns
Data hold time (vs. WR)	t_{WDH}		60		ns
WR ALE delay time	t_{WL}		80		ns
WR low-level width	t_{WW}		215		ns

3

DC Characteristics (Ta = – 40 to +85°C, $V_{DD} = AV_{DD} = +5.0V \pm 10\%$; $V_{SS} = AV_{SS} = 0V$)

Serial Operation

Item	Symbol	Condition		MIN	MAX	UNIT
SCK cycle time	t_{CYK}	SCK input	See Note 1.	800		ns
			See Note 2.	400		ns
		SCK output		1.6		ns
SCK low-level width	t_{KKL}	SCK input	See Note 1.	335		ns
			See Note 2.	160		ns
		SCK output		700		ns
SCK high-level width	t_{KKH}	SCK input	See Note 1.	335		ns
			See Note 2.	160		ns
		SCK output		700		ns
RxD setup time (vs. SCK)	t_{RXK}	See Note 1.		80		ns
RxD hold time (vs. SCK)	t_{KRX}	See Note 1.		80		ns
SCK TxD delay time	t_{KTX}	See Note 1.			210	ns

Note: 1. In asynchronous mode with clock rate of X1, or synchronous or I/O interface mode.
2. In asynchronous mode with clock rate of X16 or X64

Zero Crossover Characteristics

Item	Symbol	Condition	MIN	MAX	UNIT
Zero crossover detection input	V_{ZX}	AC coupling 60-Hz sine wave	1	1.8	VAC_{P-P}
Zero crossover accuracy	A_{ZX}			±135	mV
Zero crossover detection input frequency	f_{ZX}		0.05	1	kHz

Other Operations

Item	Symbol	Condition	MIN	MAX	UNIT
TI high- and low-level widths	t_{TIH}, t_{TIL}		6		t_{CYC}
CI high- and low-level widths	t_{CI1H}, t_{CI1L}	Event counter mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse width measuring mode	48		t_{CYC}
NMI high- and low-level widths	t_{NIH}, t_{NIL}		10		μs
INT1 high- and low-level widths	t_{I1H}, t_{I1L}		36		t_{CYC}
INT2 high- and low-level widths	t_{I2H}, t_{I2L}		36		t_{CYC}
RESET high- and low-level widths	t_{RSH}, t_{RSL}		10		μs

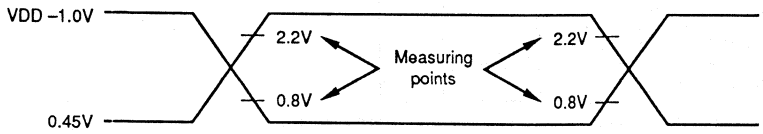
A/D Converter Characteristics

(Ta = –40 to +85°C, V_{DD} = +5.0V ±10%; V_{SS} = AV_{SS} = 0V, V_{DD} –0.5V ≤ AV_{DD} ≤ V_{DD}, 3.4V ≤ V_{AREF} ≤ AV_{DD})

Item	Symbol	Condition	MIN	TYP	MAX	UNIT
Resolution			8			Bits
Absolute accuracy (See Note.)		3.4V ≤ V_{AREF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.8%	FSR
		4.0V ≤ V_{AREF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.6%	FSR
		Ta = –10 ~ +170°C, 4.0V ≤ V_{AREF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.4%	FSR
Conversion time	t_{CONV}	66ns ≤ t_{CYC} ≤ 110ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling time	t_{SAMP}	66ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	72			t_{CYC}
Analog input voltage	V_{IAN}		0		V_{AREF}	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	V_{AREF}		3.4		AV_{DD}	V
V_{AREF} current	I_{AREF1}	Operation mode		1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} supply current	AI_{DD1}	Operation mode f_{XX} = 15 MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA

Note: Quantization error (±1/2LSB) is not included.

AC Timing Points



Formula for calculation of AC characteristics dependet on t_{CYC}

Item	Formula	MIN/MAX	UNIT
t_{AL}	2T – 100	MIN	ns
t_{LA}	T – 30	MIN	ns
t_{AR}	3T – 100	MIN	ns
t_{AD}	7T – 220	MAX	ns
t_{LDR}	5T – 200	MAX	ns
t_{RD}	4T – 150	MAX	ns
t_{LR}	T – 50	MIN	ns
t_{RL}	2T – 50	MIN	ns
t_{RR}	4T – 50 (when reading data)	MIN	ns
	7T – 50 (when fetching opcode)		
t_{LL}	2T – 40	MIN	ns
t_{AW}	3T – 100	MIN	ns
t_{LDW}	T + 110	MIN	ns
t_{LW}	T – 50	MIN	ns
t_{DW}	4T – 100	MIN	ns
t_{WDH}	2T – 70	MIN	ns
t_{WW}	4T – 50	MIN	ns
t_{CYK}	12T (SCK input)*	MIN	ns
	24T (SCK output)		
t_{KKL}	5T + 5 (SCK input)*	MIN	ns
	12T – 100 (SCK output)		
t_{KKH}	5T + 5 (SCK input)*	MIN	ns
	12T – 100 (SCK output)		

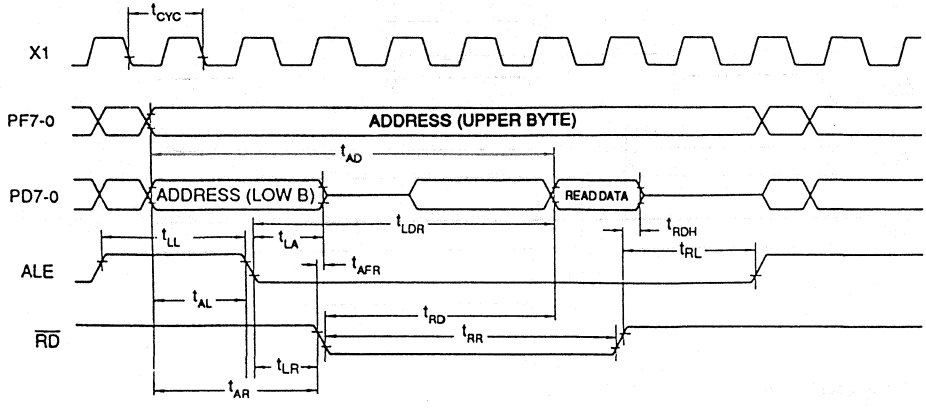
Note: In asynchronous mode with clock rate of X1, or in synchronous or I/O interface mode.

Remarks:

1: $T = t_{CYC} = 1/f_{XX}$

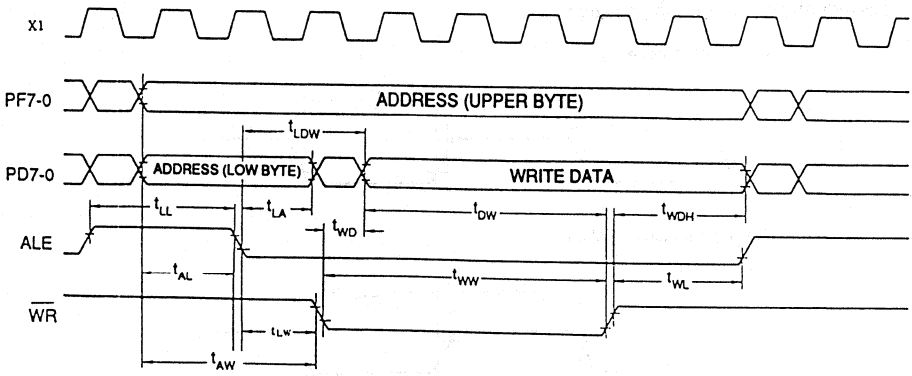
2. Items not shown here are not dependent on oscillation frequency f_{XX}.

TIMING WAVEFORM
Read Operation

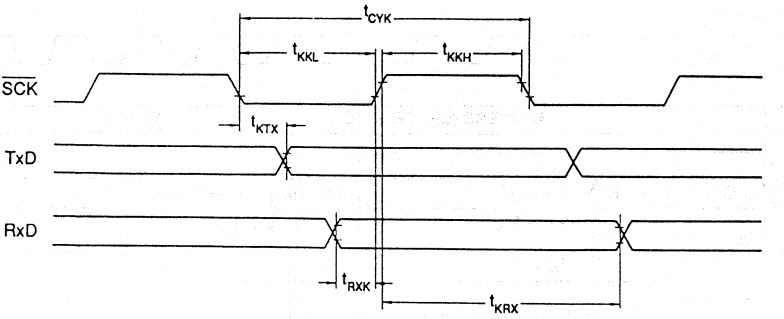


3

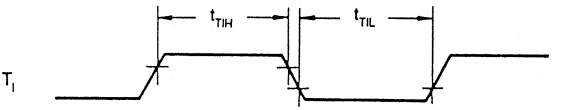
Write Operation



Serial Operation

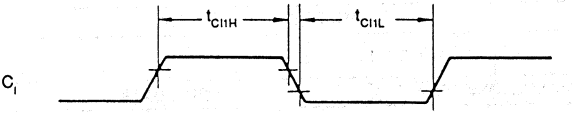


Timer Input Timing

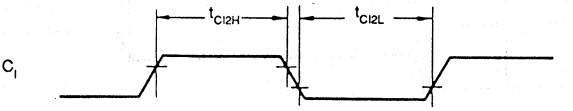


TIMER/EVENT COUNTER INPUT TIMING

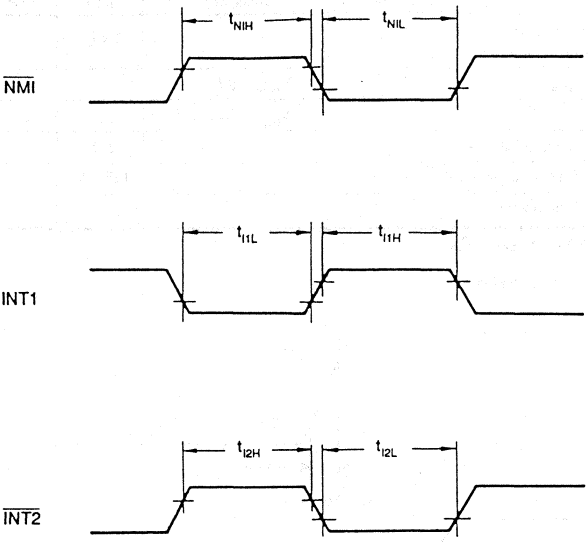
Event Counter Mode



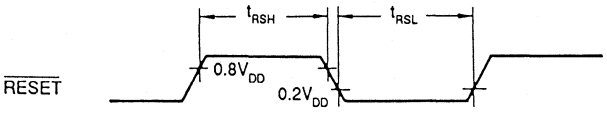
Pulse width measering Mode



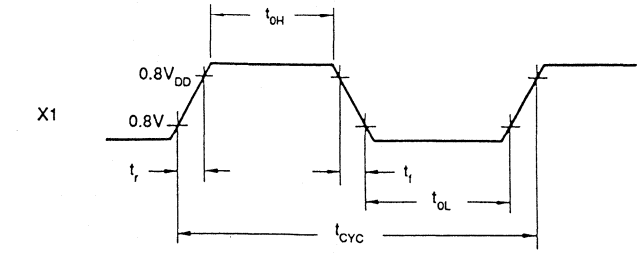
Interrupt Input Timing



Reset Input Timing



External Clock Timing



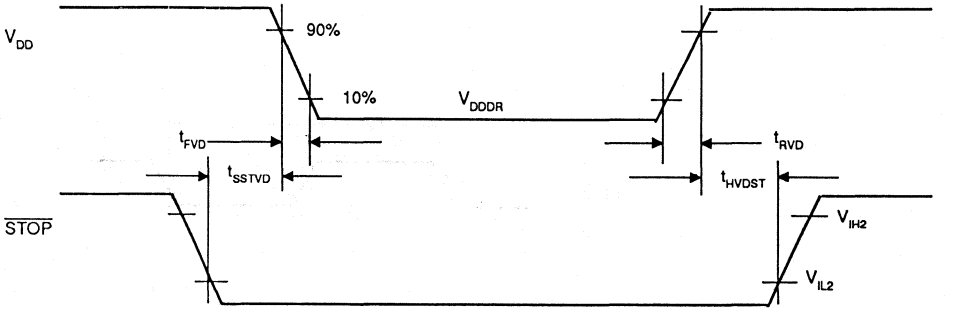
3

Data retention characteristics of low supply-voltage, data memory data retention STOP mode (Ta = -40 to +85 °C)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}		2.5		5.5	V
Data retention supply voltage	I_{DDDR}	V_{DDDR} = 2.5V			300	μA
		V_{DDDR} = 5V ± 5 %			1	mA
V_{DD} rise and fall times	t_{RVD}, t_{FVD}		200			μs
$\overline{STOP}$ setup time (vs. V_{DD})	t_{SSTVD}		12T + 0.5			μs
$\overline{STOP}$ hold time (vs. V_{DD})	t_{HVDST}		12T + 0.5			μs

Remarks: T = t_{CYC} = 1/f_{XX}

Data retention timing



DC Programming Characteristics
T_a = 25°C ± 5°C, MODE1 = V_{IL}, MODE0 = V_{IH}, V_{SS} = 0V)

Parameter	Symbol	Symbol *	Test condition	MIN.	TYP.	MAX.	Unit
Input high voltage	V_{IH}	V_{IH}		2.2		V_{DDP} +0.3	V
Input low voltage	V_{IL}	V_{IL}		–0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	$0 \le V_I \le V_{DDP}$; except for INT1, TI (PC3)			±10	μA
Output high voltage	V_{OH}	V_{OH}	I_{OH} = –1.0 mA	V_{DD} –1.0			V
Output low voltage	V_{OL}	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output leakage current	I_{LO}	—	$0 \le V_O \le V_{DDP}$, $\overline{OE}$ = V_{IH}			±10	μA
V_{DD} power supply voltage	V_{DDP}	V_{DD}	EPROM programming mode	5.75	6.0	6.25	V
			EPROM read mode	4.5	5.0	5.5	V
V_{PP} power supply voltage	V_{PP}	V_{PP}	EPROM programming mode	12.2	12.5	12.8	V
			EPROM read mode	V_{PP} = V_{DDP}			V
V_{DDP} power supply current	I_{DD}	I_{DD}	EPROM programming mode			1)	mA
			EPROM read mode $\overline{CE}$ = V_{IL}, V_I = V_{IH}			1)	mA
V_{PP} power supply current	I_{PP}	I_{PP}	EPROM programming mode $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			1)	mA
			EPROM read mode		1	1)	μA

Note *: Corresponding μPD27C256A symbols.

Note 1) to be measured on final silicon.

AC Programming Characteristics
T_a = 25°C ± 5°C, MODE1 = V_{IL}, V_{SS} = 0V)

Parameter	Symbol	Symbol *1	Test condition	MIN.	TYP.	MAX.	Unit
Address setup time to $\overline{CE}$ ↓	t_{SAC}	t_{AS}		2			μs
Data → $\overline{OE}$ ↓ delay time	t_{DDOO}	t_{OES}		2			μs
Input data setup time to $\overline{CE}$ ↓	t_{SIDC}	t_{DS}		2			μs
Address hold time from $\overline{CE}$ ↑	t_{HCA}	t_{AH}		2			μs
Input data hold time from $\overline{CE}$ ↑	t_{HCID}	t_{DH}		2			μs
Output data hold time from $\overline{OE}$ ↑	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} setup time to $\overline{CE}$ ↓	t_{SVPC}	t_{VPS}		2			μs
V_{DDP} setup time to $\overline{CE}$ ↓	t_{SVDC}	t_{VDS}		2			μs
Initial program pulse with	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Added program pulse with	t_{WL2}	t_{OPW}		2.85		78.75	ms
EPROM programming/read mode setup time to CE ↓ (*2)	t_{SMC}	—		2			μs

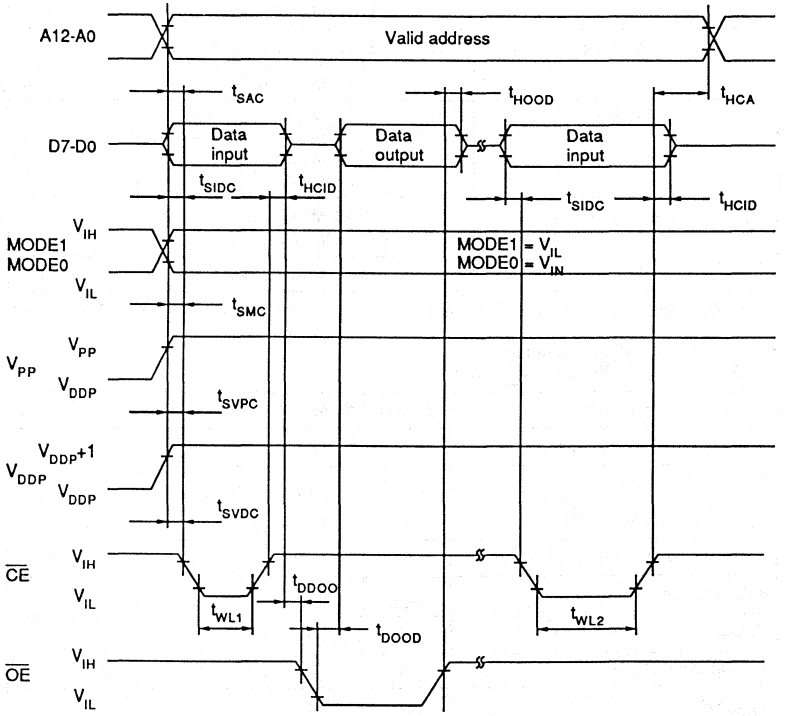
3

AC Programming Characteristics (Cont'd)
T_a = 25°C ± 5°C, MODE1 = V_{IL}, V_{SS} = 0V)

Parameter	Symbol	Symbol *1	Test condition	MIN.	TYP.	MAX.	Unit
Address → data output time	t_{DAOD}	t_{ACC}	$\overline{OE}$ = V_{IL}			2	μs
$\overline{CE}$ ↓ → data output time	t_{DCOD}	t_{CE}				1	μs
$\overline{OE}$ ↓ → data output time	t_{DOOD}	t_{OE}				1	μs
Data hold time from $\overline{OE}$ ↑	t_{HCOD}	t_{DF}		0		130	ns
Data hold time from address	t_{HAOD}	t_{OH}	$\overline{OE}$ = V_{IL}	0			ns

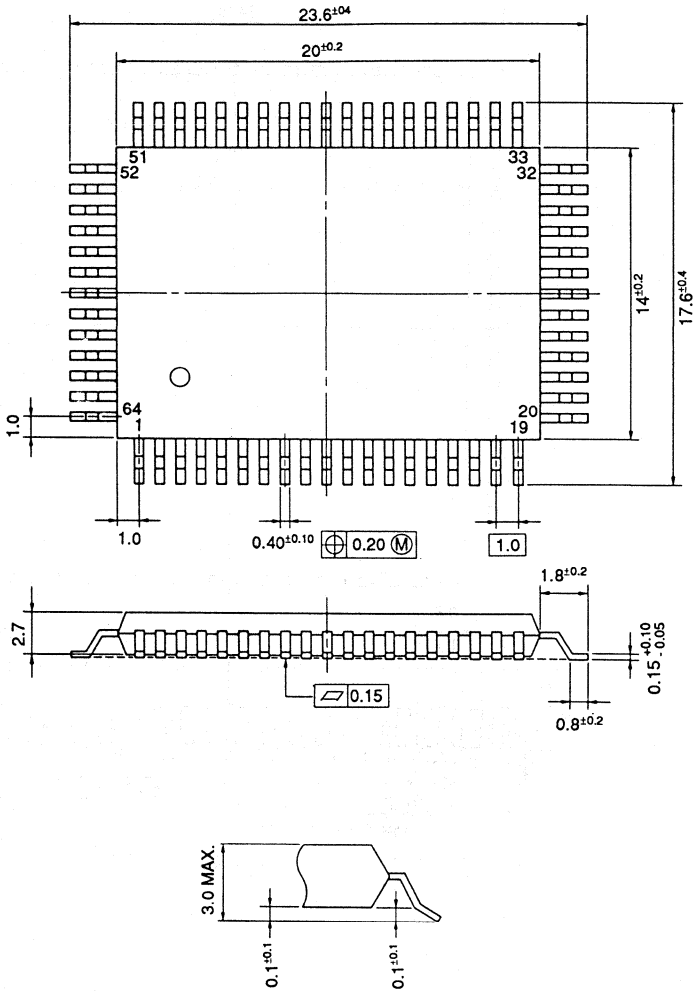
Note *1: Corresponding μPD27C256A symbols.
Note *2: When MODE1 = V_{IL} and MODE0 = V_{IH}.

EPROM Programming Mode Timing



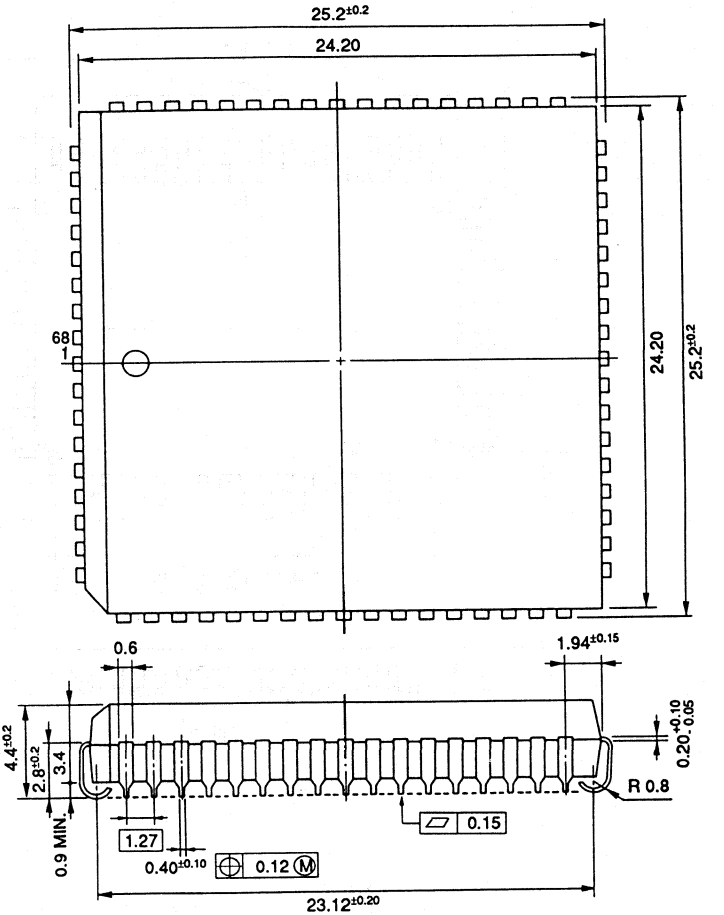
Caution 1: Apply voltage to V_{DDP} before V_{PP} and turn off V_{DDP} after V_{PP}.
Caution 2: Do not apply voltage of 12.8 V or more containing overshoot to V_{PP}.

64 - Pin FLAT PACK



3

68 - Pin LCC


25.2±0.2
24.20
68
1
24.20
25.2±0.2
0.6
1.94±0.15
4.4±0.2
2.8±0.2
3.4
0.9 MIN.
0.20 +0.10 -0.05
R 0.8
0.15
1.27
0.40±0.10
0.12 M
23.12±0.20

EPROM Erase Procedure (only Products with Ceramic Window)

The EPROM contents can be erased by light rays whose wavelength is shorter than about 400nm. The programmed EPROM data contents may also be erased if the uncovered window is exponsed to direct sunlight or a fluorescent light for several hours. Thus, to protect the data contents, cover the μPD78CP18 with an opaque film so as to prevent ultraviolet rays from entering through the top window.

For normal EPROM erase, place the μPD78PC18 under an ultraviolet light source (254nm). The minimum amount of radiation exposure required to erase the μPD78PC18 completely is 15 W.s/cm^2 (ultraviolet ray strength x erase time). This corresponds to about 15 to 20 minutes when using a ultraviolet ray lamp of 12000 μW/cm^2. However, note that the erase time may be prolonged by aging of the ultraviolet lamp, dirty package window, etc. The distance between the ultraviolet lamp and the μPD78PC18 should be within 2,5 cm.

CMOS-DESIGN RECOMMENDATIONS

In order to maximize circuit reliability please note the general CMOS design rules.

For example:

1) Don't leave unused pins open, except they are outputs or not connected.

2) Never exceed the max. voltage range.

3) Avoid accurance of very fast voltage spikes or transission rate the power supply pin.

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

Parameter	Symbol	Test Condition	Ratings	Unit
Power Supply Voltage	V_{DD}		−0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD} + 0.5	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to V_{DD} +0.5	V
Output Voltage	V_O		−0.5 to V_{DD} +0.5	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−2.0	mA
		All Output Pin Total	−50	mA
Reference Input Voltage	V_{AREF}		−0.5 to AV_{DD} +0.3	V
Operating Temperature	T_{opt}	$f_{XTAL} \leqq$ 15MHz	−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OPERATING CONDITION

OSC frequency \ Parameter	Ta	V_{DD}, AV_{DD}
$f_{XTAL} \leqq$ 15MHZ	−40°C to +85°C	+5.0V ± 10%

CAPACITANCE

(T_a = 25°C, $V_{DD} = V_{SS}$ = 0V)

Paramater	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Input Capacitance	C_I	f_C = 1MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	C_{IO}				20	pF

3

(T_a = −40 to +85 °C, V_{DD} = AV_{DD} = 5V ± 10%, V_{SS} = AV_{SS} = 0V, V_{DD} − 0.8V ≤ AV_{DD} ≤ V_{DD}, 3.4V ≤ V_{AREF} ≤ AV_{DD})

OSCILLATION CHARACTERISTICS

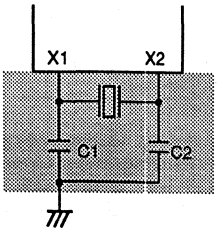
Resonator	Recommended Circuit	Parameters	Test Conditions	MIN	TYP	MAX	UNIT
Ceramic*1 Resonator or XTAL*2	(*3)	Oscillation Frequency (f_{XX})	A/D Converter Not used	4		15	MHz
			A/D Converter Used	5.8		15	MHz
External Clock	(*4)	X1 Input Frequency (f_X)	A/D Converter Not used	4		15	MHz
			A/D Converter Used	5.8		15	MHz
		X1 Input Rise, Fall Time (t_r,t_f)		0		20	ns
		X1 Input High, Low Level Width (t_H, T_L)		20		250	ns

* 1: Recommended ceramic resonators and external capacitance, as follows.

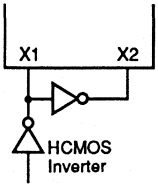
	Manufacturer	Product name	Recommended circuit constants (pF)	
			C1	C2
15 MHz	Murata	CSA15.0X3	22	22
		CSA12.0MT	30	30
		CST12.0MT	On-chip	On-chip
		CSA10.0MT	30	30
		CST10.0MT	On-chip	On-chip
		CSA6.00MG	30	30
		SCT6.00MG	On-chip	On-chip
	TDK	FCR12.0MC	On-chip	On-chip
12 MHz	Murata	CSA12.0MT18	30	30
		CST12.0MT18	On-chip	On-chip

* 2: For XTAL, the following external capacitances are recommended:
C1 = C2 = 10 pF

* 3:



* 4:



Note 1: Oscillator circuti should be in the nearest area from X1 and X2 pins.
Note 2: Do not place other signal lines in the range of ▨.

(T_a = -40°C to +85°C, V_{DD} = +5.0V±10%, V_{SS} = 0V)

DC CHARACTERISTICS

Parameter	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL1}	All except RESET, STOP, NMI, SCK, INT 1, TI, AN4 to 7	0		0.8	V
	V_{IL2}	RESET, STOP, NMI, SCK, INT1, TI, AN4 to 7	0		$0.2V_{DD}$	V
Input High Voltage	V_{IH1}	All except RESET, STOP, NMI, SCK, INT1, TI, AN4 to 7, X1, X2	2.2		V_{DD}	V
	V_{IH2}	RESET, STOP, NMI, SCK, INT1, TI, AN4 to 7, X1, X2	$0.8V_{DD}$		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	V_{DD}-1.0			V
		I_{OH} = -100μA	V_{DD}-0.5			V
Input Current	I_I	INT1, TI (PC3); $0V \leq V_I \leq V_{DD}$			±200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3), $0V \leq V_I \leq V_{DD}$			±10	μA
Output Leakage Current	I_{LO}	$0V \leq V_O \leq V_{DD}$			±10	μA
AV_{DD} Supply Current	AI_{DD}			1)	1)	mA
AV_{DD} Supply Current	AI_{DD2}	STOP MODE		1)	1)	μA
V_{DD} Supply Current	I_{DD1}	Operation mode f=15MHz		1)	1)	mA
	I_{DD2}	HALT MODE f=15 MHz		1)	1)	mA
Data Retention Voltage	V_{DDDR}	Hardware/Software STOP MODE	2.5			V
Data Retention Current	I_{DDDR}	Hardware/Software STOP Mode, V_{DDDR} = 2,5V		1)	1)	μA
		V_{DDDR} = 5V±10%		1)	1)	μA

Note 1) to be measured on final silicon.

3

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = -40°C to +85°C, V_{DD} = + 5.0 V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	MIN	MAX	Unit
X1 Input Cycle Time	t_{CYC}		66	250	ns
Address Setup to ALE↓	t_{AL}	*3, *4	30		ns
Adress Hold after ALE↓	t_{LA}	*3, *4	35		ns
Adress to $\overline{RD}$↓ Delay Time	t_{AR}	*3, *4	100		ns
$\overline{RD}$↓ to Address Floating	t_{AFR}	*4		20	ns
Adress to Data Input	t_{AD}	*3, *4		250	ns
ALE↓ to Data Input	t_{LDR}	*3, *4		135	ns
$\overline{RD}$↓ to Data Input	t_{RD}	*3, *4		120	ns
ALE to $\overline{RD}$↓ Delay Time	t_{LR}	*3, *4	15		ns
Data Hold after $\overline{RD}$↑	t_{RDH}	*4	0		ns
$\overline{RD}$↑ to ALE↑ Delay Time	t_{RL}	*3, *4	80		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read, *3, *4	215		ns
		OP code Fetch, *3, *4	415		ns
ALE Width High	t_{LL}	*3, *4	90		ns
$\overline{M1}$ Setup time to ALE↓	t_{ML}	*3	30		ns
$\overline{M1}$ Hold Time after ALE↓	t_{LM}	*3	35		ns
$\overline{IO}$/M Setup Time to ALE↓	t_{IL}	*3	30		ns
$\overline{IO}$/M Hold Time after ALE↓	t_{LI}	*3	35		ns
Address to $\overline{WR}$↓ Delay	t_{AW}	*3, *4	100		ns
ALE↓ to Data Output	t_{LDW}	*3, *4		180	ns
$\overline{WR}$↓ to Data Output	t_{WD}	*4		100	ns
ALE to $\overline{WR}$↓ Delay	t_{LW}	*3, *4	15		ns
Data Setup Time to $\overline{WR}$↑	t_{DW}	*3, *4	165		ns
Data Hold Time after $\overline{WR}$↑	t_{WDH}	*3, *4	60		ns
$\overline{WR}$↑ to ALE ↑ Delay Time	t_{WL}	*3, *4	80		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *4	215		ns

AC CHARACTERISTICS
SERIAL OPERATION

Parameter	Symbol	Test Condition		MIN	MAX	UNIT
$\overline{SCK}$ Cycle Time	tCYK	$\overline{SCK}$ Input	*5	800		ns
			*6	400		ns
		$\overline{SCK}$ Output		1.6		μs
$\overline{SCK}$ Width Low	tKKL	$\overline{SCK}$ Input	*5	335		ns
			*6	160		ns
		$\overline{SCK}$ Output		700		ns
$\overline{SCK}$ Width High	tKKH	$\overline{SCK}$ Input	*5	335		ns
			*6	160		ns
		$\overline{SCK}$ Output		700		ns
RxD Setup Time to $\overline{SCK}$↑	tRXK	*5		80		ns
RxD Hold Time After $\overline{SCK}$↑	tKRX	*5		80		ns
$\overline{SCK}$↓ to TxD Delay Time	tKTX	*5			210	ns

A/D CONVERTER
CHARACTERISTICS

(T_a = −40°C to +85°C, V_{DD} = 5.0V ± 10%, AV_{DD} = +5.0V ± 10%, V_{SS} = AV_{SS} = 0V,
V_{DD} −0.5V ≤ AV_{DD} ≤ V_{DD}, 3.4V ≤ VA_{REF} ≤ AV_{DD})

Parameter	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Resolution			8			Bits
Absolute Accuracy *1		3.4V ≤ VA_{REF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.8	%FSR
		4.0V ≤ VA_{REF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.6	%FSR
		T_a = −10 to +70°C, 4.0V ≤ VA_{REF} ≤ AV_{DD}, 66ns ≤ t_{CYC} ≤ 170ns			±0.4	%FSR
Conversion time	t_{CONV}	66ns ≤ t_{CYC} ≤ 110ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling Time	t_{SAMP}	66ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
Reference Voltage	V_{AREF}		3.4		AV_{DD}	V
V_{AREF} Current	I_{AREF1}	Operation mode		1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} Supply Current	AI_{DD1}	Operation mode, f_{XX} = 15MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA

*1: Except quantization error (i.e. ±1/2 LSB).

3

ZERO-CROSS CHARACTERISTICS

(T_a = -40°C to +85°C, V_{DD} = +5.0V±10%, V_{SS} = 0V)

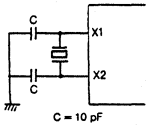
Parameter	Symbol	Test Condition	MIN	MAX	UNIT
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60Hz Sine Wave		±135	mV
Zero-Cross Detection Input Frequency	f_{ZX}		0.05	1	kHz

OTHER OPERATIONS

(T_a = -40°C to +85°C, V_{DD} = +5.0V ± 10%, V_{SS} = 0V)

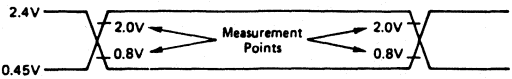
Parameter	Symbol	Test Condition	MIN	MAX	UNIT
TI width high, low	t_{TIH}, t_{TIL}		6		t_{CYC}
CI width high, low	t_{CI1H}, t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ width high, low	t_{NIH}, t_{NIL}		10		μs
INT1 width high, low	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ width high, low	t_{I2H}, t_{I2L}		36		t_{CYC}
$\overline{RESET}$ width high, low	t_{RSH}, t_{RSL}		10		μs

*1. For XTAL oscillation, following circuit is recommended.



*2. T_a = +25°C, V_{DD} = 5 V
*3. f_{XTAL} = 15MHZ
*4. Load Capacitance: C_L = 150pF
*5. x1 Clock Rate in Asynchronous Mode, Synchronous Mode, I/O Interface Mode
*6. x16, x64 Clock Rate in Asynchronous Mode

AC TIMING MEASUREMENT POINT



BUS TIMING DEPENDING ON t_{CYC}

Symbol	Calculating Expression	MIN./MAX.	units
t_{AL}	2T - 100	MIN	ns
t_{LA}	T - 30	MIN	ns
t_{AR}	3T - 100	MIN	ns
t_{AD}	7T - 220	MAX	ns
t_{LDR}	5T - 200	MAX	ns
t_{RD}	4T - 150	MAX	ns
t_{LR}	T - 50	MIN	ns
t_{RL}	2T - 50	MIN	ns
t_{RR}	4T - 50 (Data Read)	MIN	ns
	7T - 50 (OP Code Fetch)		
t_{LL}	2T - 40	MIN	ns
t_{ML}	2T - 100	MIN	ns
t_{LM}	T - 30	MIN	ns
t_{IL}	2T - 100	MIN	ns
t_{LI}	T - 30	MIN	ns
t_{AW}	3T - 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T - 50	MIN	ns
t_{DW}	4T - 100	MIN	ns
t_{WDH}	2T - 70	MIN	ns
t_{WL}	2T - 50	MIN	ns
t_{WW}	4T - 50	MIN	ns
t_{CYK}	12T ($\overline{SCK}$ Input) *1	MIN	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	5T + 5 ($\overline{SCK}$ Input) *1	MIN	ns
	12T - 100 ($\overline{SCK}$ Output)		
t_{KKH}	5T + 5 ($\overline{SCK}$ Input) *2	MIN	ns
	12T - 100 ($\overline{SCK}$ Output)		

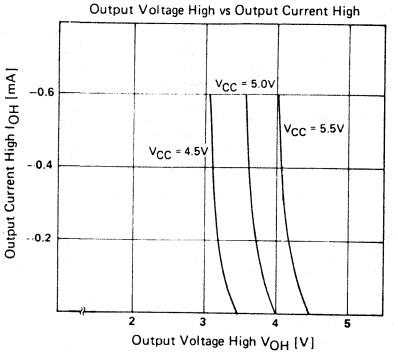
Note 1. In case of x1 clock rate in asynchronous mode, synchronous mode, or I/O interface mode.
2. $T = t_{CYC} = 1/f_{XTAL}$
3. Parameters which can't be found in this table don't depend on oscillation frequency (f_{XTAL}).

3

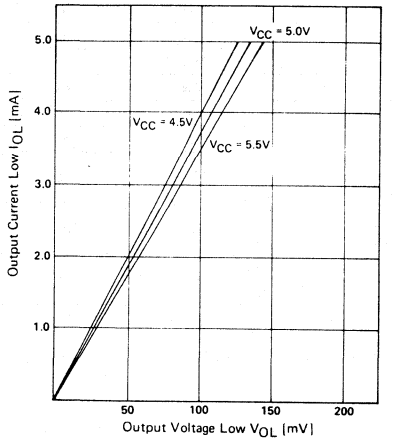
CHARACTERISTICS CURVE
– REFERENCE –

(T_a = 25°C)

Output Voltage High vs Output Current High

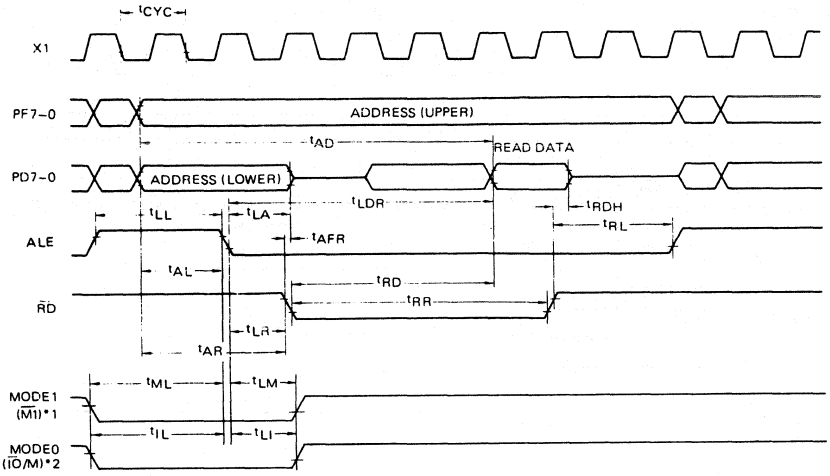


Output Voltage Low vs Output Current Low



TIMING WAVEFORM

Read Operation



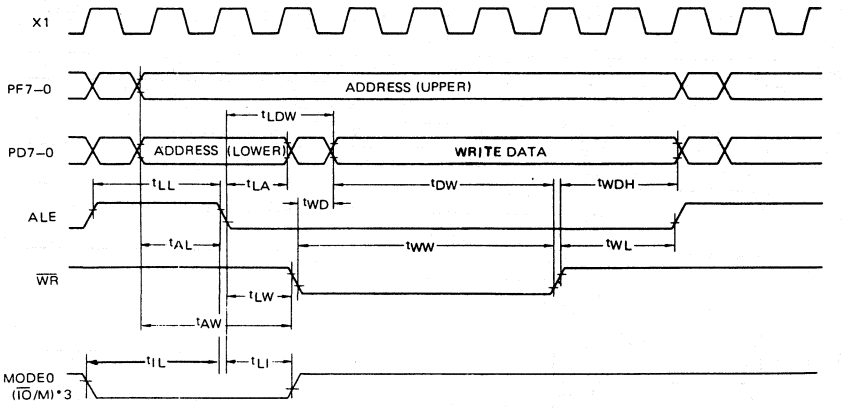
*1 $\overline{M1}$ is output at the fetech cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

*2 $\overline{IO}$/M is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

3

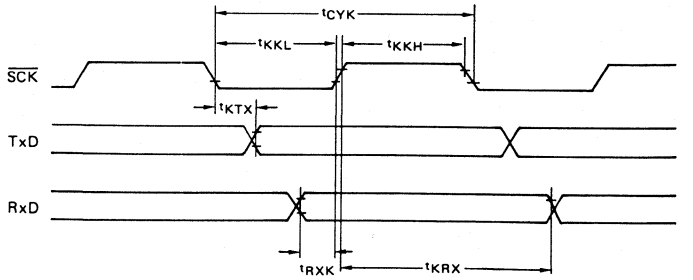
TIMING WAVEFORM

Write Operation

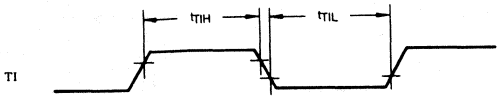


*3 $\overline{IO}$/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Serial Operation

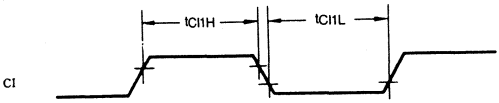


TIMER INPUT TIMING

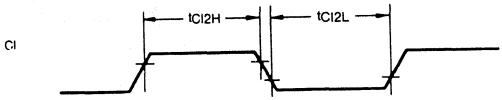


TIMER/EVENT COUNTER INPUT TIMING

EVENT COUNT MODE

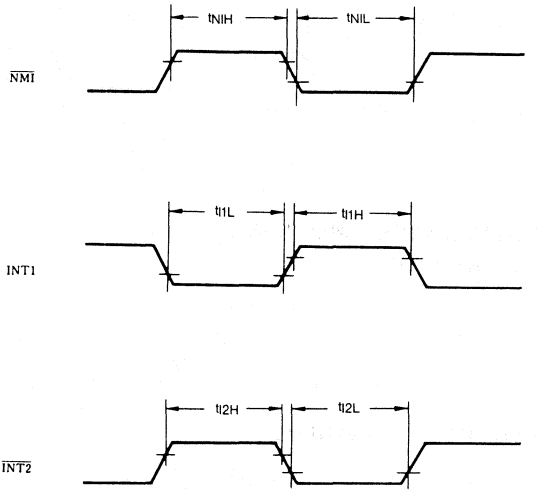


PULSE WIDTH MEASUREMENT MODE

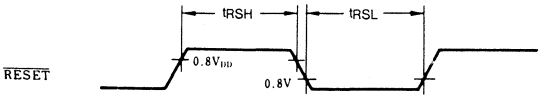


3

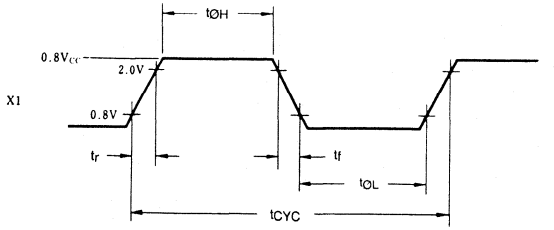
INTERRUPT INPUT TIMING



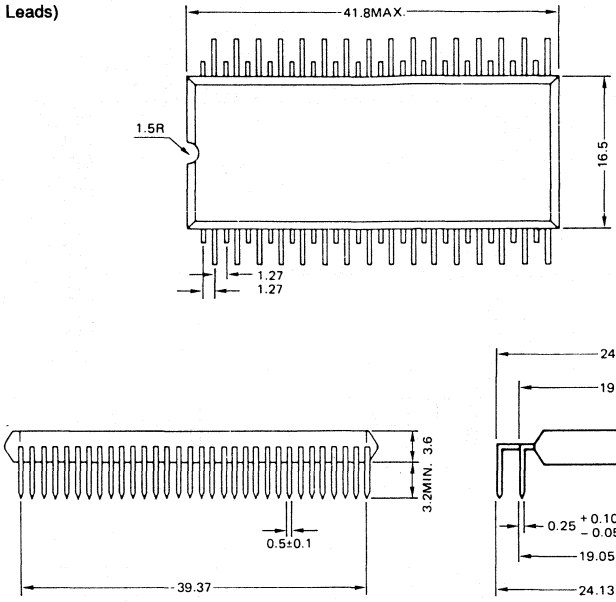
RESET INPUT TIMING



EXTERNAL CLOCK TIMING

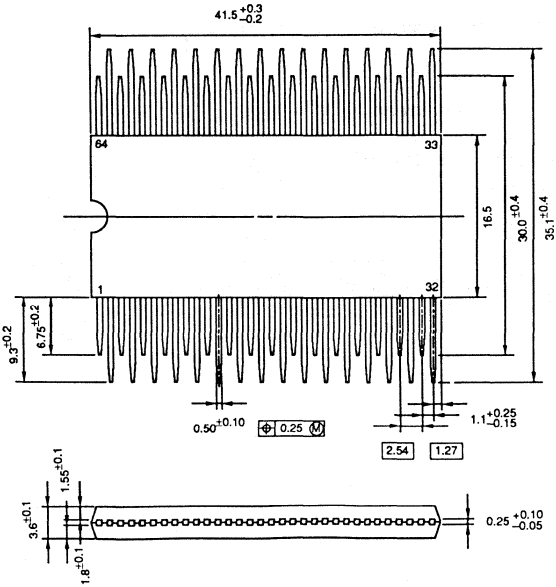


64-PIN PLASTIC QUIP (Bent Leads)
OUTLINE (Units: mm)
μPD78C17GQ
μPD78C18GQ

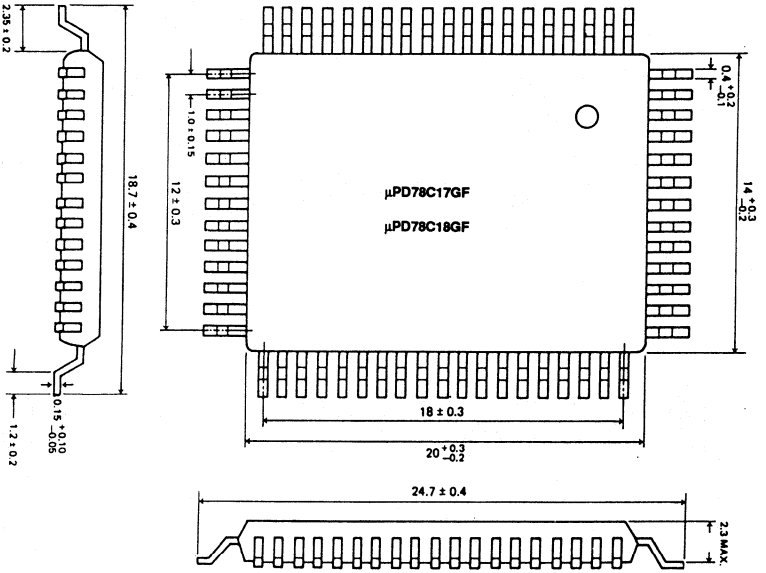


When ordering this package, specify as follows:
μPD78C17GQ-36
μPD78C18GQ-XXX-36

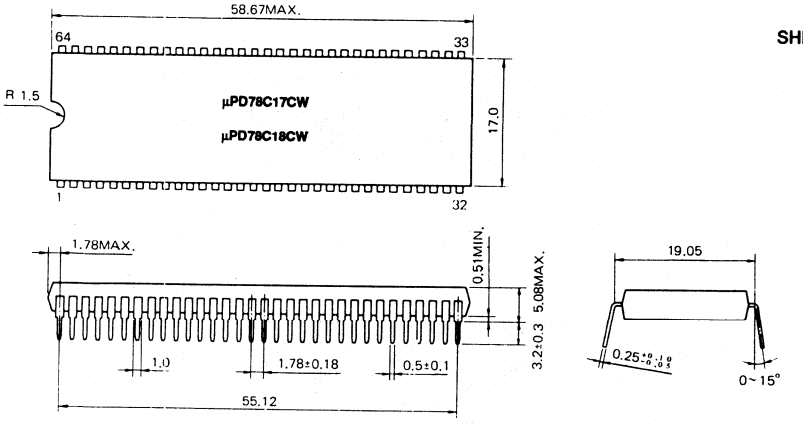
64 PIN PLASTIC
QUIP STRAIGHT LEADS
PACKAGE DIMENSIONS
(Units: mm)



64-PIN PLASTIC
FLAT PACK OUTLINE
(Unit: mm)
μPD78C17GF
μPD78C18GF



64-PIN PLASTIC
SHRINK DIP OUTLINE
(Unit: mm)
μPD78C17CW
μPD78C18CW



Section 4: The μCOM84 Family

Section 4 – The μCOM84 Family

8-BIT, SINGLE-CHIP NMOS MICROCOMPUTERS WITH UNIVERSAL PPI

DESCRIPTION

The μPD8041AH and μPD8741A are programmable peripheral interface controllers intended for use in master/slave configurations with 8048, 8080A, 8085A, 8086, and other 8- and 16-bit microprocessors. The μPD8041AH/8741A functions as a totally self-sufficient controller with its own program and data memory to effectively unburden the master CPU from I/O handling and peripheral control functions.

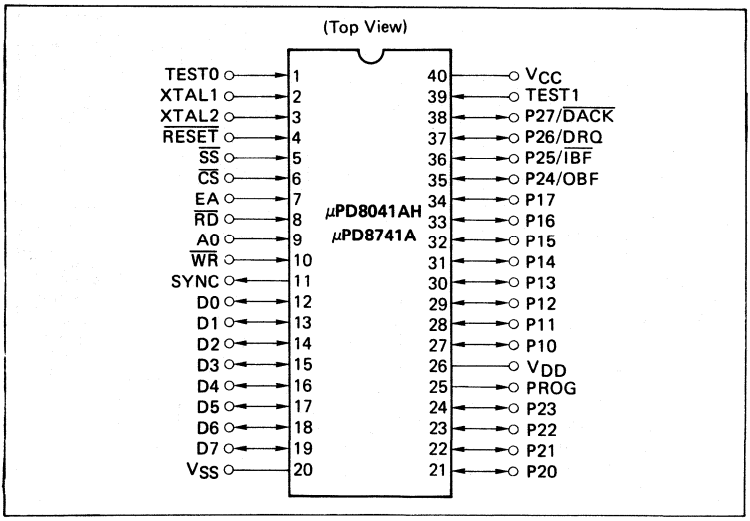
The bus structure and data and status registers of the μPD8041AH/8741A allow easy interface to the master processor bus. This enables the processor to perform control tasks which offload main system processing and more efficiently distribute processing functions.

The μPD8041AH/8741A contains an 8-bit CPU, 1K x 8 program memory, 64 x 8 data memory, 18 I/O lines, a counter/timer, and a clock generator. The program memory for the μPD8041AH is factory maskprogrammed, while program memory for the μPD8741A is UV EPROM for more flexibility.

FEATURES

- Complete single chip microcomputer
  - 8-bit CPU
  - 1K x 8 ROM / UVPROM
  - 64 x 8 RAM
  - 8-bit timer/counter
  - 18 I/O lines
- 8048-, 8080A-, 8085A-, 8086-compatible bus structure
- Asynchronous slave-to-master interface
  - 8-bit status register
  - Two data registers
- Interrupt, DMA, or polled operation
- Expandable I/O
- Single +5V power supply (8041AH)

PIN CONFIGURATION

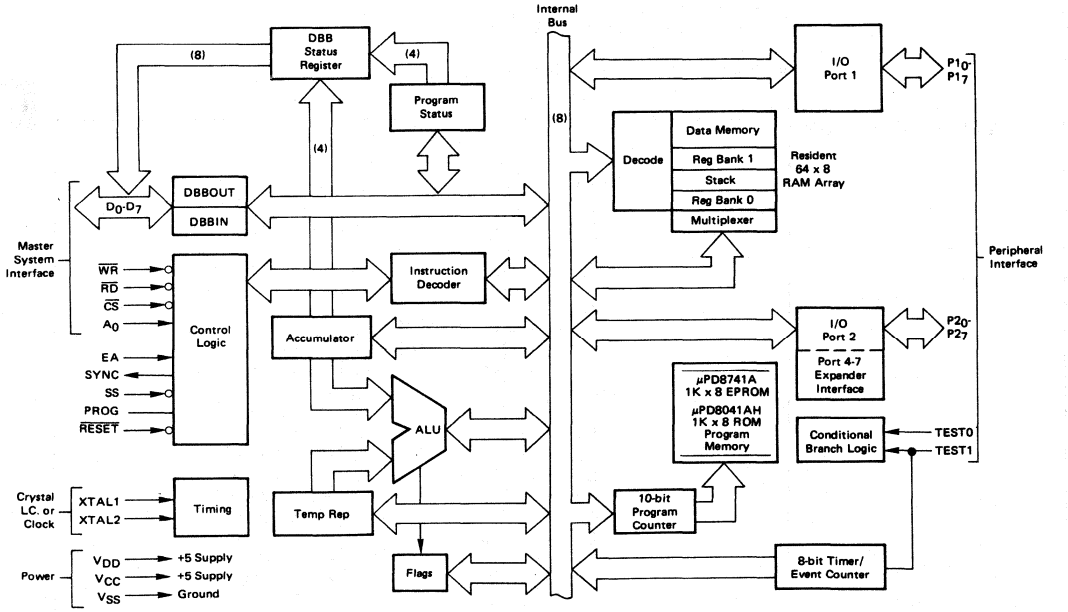


4

PIN IDENTIFICATION

NO.	SYMBOL	FUNCTION
1	T0	Testable input 0
2	XTAL1	Crystal input 1
3	XTAL2	Crystal input 2
4	$\overline{RESET}$	Reset input
5	$\overline{SS}$	Single step input
6	$\overline{CS}$	Chip select input
7	EA	External access input
8	$\overline{RD}$	Read strobe input
9	A_0	Adress input 0
10	$\overline{WR}$	Write strobe output
11	SYNC	SYNC output
12–19	D_0–D_7	Bidirectional data bus
20	V_{SS}	Ground potential
21–24, 35–38	$P2_0$–$P2_7$	Quasi-bidirectional Port 2
25	PROG	Program pulse output
26	V_{DD}	Programming supply voltage
27–34	$P1_0$–$P1_7$	Quasi-bidirectional Port 1
39	T1	Testable input 1
40	V_{CC}	Primary power supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C

Power supply voltage, V_{CC}	−0.5V to +7.0V
Power supply voltage, V_{DD}	−0.5V to +7.0V
Input voltage, V_{IN}	−0.5V to +7.0V
Output voltage, V_O	−0.5V to +7.0V
Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input capacitance	C_I				10	pF
Output Capacitance	C_{IO}				20	pF

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	μPD8741A		μPD8041AH		UNIT
			MIN	MAX	MIN	MAX	
Input voltage low	V_{IL}	All except X1, X2, and $\overline{RESET}$	−0.5	0.8	−0.5	0.8	V
	V_{IL1}	X1, X2, $\overline{RESET}$	−0.5	0.6	−0.5	0.6	V
Input voltage high	V_{IH}	Except X1, X2, and $\overline{RESET}$	2.0	V_{CC}	2.0	V_{CC}	V
	V_{IH1}	X1, X2, $\overline{RESET}$	3.8	V_{CC}	3.8	V_{CC}	V
Output voltage low	V_{OL}	D_0–D_7, SYNC, I_{OL} = 2.0 mA		0.45		0.45	V
	V_{OL1}	Except PROG, I_{OL} = 1.0 mA		0.45		0.45	V
	V_{OL2}	PROG, I_{OL} = 1.0 mA		0.45		0.45	V
Output voltage high	V_{OH}	D_0–D_7, I_{OH} = −400 μA	2.4		2.4		V
	V_{OH1}	All other outputs: I_{OH} = −50 μA	2.4		2.4		V
Input current low	I_{LI}	$P1_0$–$P1_7$, $P2_0$–$P2_7$; V_{IL} = 0.8V		0.5		0.5	mA
	I_{LI1}	$\overline{SS}$, $\overline{RESET}$; V_{IL} = 0.8V		0.2		0.2	mA
Input leakage current	I_{IL}	T0, T1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, EA, A_0, $V_{SS} \leq V_{IN} \leq V_{CC}$		± 10		± 10	μA
Output leakage current	I_{OL}	D_0–D_7, High Z state, V_{SS} +0.45 V ≤ V_{IN} ≤ V_{CC}		± 10		± 10	μA
Supply current (total)	I_{DD}	V_{DD}		15		15	mA
	I_{DD} + I_{CC}			135		125	mA

4

AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

DBB READ

PARAMETER	SYMBOL	TEST CONDITIONS	μPD8741A		μPD8041AH		UNIT
			MIN	MAX	MIN	MAX	
$\overline{CS}$, A_0 setup to $\overline{RD}$ ↓	t_{AR}		0		0		ns
$\overline{CS}$, A_0 hold after $\overline{RD}$ ↑	t_{RA}		0		0		ns
$\overline{RD}$ pulse width	t_{RR}		250		160		ns
$\overline{CS}$, A_0, to data out delay	t_{AD}	μPD8741A: C_L = 150 pF μPD8041AH: C_L = 100 pF		225		130	ns
$\overline{RD}$ ↓ to data out delay	t_{RD}	μPD8741A: C_L = 150 pF μPD8041AH: C_L = 100 pF		225		130	ns
$\overline{RD}$ ↑ to data float delay	t_{DF}			100		85	
Cycle time	t_{CY}		2.5	15	1.36	15	ns

DBB WRITE

PARAMETER	SYMBOL	TEST CONDITIONS	μPD8741A		μPD8041AH		UNIT
			MIN	MAX	MIN	MAX	
$\overline{CS}$, A_0 setup to $\overline{WR}$ ↓	t_{AW}		0		0		ns
$\overline{CS}$, A_0 hold after $\overline{WR}$ ↑	t_{WA}		0		0		ns
$\overline{WR}$ pulse width	t_{WW}		250		160		ns
Data setup to $\overline{WR}$ ↑	t_{DW}		150		130		ns
Data hold after $\overline{WR}$ ↑	t_{WD}		0		0		ns

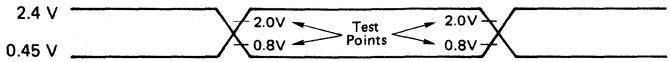
PORT 2

PARAMETER	SYMBOL	TEST CONDITIONS	μPD8741A		μPD8041AH		UNIT
			MIN	MAX	MIN	MAX	
Port control setup to PROG ↓	t_{CP}	μPD8041AH: C_L = 80 pF	110		100		ns
Port control hold after PROG ↓	t_{PC}	μPD8041AH: C_L = 20 pF	100		60		ns
Input data setup to PROG ↓	t_{PR}	μPD8041AH: C_L = 80 pF		810		650	ns
Input data hold time	t_{PF}	μPD8041AH: C_L = 20 pF	0	150	0	150	ns
Output data setup time	t_{DP}	μPD8041AH: C_L = 80 pF	250		200		ns
Output data hold time	t_{PD}	μPD8041AH: C_L = 20 pF	65		65		ns
PROG pulse with	t_{PP}		1200		700		ns

DMA

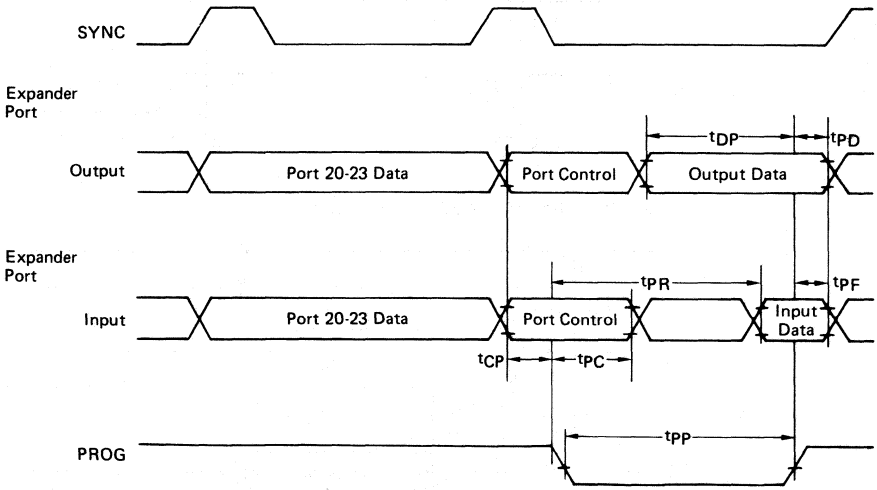
PARAMETER	SYMBOL	TEST CONDITIONS	μPD8741A		μPD8041AH		UNIT
			MIN	MAX	MIN	MAX	
$\overline{DACK}$ setup time to $\overline{RD}$, $\overline{WR}$	t_{ACC}		0		0		ns
$\overline{DACK}$ hold time after $\overline{RD}$, $\overline{WR}$	t_{CAC}		0		0		ns
Data output delay after $\overline{DACK}$	t_{ACD}	μPD8741A: C_L = 150 pF		225		130	ns
DRQ clear delay time after $\overline{RD}$, $\overline{WR}$	t_{CRQ}	μPD8041AH: C_L = 100 pF		200		130	ns

AC TIMING TEST POINTS

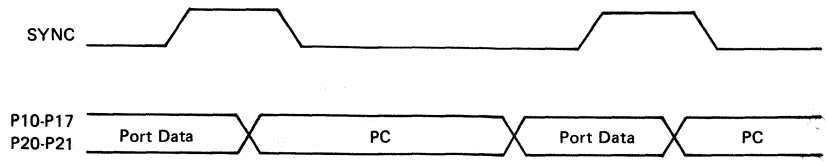


TIMING WAVEFORMS

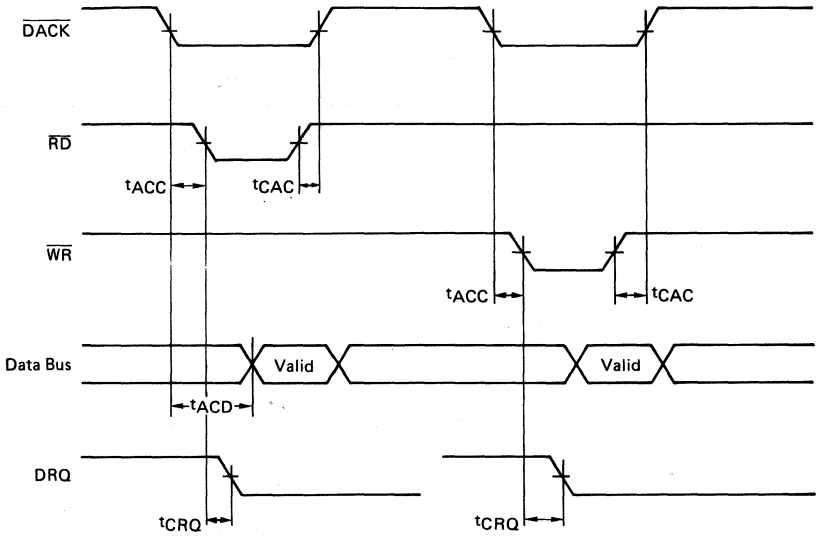
PORT 2



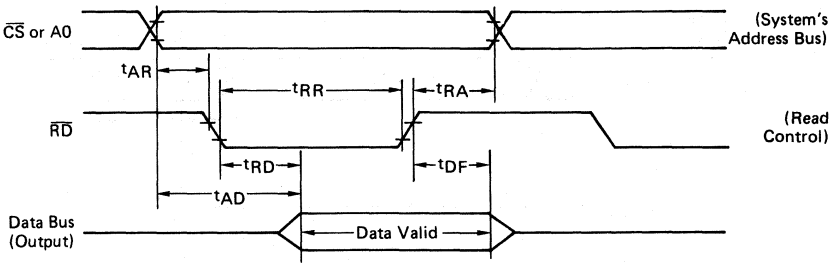
PORT (EA = 1)



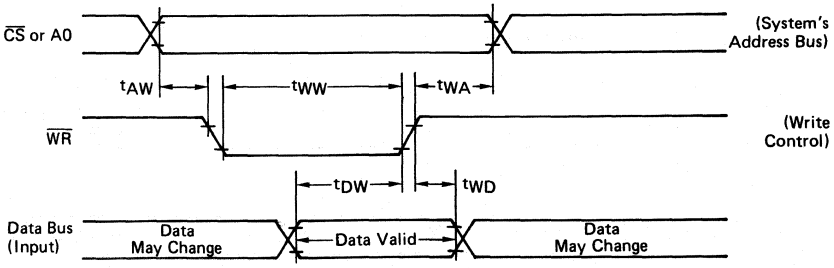
DMA



READ OPERATION (DBBOUT REGISTER)



WRITE OPERATION (DBBIN REGISTER)



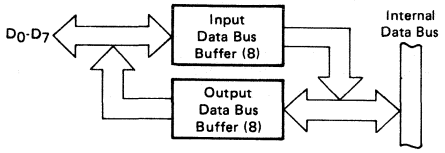
FUNCTIONAL DESCRIPTION

Two data bus buffers, an 8-bit status register, the $\overline{RD}$ and $\overline{WR}$ inputs, and expandable I/O lines enhance the μPD8041AH/8741A. These features enable easier master/slave interface and increased functionality.

DATA BUS BUFFERS

Figure 1 shows how the input and output data bus buffers enable a smooth data flow to and from the master processors.

Figure 1. Data Bus Buffers



STATUS REGISTER

The 8-bit status register includes four user-definable bits, ST_4–ST_7. Use the MOV STS, A instruction (90H) to define bits ST_4–ST_7 by moving accumulator bits 4–7 to bits 4–7 of the status register. Bits ST_0–ST_3 are not affected.

Figure 2 shows the format of the status register.

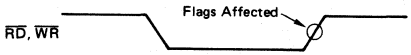
Figure 2. Status register Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
ST_7	ST_6	ST_5	ST_4	F1	F0	IBF	OBF

$\overline{RD}$ AND $\overline{WR}$

The $\overline{RD}$ and $\overline{WR}$ inputs are edge-sensitive. Figure 3 shows that status bits $\overline{IFB}$, OBF, F1, and F0 are affected on the trailing edge at $\overline{RD}$ or $\overline{WR}$.

Figure 3. $\overline{RD}$ and $\overline{WR}$ inputs



PORT 2_4–PORT 2_7

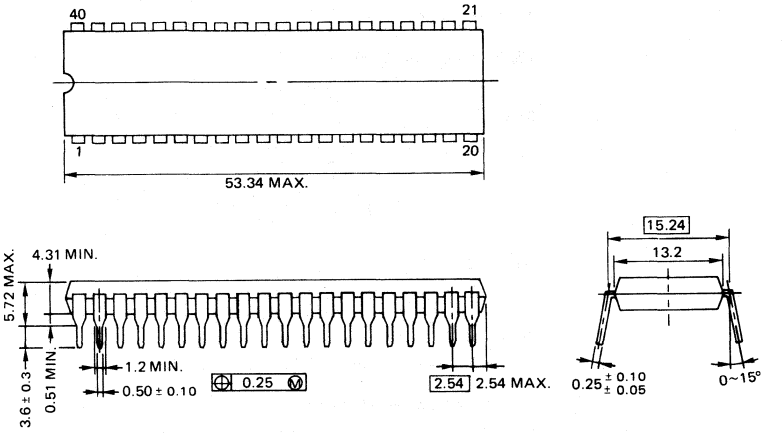
$P2_4$ and $P2_5$ can be used as either port lines or buffer status flag lines. This allows you to make OBF and $\overline{IBF}$ status available externally to interrupt the master processor. Upon execution of the EN FLAGS instruction (F5H), $P2_4$ becomes the OBF pin. When a 1 is written to $P2_4$, the OBF pin is enabled and the status of OBF is output. A0 to $P2_4$ disables the OBF pin AND the pin remains low. This pin indicates valid data is available from the μPD8041AH/8741A.

An EN FLAGS instruction execution also enables $P2_5$ to indicate that the μPD8041AH/8741A is ready to accept data. A1 written to $P2_5$ enables the $\overline{IBF}$ pin and the status of $\overline{IBF}$ is available on $P2_5$. A0 written to $P2_5$ disables the $\overline{IBF}$ pin. If OBF is not true, the data at the data bus is invalid.

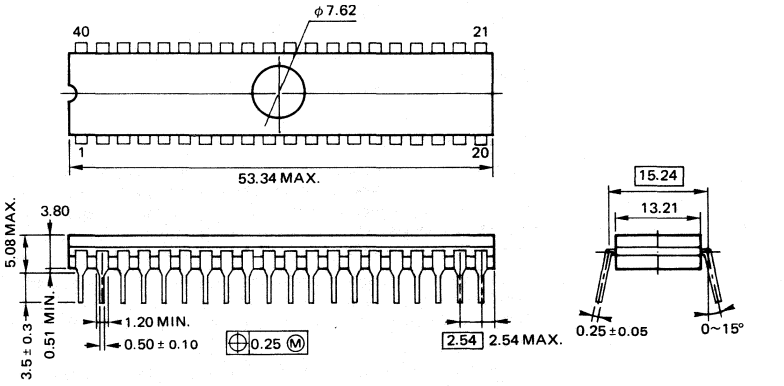
$P2_6$ and $P2_7$ can be used as either port lines or DMA handshake lines to allow DMA interface. The EN DMA instruction (E5H) enables $P2_6$ and $P2_7$ to be used as DRQ (DMA request) and $\overline{DACK}$ (DMA acknowledge), respectively.

When a 1 is written to $P2_6$, DRQ is activated and a DMA request is issued. The EN DMA instruction deactivates DRQ. You can also deactivate DRQ by adding $\overline{DACK}$ with $\overline{RD}$ or $\overline{WR}$. Execution of the EN DMA instruction enables $P2_7$ ($\overline{DACK}$) to function as a chip select input for the data bus buffer registers during DMA transfers.

40-PIN PLASTIC DIP PACKAGE
OUTLINE (Unit : mm)
μPD8041AHC–XXX



40-PIN CERAMIC DIP PACKAGE
OUTLINE (Unit : mm)
μPD8741AD



HIGH-SPEED, 8-BIT, SINGLE-CHIP HMOS MICROCOMPUTERS

DESCRIPTION

The μPD8035HL and the μPD8048H make up the μPD8048H family of single-chip 8-bit microcomputers. The processors in this family differ only in their internal program memory options: the μPD8048H with 1K x 8 bytes of mask ROM and the μPD8035HL with external memory.

The NEC μPD8035HL and μPD8048H are single component, 8-bit, parallel microprocessors using n-channel silicon gate MOS technology. The μPD8048H family of components functions efficiently in control as well as in arithmetic applications. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

The μPD8035HL/48H instruction set comprises 1 and 2 byte instructions with over 70 % of them single-byte. Execution requires only 1 or 2 cycles per instruction and over 50 % are single-cycle instructions.

The functions of the μPD8048H series of microprocessors can easily be expanded using standard 8080A/8085A peripherals and memories.

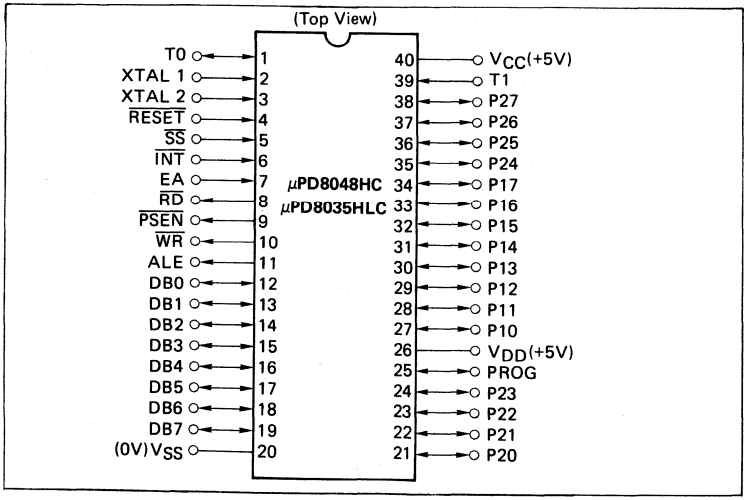
The μPD8048H contains the following functions usually found in external peripheral devices: 1024 x 8 bits of ROM program memory; 64 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

The μPD8035HL is intended for applications using external program memory only. It contains all the features of the μPD8048H except the 1024 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

FEATURES

- Fully compatible with industry standard 8048/8748/8035
- 2.5 μs cycle time: all instructions 1 or 2 bytes
- Interval timer/event counter
- 64 x 8-byte RAM data memory
- External and timer interrupts
- 96 instructions: 70 % single byte
- 27 I/O lines
- Internal clock generator
- 8 level stack
- Compatible with 8080A/8085A peripherals
- HMOS silicon gate technology
- Single +5V power supply

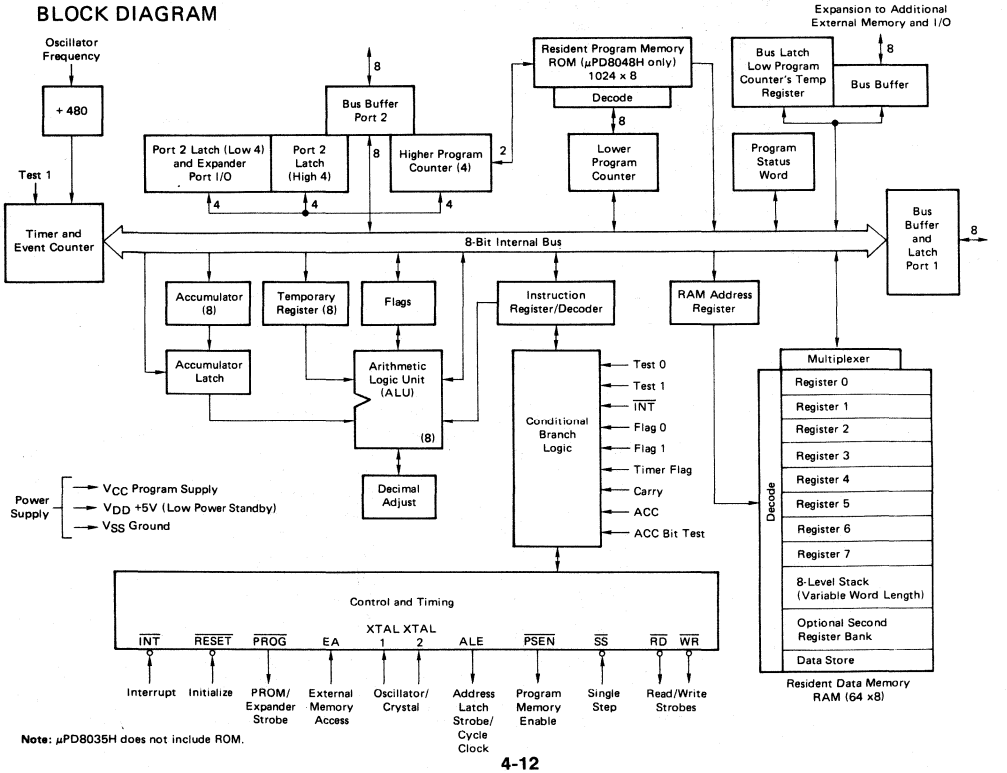
PIN CONFIGURATION



PIN IDENTIFICATION

NO.	SYMBOL	FUNCTION
1	T0	Test 0 input/output
2	XTAL1	Crystal 1 input
3	XTAL2	Crystal 2 input
4	$\overline{\text{RESET}}$	Reset input
5	$\overline{\text{SS}}$	Single step input
6	$\overline{\text{INT}}$	Interrupt input
7	EA	External access input
8	$\overline{\text{RD}}$	Read output
9	$\overline{\text{PSEN}}$	Program store enable output
10	$\overline{\text{WR}}$	Write output
11	ALE	Address latch enable output
12–19	DB_0–DB_7	Bidirectional data bus
20	V_{SS}	Ground
21–24, 35–38	$P2_0$–$P2_7$	Quasi-bidirectional Port 2
25	$\overline{\text{PROG}}$	Program output
26	V_{DD}	RAM power supply
27–34	$P1_0$–$P1_7$	Quasi-bidirectional Port 1
39	T1	Test 1 input
40	V_{CC}	Primary power supply

BLOCK DIAGRAM



Note: μPD8035H does not include ROM.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C

Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Voltage on any pin, $V_{I/O}$	−0.5V to +7V (Note 1)
Power dissipation, P_D	1.5W

Note:

(1) With respect to ground.

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input low voltage (All except XTAL1, XTAL2)	V_{IL}		−0.5		0.8	V
Input low voltage ($\overline{RESET}$, X1, X2)	V_{IL1}		−0.5		0.8	V
Input high voltage (All except XTAL1, XTAL2, $\overline{RESET}$)	V_{IH}		2.0		V_{CC}	V
Input high voltage (XTAL1, XTAL2, $\overline{RESET}$)	V_{IH1}		3.8		V_{CC}	V
Output low voltage (Bus)	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output low voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
Output low voltage ($\overline{PROG}$)	V_{OL2}	I_{OL} = 2.0 mA			0.45	V
Output low voltage (all other outputs)	V_{OL3}	I_{OL} = 2.0 mA			0.45	V
Output high voltage (Bus)	V_{OH}	I_{OH} = −400 μA	2.4			V
Output high voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH1}	I_{OH} = −400 μA	2.4			V
Output high voltage (all other outputs)	V_{OH2}	I_{OH} = −40 μA	2.4			V
Input leakage current (T1, $\overline{INT}$)	I_{LI}	$V_{SS} \leq V_{IN} \leq V_{CC}$			± 10	μA
Input leakage current ($P1_0$–$P1_7$, $P2_0$–$P2_7$, EA, $\overline{SS}$)	I_{LI1}	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V			−500	μA
Output leakage current (Bus T0, high impedance state)	I_{OL}	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V			± 10	μA
Power down supply current	I_{DD}	T_A = 25°C		4	8	mA
Total supply current	I_{DD} + I_{CC}	T_A = 25°C		50	80	mA
RAM standby voltage	V_{DD}	Standby mode. Reset ≤ 0.6V	2.2		5.5	V

4

AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cycle time	t_{CY}	(Note 1)	2.5		15	μs
ALE pulse width	t_{LL}	(Note 1)	410			ns
Address setup to ALE	t_{AL}	(Note 1)	220			ns
Address hold from ALE	t_{LA}	(Note 1)	120			ns
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	(Note 1)	1050			ns
Control pulse width ($\overline{PSEN}$)	t_{CC2}	(Note 1)	800			ns
Data setup $\overline{WR}$	t_{DW}	(Note 1)	880			ns
Data hold after $\overline{WR}$	t_{WD}	(Note 2)	110			ns
Data hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	(Note 1)	0		220	ns
$\overline{RD}$ to data in	t_{RD1}	(Note 1)			800	ns
$\overline{PSEN}$ to data in	t_{RD2}	(Note 1)			550	ns
Address setup to $\overline{WR}$	t_{AW}	(Note 1)	680			ns
Address setup to data ($\overline{RD}$)	t_{AD1}	(Note 1)			1570	ns
Address setup to data ($\overline{PSEN}$)	t_{AD2}	(Note 1)			1090	ns
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	(Note 1)	290			ns
Address float to $\overline{PSEN}$	t_{AFC2}	(Note 1)	40			ns
ALE to control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	(Note 1)	420			ns
ALE to control ($\overline{PSEN}$)	t_{LAFC2}	(Note 1)	170			ns
Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t_{CA1}	(Note 1)	120			ns
Control to ALE ($\overline{PSEN}$)	t_{CA2}	(Note 1)	620			ns
Port control setup to $\overline{PROG}$	t_{CP}	(Note 1)	210			ns
Port control hold to $\overline{PROG}$	t_{PC}	(Note 1)	460			ns
$\overline{PROG}$ to P2 input valid	t_{PR}	(Note 1)			1300	ns
Input data hold from $\overline{PROG}$	t_{PF}	(Note 1)			250	ns
Output data setup	t_{DP}	(Note 1)	850			ns
Output data hold	t_{PD}	(Note 1)	200			ns
$\overline{PROG}$ pulse width	t_{PP}	(Note 1)	1500			ns
Port 2 I/O data setup to ALE	t_{PL}	(Note 1)	460			ns
Port 2 I/O data hold to ALE	t_{LP}	(Note 1)	150			ns
Port output from ALE	t_{PV}	(Note 1)			850	ns
T0 rep rate	t_{OPRR}	(Note 1)	500			ns

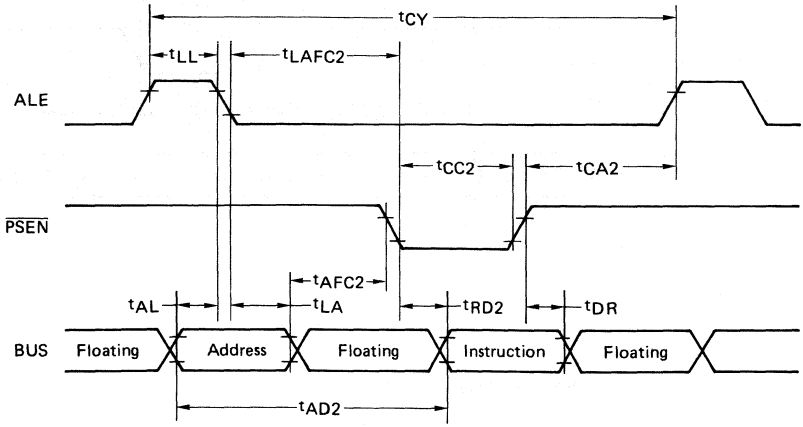
Note:

(1) Control outputs: C_L = 80 pF, bus outputs: C_L = 150 pF

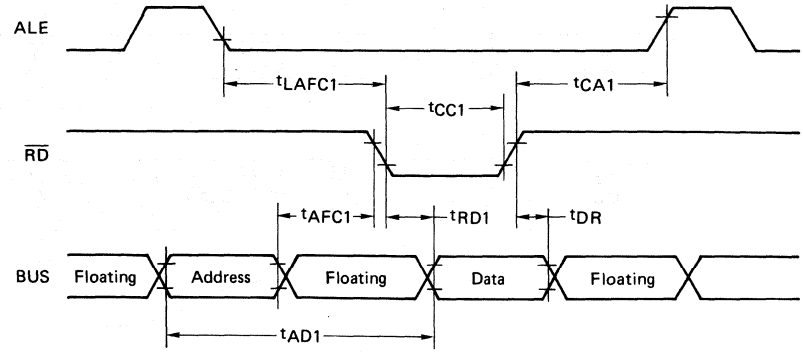
(2) Bus high impedance, load = 20 pF

TIMING WAVEFORMS

INSTRUCTION FETCH FROM EXTERNAL MEMORY

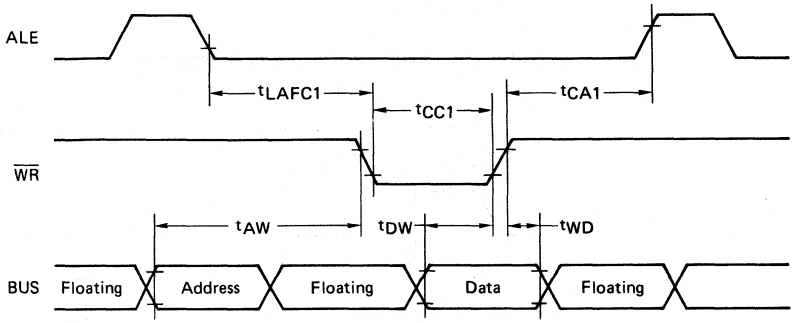


READ FROM EXTERNAL DATA MEMORY

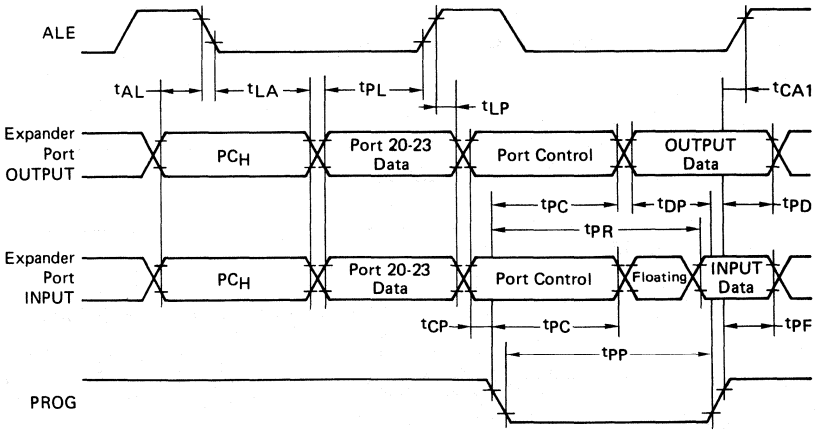


4

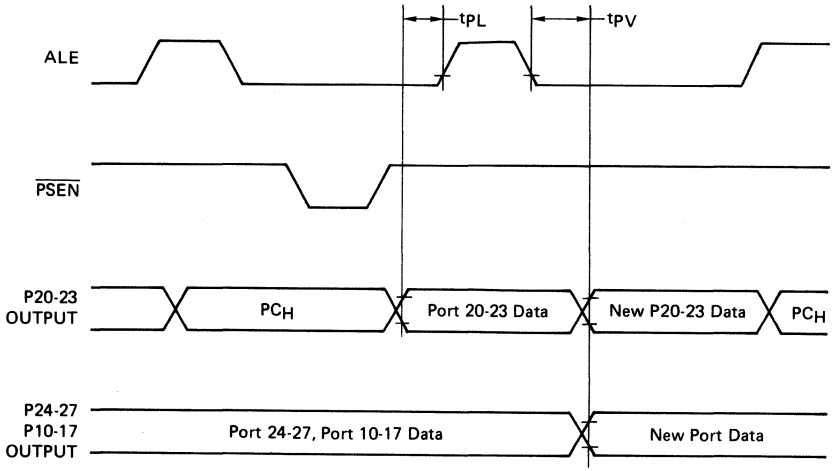
WRITE TO EXTERNAL MEMORY



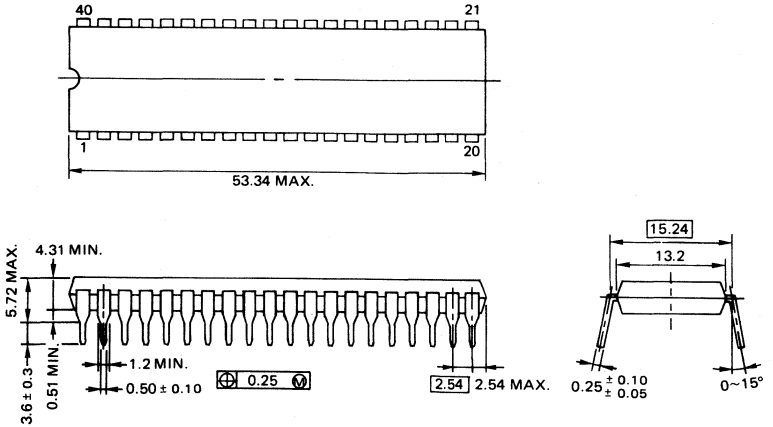
PORT 2 TIMING



I/O PORT TIMING



40-PIN PLASTIC DIP PACKAGE
OUTLINE (UNIT : mm)
μPD8035HLC
μPD8048HC –XXX



HIGH-SPEED, 8-BIT, SINGLE-CHIP NMOS MICROCOMPUTER WITH UV EPROM

DESCRIPTION

The μPD8748H is one of the μPD8048 family of single-chip 8-bit microcomputers. It is a high-speed NMOS processor that functions efficiently in control and arithmetic applications. The flexible instruction set allows you to directly set and reset individual data bits within the accumulator and the I/O ports. The variety of branch and table look-up instructions simplifies the implementation of standard logic functions.

The instruction set is made up of one- and two-byte instructions. Over 70 % are single-byte instructions that require only one or two cycles. Over 50 % require a single cycle.

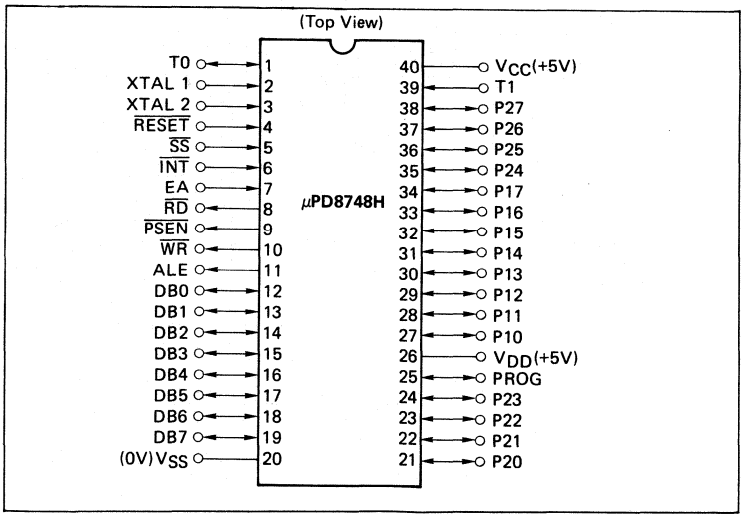
The μPD8048H functions as a stand-alone microcomputer. You can expand its functions with standard 8080A/8085A peripherals and memories. It contains 1024 x 8 bits of ROM program memory, 64 x 8 bits of RAM data memory, 27 I/O lines, an 8-bit internal timer/event counter, oscillator, and clock circuitry.

The μPD8748H differs from the μPD8048 in that it has 1K of on-board EPROM. This is useful in preproduction or prototype applications where the software is not complete or in system designs in quantities that do not require a mask ROM. See the μPD8048H/8035HL data sheet for more information.

FEATURES

- Low programming voltage
- Fully compatible with 8048/8748/8035
- NMOS silicon gate technology
- Single +5V supply
- 2.5μs cycle time
- 96 instructions; 70 % single byte
- Internal timer/event counter
- 64 x 8 byte RAM data memory
- Single interrupt level
- 27 I/O lines
- Internal clock generator
- 8-level stack
- Compatible with 8080A/8085A peripherals
- Available in one-time-programmable plastic package

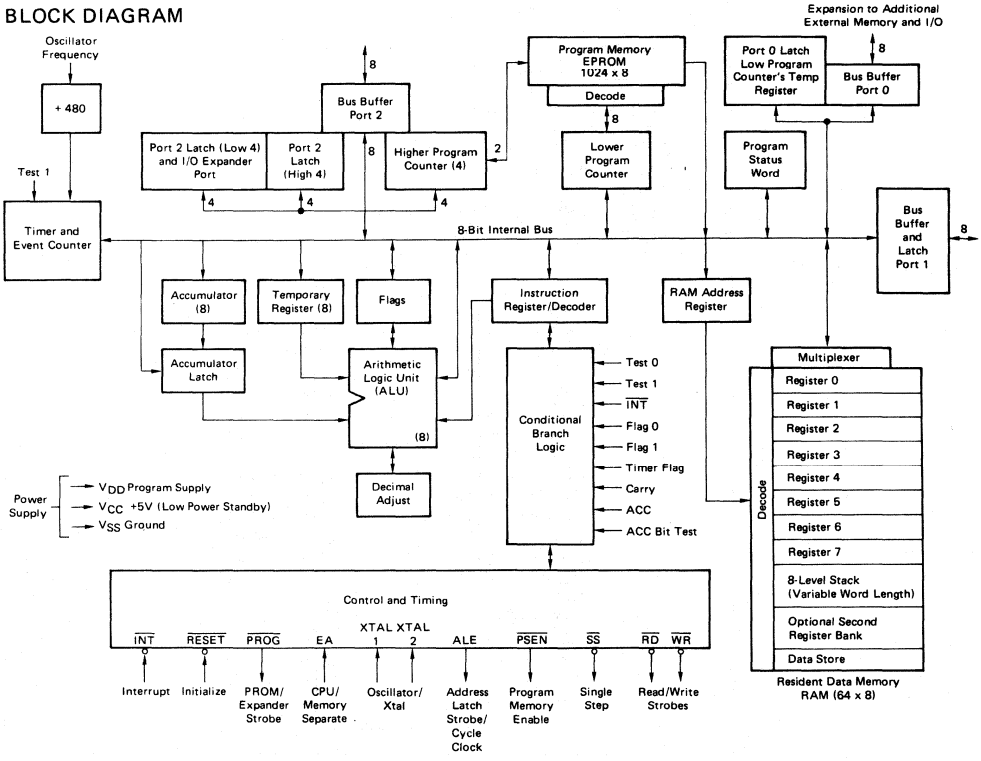
PIN CONFIGURATION



PIN IDENTIFICATION

NO.	SYMBOL	FUNCTION
1, 39	T0, T1	Testable inputs 0 and 1
2, 3	XTAL1, XTAL2	Crystal inputs
4	$\overline{\text{RESET}}$	System reset input
5	$\overline{\text{SS}}$	Single step input
6	$\overline{\text{INT}}$	Interrupt input
7	EA	External access input
8	$\overline{\text{RD}}$	Read strobe output
9	$\overline{\text{PSEN}}$	Program store enable output
10	$\overline{\text{WR}}$	Write strobe output
11	ALE	Address latch enable output
12–19	D_0–D_7	8-bit bidirectional port
20	V_{SS}	Ground
21–24, 35–38	$P2_0$–$P2_7$	8-bit quasibidirectional port 2
25	PROG	Program pulse input
26	V_{DD}	Programming power supply
27–34	$P1_0$–$P1_7$	8-bit quasibidirectional port 1
40	V_{CC}	Primary power supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C

Operating temperature, T_{OP}	0°C to +70°C
Storage temperature, T_{ST}	−65°C to +150°C
Output voltage, V_O	−0.5V to +7.0V
Input voltage, V_I	−0.5V to +7.0V
Power supply voltages, V_{CC}, V_{DD}	−0.5V to +7.0V

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input low voltage (except XTAL1, XTAL2, $\overline{RESET}$)	V_{IL}		−0.5		0.8	V
Input low voltage (XTAL1, XTAL2, $\overline{RESET}$)	V_{IL1}		−0.5		0.6	V
Input high voltage (except XTAL1, XTAL2, $\overline{RESET}$)	V_{IH}		2.0		V_{CC}	V
Input high voltage (XTAL1, XTAL2, $\overline{RESET}$)	V_{IH1}		3.8		V_{CC}	V
Output low voltage (Bus)	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output low voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}	I_{OL} = 1.8 mA			0.45	V
Output low voltage (PROG)	V_{OL2}	I_{OL} = 1.0 mA			0.45	V
Output low voltage (all other outputs)	V_{OL3}	I_{OL} = 1.6 mA			0.45	V
Output high voltage (Bus)	V_{OH}	I_{OH} = −400 μA	2.4			V
Output high voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH1}	I_{OH} = −100 μA	2.4			V
Output high voltage (all other outputs)	V_{OH2}	I_{OH} = −40 μA	2.4			V
Input leakage current (T1, $\overline{INT}$)	I_{LI}	$V_{SS} \leq V_I \leq V_{CC}$			± 10	μA
Input leakage current ($P1_0$–$P1_7$, $P2_0$–$P2_7$, EA, $\overline{SS}$)	I_{LI1}	V_{SS} +0.45V $\leq V_I \leq V_{CC}$			−500	μA
Output leakage current (Bus, T0, high impedance)	I_{LO}	V_{SS} +0.45V $\leq V_I \leq V_{CC}$			± 10	μA
Supply current (V_{DD})	I_{DD}			2	5	mA
Total supply current	$I_{DD} + I_{CC}$			85	110	mA

PROGRAMMING DC CHARACTERISTICS

T_A = 25°C ± 5°C, V_{CC} = +5V ± 5 %, V_{DD} = +21V ± 0.5V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD} voltage high level	V_{DDH}		20.5		21.5	V
V_{DD} voltage low level	V_{DDL}		4.75		5.25	V
PROG voltage high level	V_{PH}		17.5		18.5	V
PROG voltage low level	V_{PL}		4.0		V_{CC}	V
EA program/verify voltage high level	V_{EAH}		17.5		18.5	V
V_{DD} high voltage supply current	I_{DD}				20.0	mA
PROG high voltage supply current	I_{PROG}				1.0	mA
EA high voltage supply current	I_{EA}				1.0	mA

4

AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cycle time	t_{CY}		1.36		15.0	μs
ALE pulse width	t_{LL}	(1, 3)	150			ns
Address setup before ALE	t_{AL}	(1, 3)	70			ns
Address hold after ALE	t_{LA}	(1, 3)	50			ns
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	(1, 3)	480			ns
Control pulse width ($\overline{PSEN}$)	t_{CC2}	(1, 3)	350			ns
Data setup before $\overline{WR}$	t_{DW}	(1, 3)	390			ns
Data hold after $\overline{WR}$	t_{WD}	(1, 2, 3)	40			ns
Data hold after $\overline{RD}$, $\overline{PSEN}$	t_{DR}	(1, 3)	0		110	ns
$\overline{RD}$ to data in	t_{RD1}	(1, 3)			330	ns
$\overline{PSEN}$ to data in	t_{RD2}	(1, 3)			190	ns
Address setup before $\overline{WR}$	t_{AW}	(1, 3)	300			ns
Address setup before data in ($\overline{RD}$)	t_{AD1}	(1, 3)			730	ns
Address setup before data in ($\overline{PSEN}$)	t_{AD2}	(1, 3)			460	ns
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	(1, 3)	140			ns
Address float to $\overline{PSEN}$	t_{AFC2}	(1, 3)	10			ns
ALE to $\overline{RD}$, $\overline{WR}$ delay time	t_{LAFC1}	(1, 3)	200			ns
ALE to $\overline{PSEN}$ delay time	t_{LAFC2}	(1, 3)	60			ns
$\overline{RD}$, $\overline{WR}$, PROG to ALE delay time	t_{CA1}	(1, 3)	50			ns
$\overline{PSEN}$ to ALE delay time	t_{CA2}	(1, 3)	320			ns
Port 2 Timing						
Port control setup before PROG	t_{CP}	(1, 3)	100			ns
Port control hold after PROG	t_{PC}	(1, 3)	160			ns
Input data setup before PROG	t_{PR}	(1, 3)			650	ns
Input data hold after PROG	t_{PF}	(1, 3)	0		140	ns
Output data setup before PROG	t_{DP}	(1, 3)	400			ns
Output data hold after PROG	t_{PD}	(1, 3)	90			ns
PROG pulse width	t_{PP}	(1, 3)	700			ns
Port 2 I/O data setup before ALE	t_{PL}	(1, 3)	160			ns
Port 2 I/O data setup after ALE	t_{LP}	(1, 3)	15			ns
ALE to port output time	t_{PV}	(1, 3)			510	ns
T0 output cycle time	t_{OPRR}	(1, 3)	270			ns

Note:

(1) Control Output: C_L = 80 pF, Bus Output: C_L = 150 pF

(2) Bus high impedance, load = 20 pF

(3) Clock oscillation frequency, f_{OSC} = 11 MHz

PROGRAMMING AC CHARACTERISTICS

T_A = 25°C ± 5°C, V_{DD} = +21V ± 0.5V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Address setup before $\overline{RESET}$ ↑	t_{AW}		4 t_{CY}			
Address hold after $\overline{RESET}$ ↑	t_{WA}		4 t_{CY}			
Data input setup before PROG ↓	t_{DW}		4 t_{CY}			
Data input hold after PROG ↓	t_{WD}		4 t_{CY}			
$\overline{RESET}$ hold after verify	t_{PH}		4 t_{CY}			
V_{DD} setup before PROG ↑	t_{VDDW}		0		1.0	ms
V_{DD} hold after PROG ↓	t_{VDDH}		0		1.0	ms
PROG pulse width	t_{PW}		50		60	ms
TEST 0 setup before program mode	t_{TW}		4 t_{CY}			
TEST 0 hold after program mode	t_{WT}		4 t_{CY}			
TEST 0 to data output delay (1)	t_{DO}				4 t_{CY}	
$\overline{RESET}$ pulse width to latch address	t_{WW}		4 t_{CY}			
V_{DD} and PROG rise and fall times	t_r, t_f		0.5		100	μs
CPU cycle time	t_{CY}	4.0 μs/3.7 MHz	4.0		15	μs
$\overline{RESET}$ setup before EA ↑	t_{RE}		4 t_{CY}			

Note:

(1) If TEST 0 is high, t_{DO} is triggered by RESET ↑.

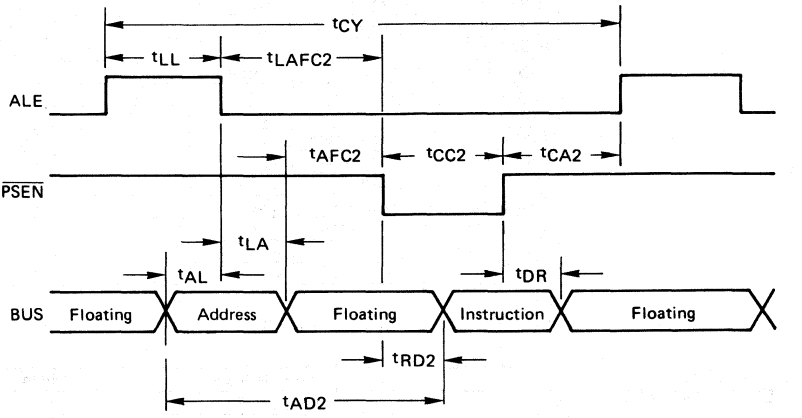
BUS TIMING REQUIREMENTS

SYMBOL	TIMING FORMULA	MIN/MAX	UNIT
t_{LL}	(7/30) t_{CY} −170	MIN	ns
t_{AL}	(2/15) t_{CY} −110	MIN	ns
t_{LA}	(1/15) t_{CY} − 40	MIN	ns
t_{CC1}	(1/ 2) t_{CY} −200	MIN	ns
t_{CC2}	(2/ 5) t_{CY} −200	MIN	ns
t_{DW}	(13/30) t_{CY} −200	MIN	ns
t_{WD}	(1/15) t_{CY} − 50	MIN	ns
t_{DR}	(1/10) t_{CY} − 30	MAX	ns
t_{RD1}	(11/13) t_{CY} −170	MAX	ns
t_{RD2}	(4/15) t_{CY} −170	MAX	ns
t_{AW}	(1/ 3) t_{CY} −150	MIN	ns
t_{AD1}	(7/10) t_{CY} −220	MAX	ns
t_{AD2}	(1/ 2) t_{CY} −220	MAX	ns
t_{AFC1}	(2/15) t_{CY} − 40	MIN	ns
t_{AFC2}	(1/30) t_{CY} − 40	MIN	ns
t_{LAFC1}	(1/ 5) t_{CY} − 75	MIN	ns
t_{LAFC2}	(1/10) t_{CY} − 75	MIN	ns
t_{CA1}	(1/15) t_{CY} − 40	MIN	ns
t_{CA2}	(4/15) t_{CY} − 40	MIN	ns
t_{CP}	(2/15) t_{CY} − 80	MIN	ns
t_{PC}	(4/15) t_{CY} −200	MIN	ns
t_{PR}	(17/30) t_{CY} −120	MAX	ns
t_{PF}	(1/10) t_{CY}	MAX	ns
t_{DP}	(2/ 5) t_{CY} −150	MIN	ns
t_{PD}	(1/10) t_{CY} − 50	MIN	ns
t_{PP}	(7/10) t_{CY} −250	MIN	ns
t_{PL}	(4/15) t_{CY} −200	MIN	ns
t_{LP}	(1/30) t_{CY} − 30	MIN	ns
t_{PV}	(3/10) t_{CY} + 100	MAX	ns
t_{OPRR}	(1/ 5) t_{CY}	MIN	ns
t_{CY}	(1/f_{OSC}) x 15		μs

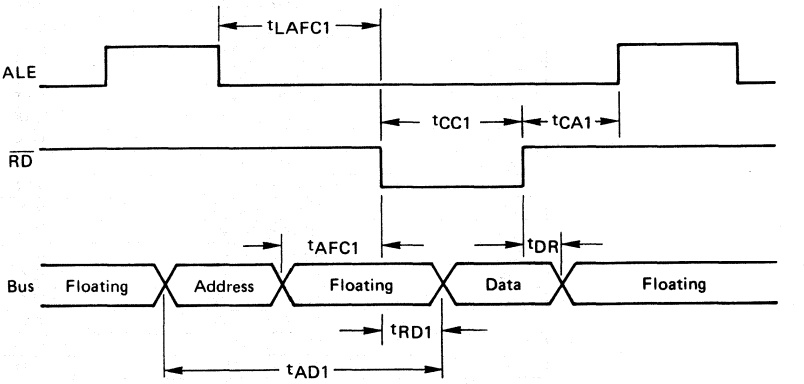
4

TIMING WAVEFORMS

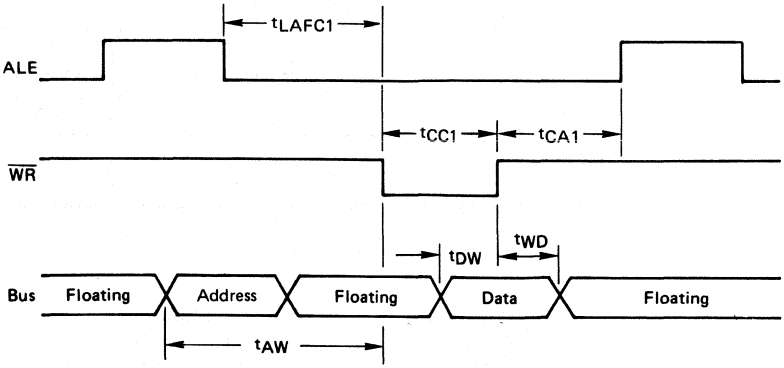
INSTRUCTION FETCH (EXTERNAL PROGRAM MEMORY)



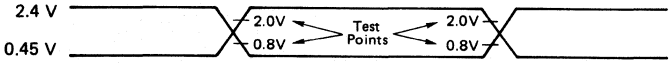
READ (EXTERNAL DATA MEMORY)



WRITE (EXTERNAL DATA MEMORY)

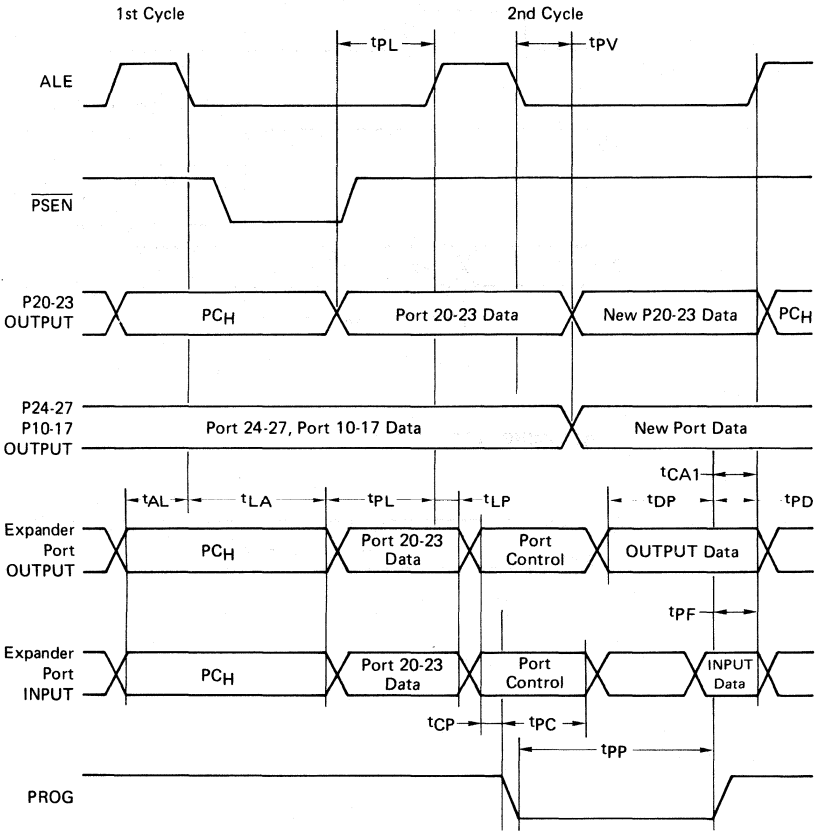


AC TIMING TEST POINTS

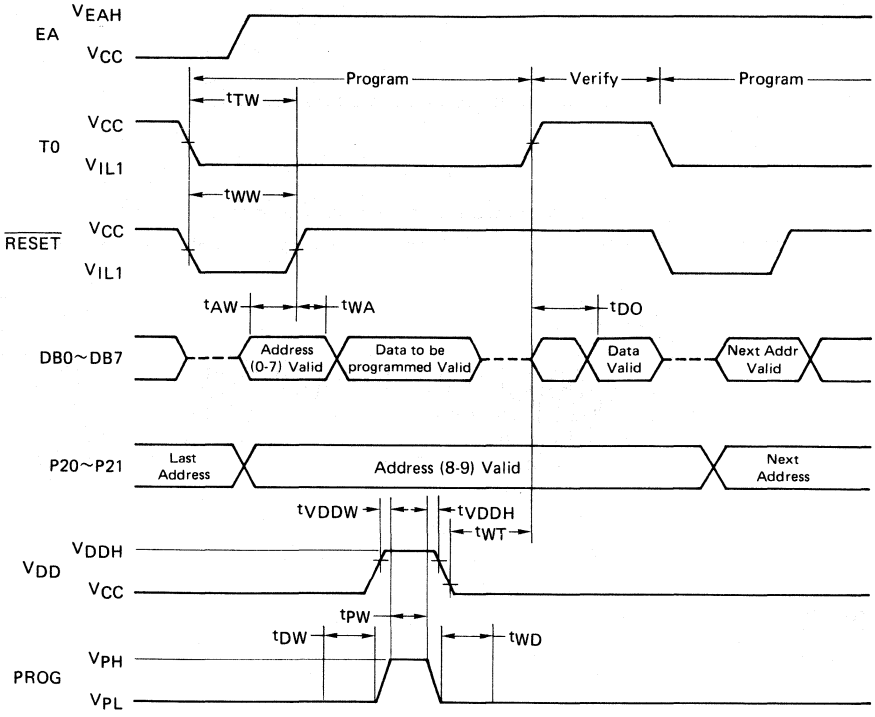


4

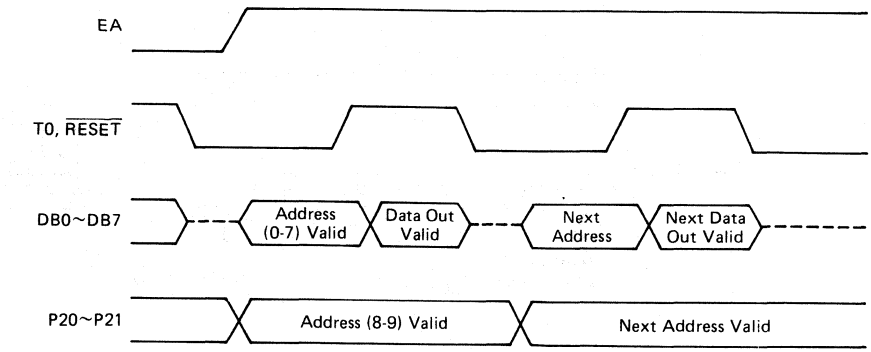
PORT 1/PORT 2


1st Cycle
2nd Cycle
tPL
tPV
ALE
PSEN
P20-23 OUTPUT
PCH
Port 20-23 Data
New P20-23 Data
PCH
P24-27 P10-17 OUTPUT
Port 24-27, Port 10-17 Data
New Port Data
tCA1
tAL
tLA
tPL
tLP
tDP
tPD
Expander Port OUTPUT
PCH
Port 20-23 Data
Port Control
OUTPUT Data
tPF
Expander Port INPUT
PCH
Port 20-23 Data
Port Control
INPUT Data
tCP
tPC
tPP
PROG

PROGRAM/VERIFY



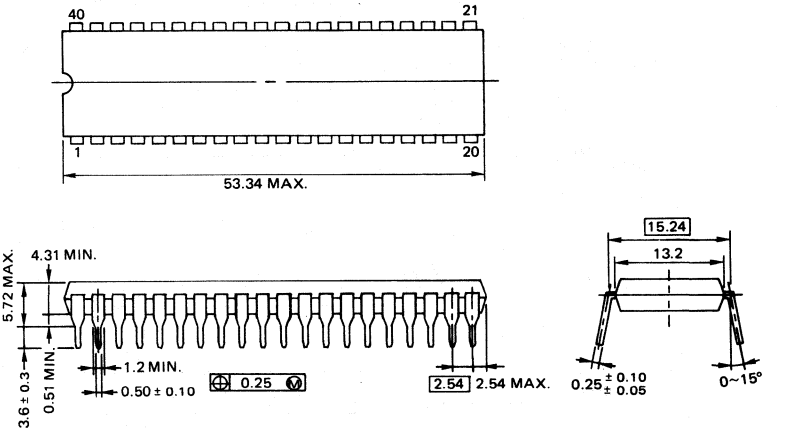
VERIFY



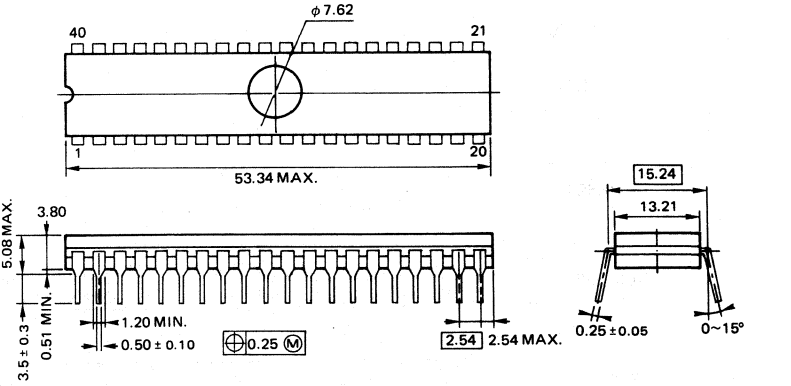
Note:

1. When EA is „low" or T0 = 5V, PROG should be in floating condition (≠ 18V).
2. t_{CY} 4 μs can be achieved using 3.7 MHz frequency at the XTAL1 and XTAL2.

40-PIN PLASTIC DIP PACKAGE
OUTLINE (UNIT : mm)
μPD8748HC



40-PIN CERAMIC DIP PACKAGE
OUTLINE (UNIT : mm)
μPD8748HD



HIGH-SPEED, 8-BIT, SINGLE-CHIP HMOS MICROCOMPUTERS

DESCRIPTION

The NEC μPD8039HL, μPD8049H and the μPD8749H are high performance, single component, 8-bit parallel microcomputers using n-channel silicon gate MOS technology. The processors differ only in their internal program memory options: the μPD8049H has 2K x 8 bytes of mask ROM, the μPD8749H has 2K x 8 of UV erasable EPROM and the μPD8039HL has external program memory.

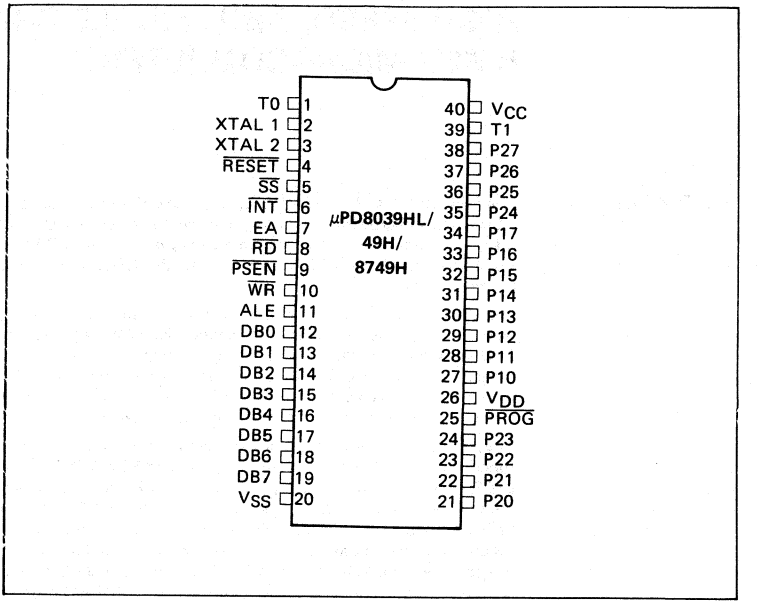
The μPD8049H family functions efficiently in control as well as arithmetic applications. The powerful instruction set eases bit handling applications and provides facilities for binary and BCD arithmetic. Standard logic functions implementation is facilitated by the large variety of branch and table look-up instructions. The instruction set is comprised of 1 and 2 byte instructions, most of which are single-byte. The instruction set requires only 1 or 2 cycles per instruction with over 50 percent of the instructions single-cycle.

The μPD8049H family of microprocessors will function as stand-alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories. The μPD8039HL is intended for applications using external program memory only. It contains all the features of the μPD8049H except for the internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products. The μPD8049H contains the following functions usually found in external peripheral devices: 2048 x 8 bits of mask ROM program memory; 128 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; and oscillator and clock circuitry. The μPD8749H differs from the μPD8049H in its 2048 x 8-bit UV erasable EPROM program memory instead of the mask ROM memory. It is useful in preproduction or prototype applications where the software design has not yet been finalized or in system designs whose quantities do not require a mask ROM.

FEATURES

- High performance 11 MHz operation
- Fully compatible with industry standard 8039/8049/8749
- Pin compatible with the μPD8048/8748
- 1.36 μs cycle time. All instructions 1 or 2 bytes
- Programmable interval timer/event counter
- 2K x 8 bytes of ROM/EPROM, 128 x 8 bytes of RAM
- External and internal interrupts
- 96 instructions: 70 percent single byte
- 27 I/O lines
- Internal clock generator
- Expandable with 8080A/8085A peripherals
- HMOS silicon gate technology
- Single +5V power supply (8039HL/49H)

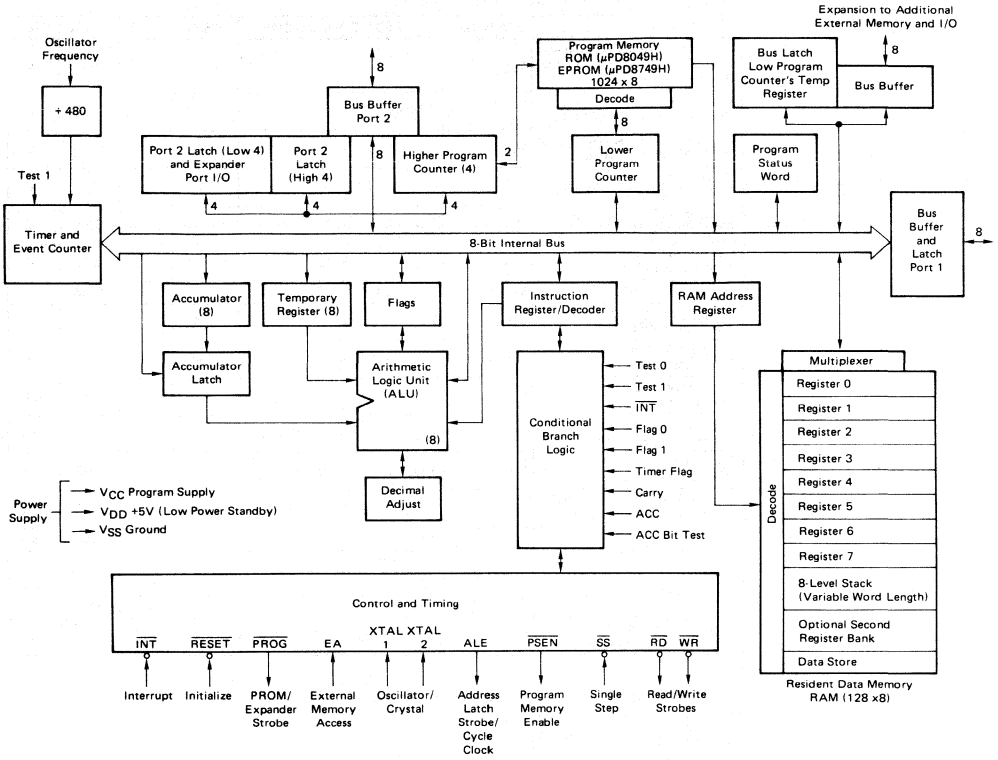
PIN CONFIGURATION



PIN IDENTIFICATION

NO.	SYMBOL	FUNCTION
1	T0	Test 0 input/output
2	XTAL1	Crystal 1 input
3	XTAL2	Crystal 2 input
4	$\overline{\text{RESET}}$	Reset input
5	$\overline{\text{SS}}$	Single step input
6	$\overline{\text{INT}}$	Interrupt input
7	EA	External access input
8	$\overline{\text{RD}}$	Read output
9	$\overline{\text{PSEN}}$	Program store enable output
10	$\overline{\text{WR}}$	Write output
11	ALE	Address latch enable output
12–19	DB_0–DB_7	Bidirectional data bus
20	V_{SS}	Ground
21–24, 35–38	$P2_0$–$P2_7$	Quasi-bidirectional Port 2
25	PROG	Program output
26	V_{DD}	RAM power supply
27–34	$P1_0$–$P1_7$	Quasi-bidirectional Port 1
39	T1	Test 1 input
40	V_{CC}	Primary power supply

BLOCK DIAGRAM



Note: μPD8039HL does not include ROM.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C

Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Voltage on any pin, $V_{I/O}$	−0.5V to +7.0V (Note 1)
Power dissipation, P_D	1.5W

Note:

(1) With respect to ground.

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input low voltage (All except XTAL1, XTAL2, $\overline{RESET}$ for 8749H)	V_{IL}		−0.5		0.8	V
Input low voltage (XTAL1, XTAL2, $\overline{RESET}$)	V_{IL1}	8749H	−0.5		0.6	V
Input high voltage (All except XTAL1, XTAL2, $\overline{RESET}$	V_{IH}		2.0		V_{CC}	V
Input high voltage (XTAL1, XTAL2, $\overline{RESET}$)	V_{IH1}		3.8		V_{CC}	V
Output low voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL}	I_{OL} = 2.0 mA, *1			0.45	V
Output low voltage (All others except PROG)	V_{OL1}	I_{OL} = 2.0 mA, *2			0.45	V
Output low voltage (PROG)	V_{OL2}	I_{OL} = 2.0 mA, *3			0.45	V
Output high voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH}	I_{OH} = −400 μA, *4	2.4			V
Output high voltage (all other outputs)	V_{OH1}	I_{OH} = −40 μA	2.4			V
Input leakage current (T1, INT)	I_{LI}	$V_{SS} \leq V_{IN} \leq V_{CC}$			± 10	μA
Input leakage current ($P1_0$–$P1_7$, $P2_0$–$P2_7$, EA, $\overline{SS}$)	I_{LI1}	V_{SS} +0.45V ≤ $V_{IN} \leq V_{CC}$			−500	μA
Input leakage current ($\overline{RESET}$)	I_{LI2}	V_{SS} +0.45V ≤ $V_{IN} \leq V_{CC}$	−10		−50	μA
Output leakage current (BUS T0, high impedance state)	I_{LO}	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V			± 10	μA
Power down supply current	I_{DD}	T_A = 25°C		5	10	mA
		8749H only		2	5	
Total supply current	$I_{DD} = I_{CC}$	T_A = 25°C		80	110	mA
		8749H only		85	110	
Minimum voltage to maintain RAM contents	V_{DD}	Mins voltage $\overline{RESET}$ ≤ 0.6V	2.2		5.5	V

Note:

*1 = for 8749H: I_{OL} = 1.8 mA for $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE;

*2 = for 8749H: I_{OL} = 1.6 mA;

*3 = for 8749H: I_{OL} = 1.0 mA;

*4 = for 8749H: I_{OH} = −100 μA for $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE;

DC PROGRAMMING CHARACTERISTICS

T_A = 25°C ± 5°C, V_{CC} = +5V ± 5 %, V_{DD} = +21V ± 0.5V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD} program voltage high level	V_{DDH}		20.5		21.5	V
V_{DD} program voltage low level	V_{DDL}		4.75		5.25	V
PROG program voltage high level	V_{PH}		17.5		18.5	V
PROG voltage low level	V_{PL}		4.0		V_{CC}	V
EA program/verify voltage high level	V_{EAH}		17.5		18.5	V
V_{DD} high voltage supply current	I_{DD}				20.0	mA
PROG high voltage supply current	I_{PROG}				1.0	mA
EA high voltage supply current	I_{EA}				1.0	mA

AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cycle time	t_{CY}		1.36		15	μs
ALE pulse width	t_{LL}		150			ns
Address setup to ALE	t_{AL}		70			ns
Address hold from ALE	t_{LA}		50			ns
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}		480			ns
Control pulse width ($\overline{PSEN}$)	t_{CC2}		350			ns
Data setup before $\overline{WR}$	t_{DW}		390			ns
Data hold after $\overline{WR}$	t_{WD}	(Note 2)	40			ns
Data hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}		0		110	ns
$\overline{RD}$ to data in	t_{RD1}				*350/330	ns
$\overline{PSEN}$ to data in	t_{RD2}				*210/190	ns
Address setup to $\overline{WR}$	t_{AW}		300			ns
Address setup to data ($\overline{RD}$)	t_{AD1}				*750/730	ns
Address setup to data ($\overline{PSEN}$)	t_{AD2}				*480/460	ns
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}		140			ns
Address float to $\overline{PSEN}$	t_{AFC2}		10			ns
ALE to control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}		200			ns
ALE to control ($\overline{PSEN}$)	t_{LAFC2}		60			ns
Control to ALE ($\overline{RD}$, $\overline{WR}$, PROG)	t_{CA1}		50			ns
Control to ALE ($\overline{PSEN}$)	t_{CA2}		320			ns
Port control setup to $\overline{PROG}$	t_{CP}		100			ns
Port control hold to $\overline{PROG}$	t_{PC}		160			ns
$\overline{PROG}$ to P2 input valid	t_{PR}				650	ns
Input data hold from $\overline{PROG}$	t_{PF}		0		140	ns
Output data setup	t_{DP}		400			ns
Output data hold	t_{PD}		90			ns
$\overline{PROG}$ pulse width	t_{PP}		700			ns
Port 2 I/O data setup to ALE	t_{PL}		160			ns
Port 2 I/O data hold to ALE	t_{LP}		40			ns
Port output from ALE	t_{PV}				510	ns
I/O rep rate	t_{OPRR}		270			ns

Note:

(1) Control outputs: C_L = 80 pF, bus outputs: C_L = 150 pF

(2) Bus high impedance, load = 20 pF

(3) Double values are for 8039HL, 8049H/8749H respectively

4

AC PROGRAMMING CHARACTERISTICS

T_A = 25°C ± 5°C, V_{CC} = +5V ± 5 %, V_{DD} = +21V ± 0.5V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Address setup time to $\overline{RESET}$ ↑	t_{AW}		4 t_{CY}			
Address hold time after $\overline{RESET}$ ↑	t_{WA}		4 t_{CY}			
Data in setup time to PROG ↑	t_{DW}		4 t_{CY}			
Data in hold time after PROG ↓	t_{WD}		4 t_{CY}			
$\overline{RESET}$ hold time to verify	t_{PH}		4 t_{CY}			
V_{DD}	t_{VDDW}		0		1.0	ms
V_{DD} hold time after PROG ↓	t_{VDDH}		0		1.0	ms
PROG pulse width	t_{PW}		50		60	ms
TEST0 setup time for program mode	t_{TW}		4 t_{CY}			
TEST0 hold time after program mode	t_{WT}		4 t_{CY}			
TEST0 to data out delay (1)	t_{D0}				4 t_{CY}	
$\overline{RESET}$ pulse width to latch address	t_{WW}		4 t_{CY}			
V_{DD} and PROG rise and fall times	t_r, t_f		0.5		100	μs
CPU operation cycle time	t_{CY}	4.0 μs / 3.7 Mhz	4.0		15	μs
RESET setup time before EA ↑	t_{RE}		4 t_{CY}			

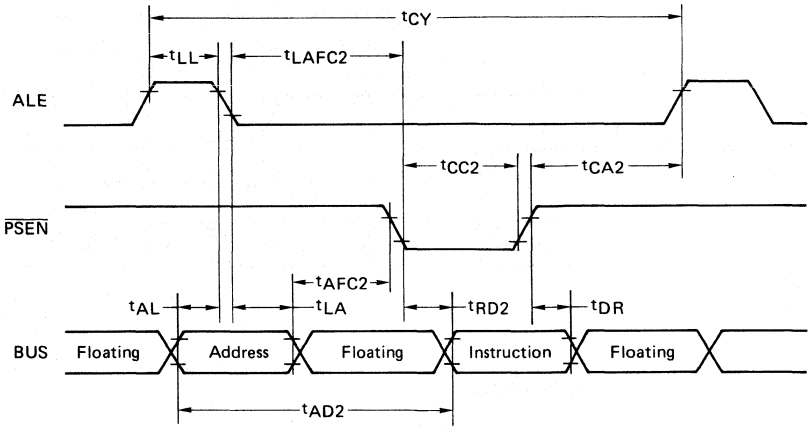
BUS TIMING REQUIREMENTS

SYMBOL	TIMING FORMULA	MIN/MAX	UNIT
t_{LL}	(7/30) t_{CY} −170	MIN	ns
t_{AL}	(2/15) t_{CY} −110	MIN	ns
t_{LA}	(1/15) t_{CY} − 40	MIN	ns
t_{CC1}	(1/ 2) t_{CY} −200	MIN	ns
t_{CC2}	(2/ 5) t_{CY} −200	MIN	ns
t_{DW}	(13/30) t_{CY} −200	MIN	ns
t_{WD}	(1/15) t_{CY} − 50	MIN	ns
t_{DR}	(1/10) t_{CY} − 30	MAX	ns
t_{RD1}	(2/ 5) t_{CY} −200 / (11/30) t_{CY} −170	MAX	ns
t_{RD2}	(3/10) t_{CY} −200 / (4/15) t_{CY} −170	MAX	ns
t_{AW}	(1/ 3) t_{CY} −150	MIN	ns
t_{AD1}	(11/15) t_{CY} −250 / (7/10) t_{CY} −220	MAX	ns
t_{AD2}	(8/15) t_{CY} −250 / (1/ 2) t_{CY} −220	MAX	ns
t_{AFC1}	(2/15) t_{CY} − 40	MIN	ns
t_{AFC2}	(1/30) t_{CY} − 40	MIN	ns
t_{LAFC1}	(1/ 5) t_{CY} − 75	MIN	ns
t_{LAFC2}	(1/10) t_{CY} − 75	MIN	ns
t_{CA1}	(1/15) t_{CY} − 40	MIN	ns
t_{CA2}	(4/15) t_{CY} − 40	MIN	ns
t_{CP}	(1/10) t_{CY} − 40 / (2/15) t_{CY} − 80	MIN	ns
t_{PC}	(4/15) t_{CY} −200	MIN	ns
t_{PR}	(17/30) t_{CY} −120	MAX	ns
t_{PF}	(1/10) t_{CY}	MAX	ns
t_{DP}	(2/ 5) t_{CY} −150	MIN	ns
t_{PD}	(1/10) t_{CY} − 50	MIN	ns
t_{PP}	(7/10) t_{CY} −250	MIN	ns
t_{PL}	(4/15) t_{CY} −200	MIN	ns
t_{LP}	(1/10) t_{CY} −100 / (1/30) t_{CY} − 30	MIN	ns
t_{PV}	(3/10) t_{CY} −100	MAX	ns
t_{OPRR}	(3/15) t_{CY}	MIN	ns
t_{CY}	11 MHz		μs

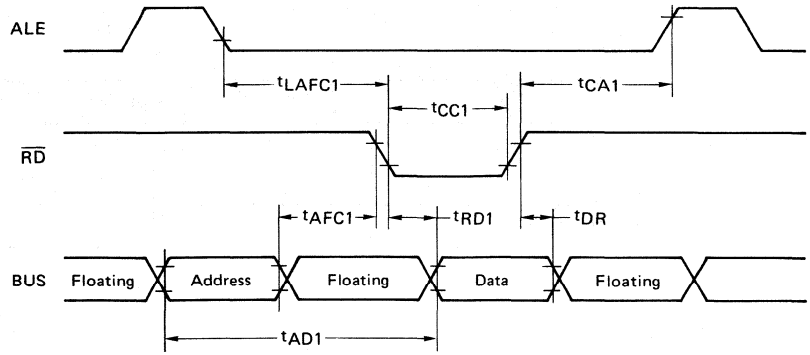
Note: Double values reflect: 8039HL, 49H/8749H

TIMING WAVEFORMS

INSTRUCTION FETCH FROM EXTERNAL MEMORY

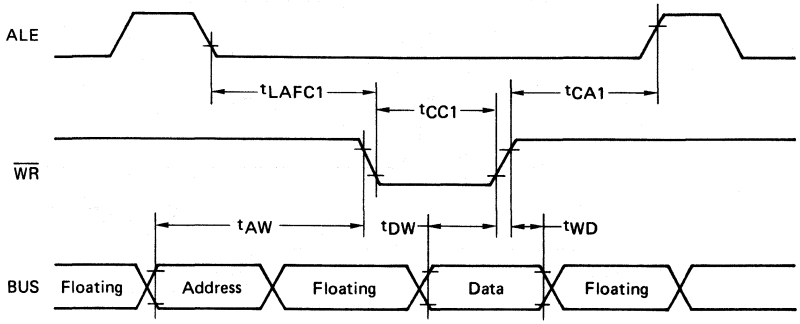


READ FROM EXTERNAL DATA MEMORY

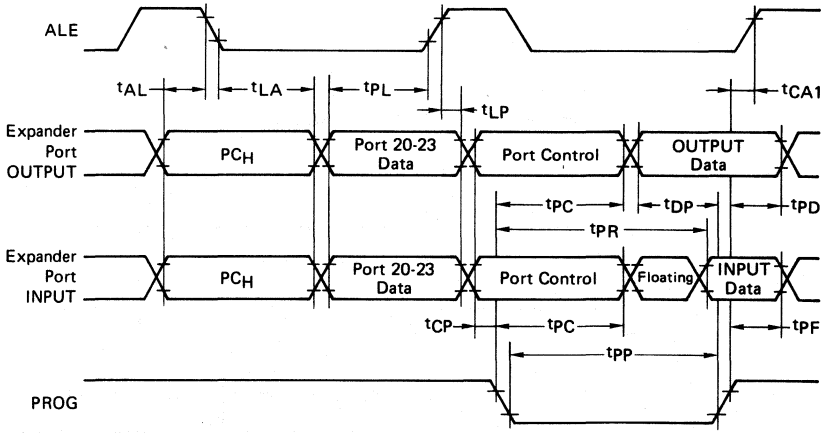


4

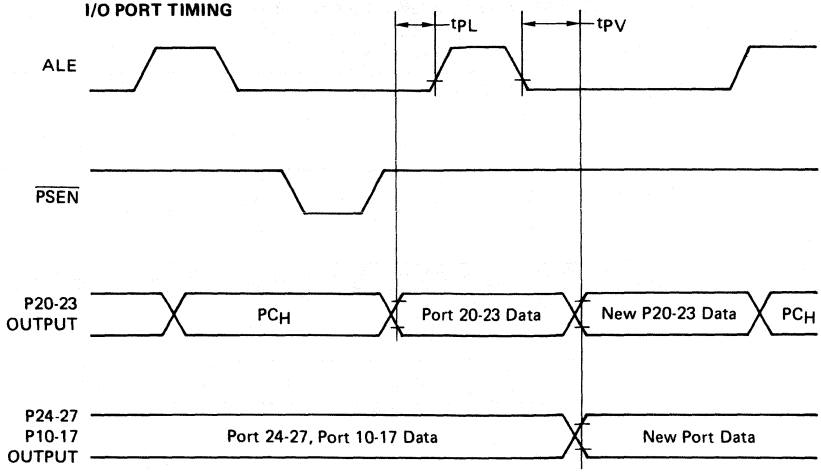
WRITE TO EXTERNAL MEMORY



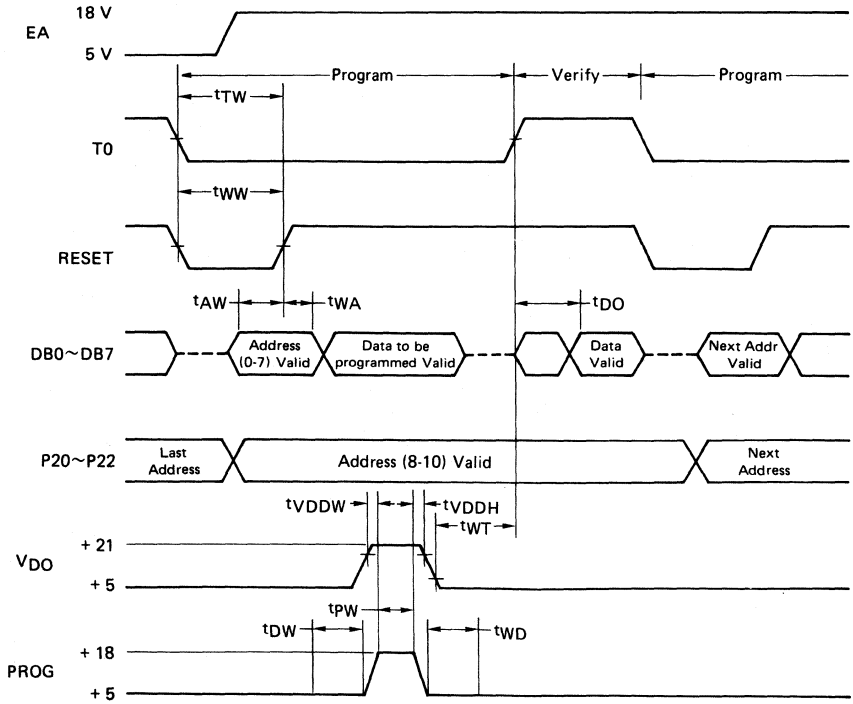
PORT 2 TIMING



I/O PORT TIMING

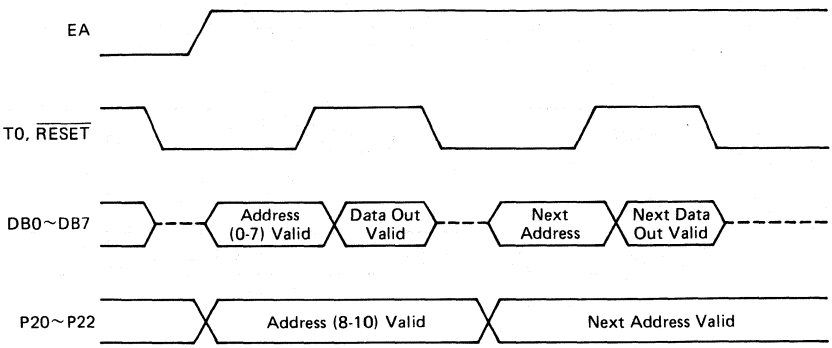


WAVEFORMS FOR PROGRAMMING THE μPD8749H

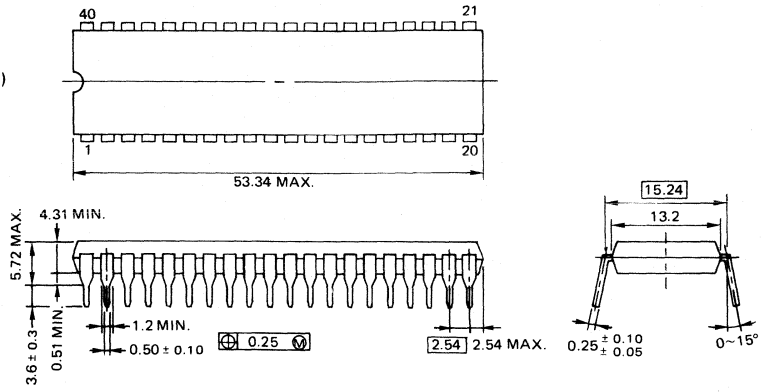


4

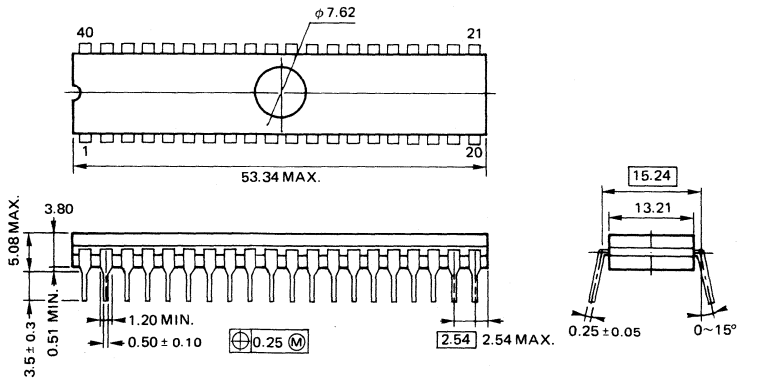
PROGRAM/VERIFY TIMING (ROM/EPROM)



40-PIN PLASTIC
DIP PACKAGE
OUTLINE (Unit : mm)
μPD8039HLC
μPD8049HC–XXX
μPD8749HC



40-PIN CERAMIC
DIP PACKAGE
OUTLINE (Unit : mm)
μPD8749HD



4

GENERAL INFORMATION

NMOS MICROCOMPUTER SELECTION GUIDE

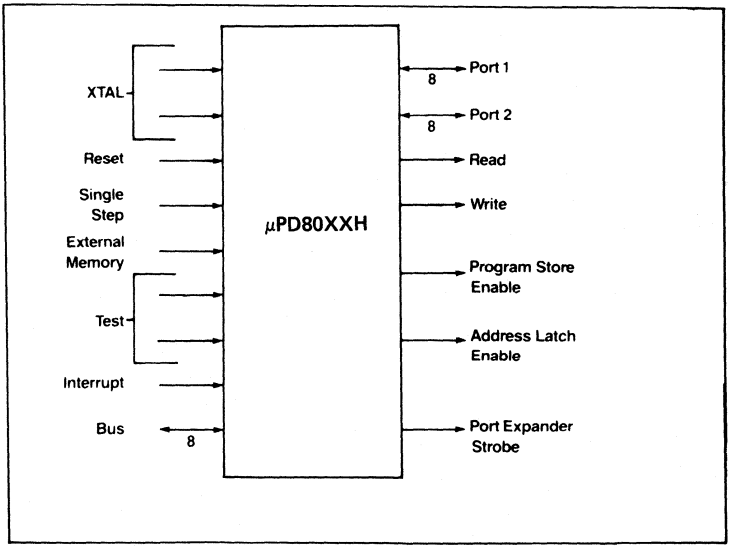
SINGLE CHIP 8-BIT MICROCOMPUTERS

DEVICE	SPECIAL FEATURES	ROM	RAM	I/O	PROCESS	CYCLE	SUPPLY VOLTAGE	PINS
8049H(A)	Temp Range −40°C to +85°C	2048x8	128x8	27	NMOS	1·360 μs	5V±10 %	40
8049H(S)	Temp Range −40°C to +110°C	2048x8	128x8	27	NMOS	1·875 μs	5V±10 %	40
8048H(A)	Temp Range −40°C to +85°C	1024x8	64x8	27	NMOS	2·50 μs	5V±10 %	40
8048H(S)	Temp Range −40°C to +110°C	1024x8	64x8	27	NMOS	3·75 μs	5V±10 %	40

SPECIAL A AND S GRADE

	NORMAL	(A) GRADE	(S) GRADE
1st electrical test	at room temp	at 85 deg c	at 110 deg c
Burn-in	4 hours	16 hours	16 hours
2nd electrical test	at room temp	at room temp	at room temp

LOGIC SYMBOL



4

INSTRUCTION SET

SYMBOL DEFINITIONS

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0–7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number of Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator
P_p	Port Designator (p–1, 2 or 4–7)
PSW	Program Status Word
Rr	Register Designator (r–0, 1 or 0–7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
S	Program Counters Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location
←	Replaced By

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Accumulator																
ADD A, # data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
Add A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 – 1	Add Indirect the contents of the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, # data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 – 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 – 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, # dø	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_n	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 – 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 – 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) 1	DECREMENT by 1 the Accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator.	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 – 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 – 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 – 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_{4-7}) ← (A_0 – 3)	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
Branch																
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 if (Rr) ≠ 0: (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC 0 – 7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC 0 – 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 – 7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Branch (Cont.)																
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
Control																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 - 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 - 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 - 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 - 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
Data Moves																
MOV A, # data	(A) ← data	Move immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, # data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, # data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0 – 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ⇄ ((Rr)(0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
Flags																
CPL C	(C) ← NOT (C)	Complement content of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement content of Flag F1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Input/Output																
ANL BUS, # data	(BUS) ← (BUS) AND data	Logical and Immediate-specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1 – 2	Logical and Immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 – 3) p = 4 – 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1 – 2	Input data from designated port (1 – 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 – 7 (A 4 – 7) ← 0	Move contents of designated port (4 – 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0 – 3; p = 4 – 7	Move contents of Accumulator to designated port (4 – 7).	0	0	1	1	1	1	p	p	1	1				
ORL BUS, # data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 – 3) p = 4 – 7	Logical or contents of Accumulator with designated port (4 – 7).	1	0	0	0	1	1	p	p	1	1				
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1 – 2	Logical or Immediate specified data with designated port (1 – 2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A [5]	(BUS) ← (A)	Output contents of Accumulator onto BUS.	0	0	0	0	0	0	1	0	1	1				
OUTL Pp, A	(Pp) ← (A); p = 1 – 2	Output contents of Accumulator to designated port (1 – 2).	0	0	1	1	1	0	p	p	1	1				
Registers																
DEC Rr, (Rr)	(Rr) ← (Rr) – 1; r = 0 – 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) + 1; r = 0 – 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 – 1	Increment indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
Subroutine																
CALL addr	((SP)) ← (PC), (PSW 4 – 7) (SP) ← (SP) + 1 (PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW 4 – 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
Timer/Counter																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1				
Miscellaneous																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

Notes:
1. Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
2. The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
3. References to the address and data are specified in bytes 2 and or 1 of the instruction.
4. Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.
5. When the Bus is written to, with an OUTL instruction, the Bus remains an Output Port until either device is reset or a MOVX instruction is executed.

SINGLE CHIP 8-BIT MICROCOMPUTERS

DESCRIPTION

The NEC μPD8048, μPD8748 and μPD8035L are single component, 8-bit, parallel microprocessors using N-channel silicon gate MOS technology. The μPD8048/8748/8035 efficiently function in control as well as arithmetic applications. The flexibility of the instruction set allows for the direct set and reset of individual data bits within the accumulator and the I/O port structure. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

The μPD8048/8748/8035L instruction set is comprised of 1 and 2 byte instructions with over 70 % single-byte and requiring only 1 or 2 cycles per instruction with over 50 % single-cycle.

The μPD8048 series of microprocessors will function as stand alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8048 contains the following functions usually found in external peripheral devices: 1024 x 8 bits of ROM program memory; 64 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

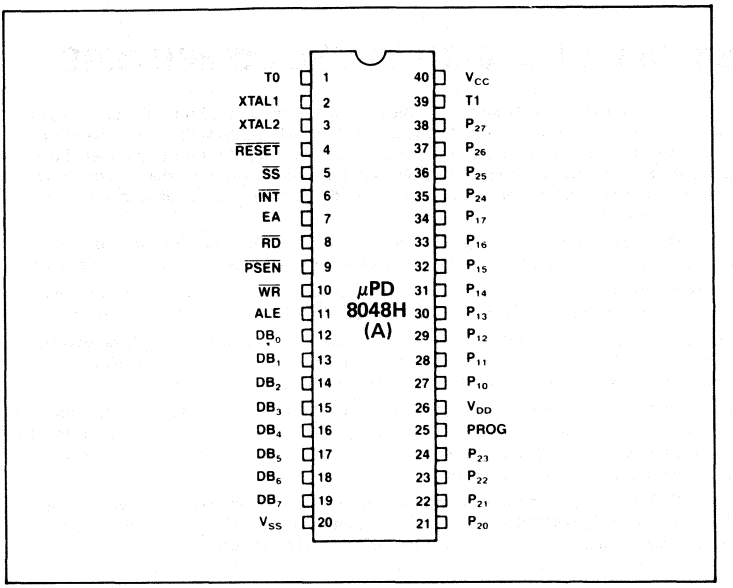
The μPD8748 differs from the μPD8048 only in its 1024 x 8-bit UV erasable EPROM program memory instead of the 1024 x 8-bit ROM memory. It is useful in preproduction or prototype applications where the software design has not yet been finalized or in system designs whose quantities do not require a mask ROM.

The μPD8035L is intended for applications using external program memory only. It contains all the features of the μPD8048 except the 1024 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

FEATURES

- Fully Compatible With Industry Standard 8048
- NMOS Silicon Gate Technology Requiring a Single +5V Supply
- 2.5 μs Cycle Time. All Instruction 1 or 2 Bytes
- Interval Timer/Event Counter
- 64 x 8 bit Ram Data Memory
- Single Level Interrupt
- 96 Instructions: 70 % Single Byte
- 27 I/O Lines
- Internal Clock Generator
- 8 Level Stack
- Compatible With 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40 Pin Packages
- Temp Range −40°C to +85°C

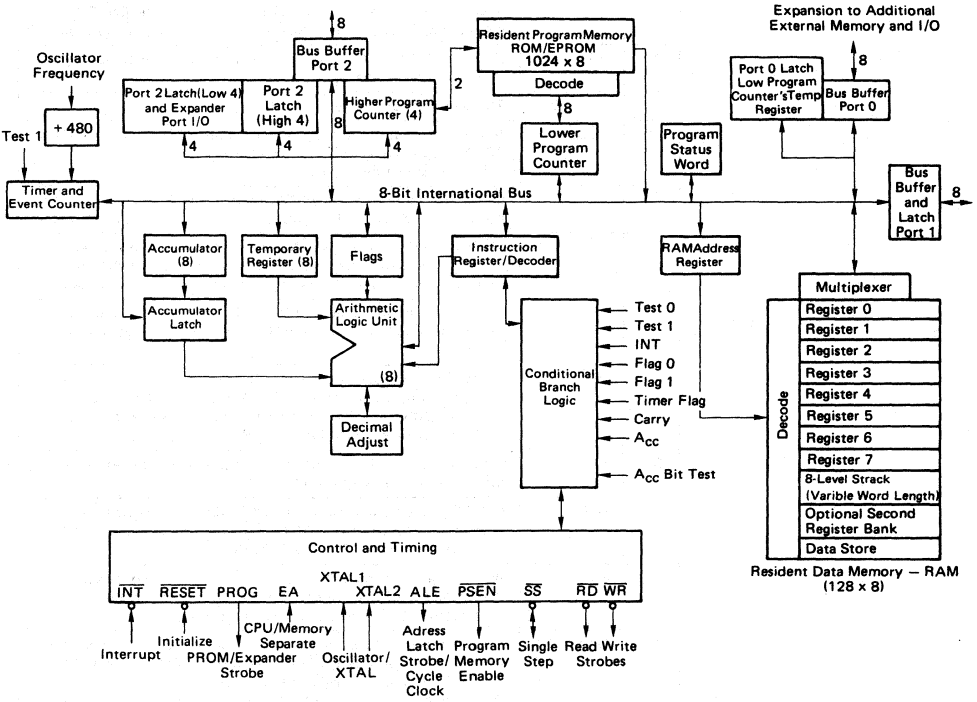
PIN CONFIGURATION



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non-TTL compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{RESET}$	Active low input for processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non-TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe output (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active-high). Occuring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12-19	D_0-D_7 BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the D_0-D_7 BUS can be latched in a static mode. During an external memory fetch, the D_0-D_7 BUS holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the D_0-D_7 BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21-24, 35-38	P_{20}-P_{27}: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in P_{20}-P_{23}. Bits P_{20}-P_{23} are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	Program Pulse. A +25V pulse applied to this input is used for programming the μPD8748. PROG is also used as an output strobe for the μPD8243.
26	V_{DD}	Programming Power Supply. V_{DD} must be set to +25V for programming the μPD8748, and to +5V for the ROM and PROM versions for normal operation. V_{DD} functions as the Low Power Standby input for the μPD8048.
27-34	P_{10}-P_{17}: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power supply. V_{CC} is +5V for programming and operation of the μPD8748, and for operation of the μPD8035L and μPD8048.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature	−40°C to +85°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +150°C
Voltage on Any Pin	−0.5V to +7V ①
Power Dissipation	1.5 W

Note: ① With respect to ground.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated unter conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = -40°C$ to $+85°C$; $V_{CC} = V_{DD} = +5V \pm 10\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}		0		0.7	V
Input Low Voltage ($\overline{RESET}$, X1, X2)	V_{IL1}		0		0.7	V
Input High Voltage (All Except XTAL 1, XTAL 2, RESET)	V_{IH}		2.3		V_{CC}	V
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}		3.8		V_{CC}	V
Output Low Voltage (BUS)	V_{OL}	$I_{OL} = 2.0$ mA			0.45	V
Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}	$I_{OL} = 2.0$ mA			0.45	V
Output Low Voltage (PROG)	V_{OL2}	$I_{OL} = 2.0$ mA			0.45	V
Output High Voltage (BUS)	V_{OH}	$I_{OH} = -100\ \mu A$	2.4			V
Output High Voltage (RD, WR, PSEN, ALE)	V_{OH1}	$I_{OH} = -100\ \mu A$	2.4			V
Output High Voltage (All Other Outputs)	V_{OH2}	$I_{OH} = -30\ \mu A$	2.4			V
Input Leakage Current (T_1, EA, INT)	I_{IL}	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$			± 10	μA
Input Leakage Current (P_{10}–P_{17}, P_{20}–P_{27}, EA, $\overline{SS}$)	I_{IL1}	$V_{CC} \geqslant V_{IN} \geqslant V_{SS} + 0.45V$			-700	μA
Output Leakage Current (BUS, T_0–High Impedance State)	I_{OL}	$V_{CC} \geqslant V_{IN} \geqslant V_{SS} + 0.45V$			± 10	μA
Power Down Supply Current	I_{DD}	$T_a = 25°C$			8	mA
Total Supply Current	$I_{DD}+I_{CC}$	$T_a = 25°C$			100	mA
RAM Standby Voltage	V_{DD}	Standby Mode. Reset $\leqslant 0.6V$	3.0		5.5	V

4

AC CHARACTERISTICS

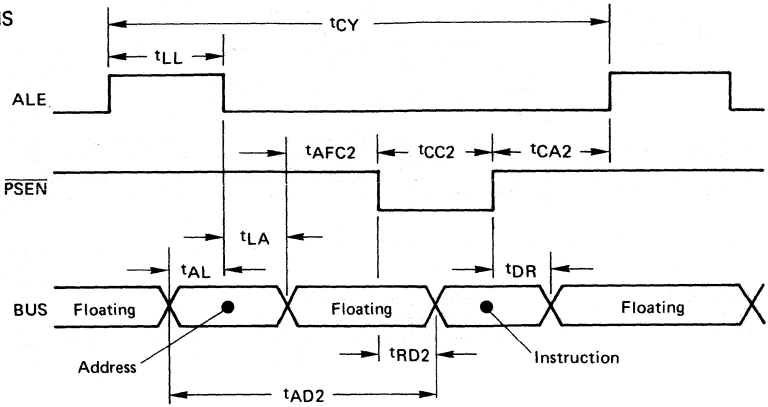
T_a = −40°C to +80°C; V_{CC} = V_{DD} = 5V ± 10 %; V_{SS} = 0V

PARAMETER	SYMBOL	f(t_{CY}) and TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
ALE Pulse Width	t_{LL}	7/30 t_{CY} −170	410			ns
Addr Setup to ALE	t_{AL}	2/15 t_{CY} −110	220			ns
Addr Hold from ALE	t_{LA}	1/15 t_{CY} −40	120			ns
Control Pulse Width (RD, WR)	t_{CC1}	1/2 t_{CY} −200	1050			ns
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}	2/5 t_{CY} −200	800			ns
Data Setup $\overline{WR}$	t_{DW}	13/30 t_{CY} −200	880			ns
Data Hold after $\overline{WR}$	t_{WD}	1/15 t_{CY} −50	110			ns
Data Hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	1/10 t_{CY} −30	0		220	ns
$\overline{RD}$ to Data in	t_{RD1}	2/5 t_{CY} −200			800	ns
$\overline{PSEN}$ to Data in	t_{RD2}	3/10 t_{CY} −200			550	ns
Addr Setup to $\overline{WR}$	t_{AW}	1/3 t_{CY} −150	680			ns
Addr Setup to Data ($\overline{RD}$)	t_{AD1}	11/15 t_{CY} −250			1570	ns
Addr Setup to Data ($\overline{PSEN}$)	t_{AD2}	8/15 t_{CY} −250			1090	ns
Addr Float to $\overline{RD}$, $\overline{WD}$	t_{AFC1}	2/15 t_{CY} −40	290			ns
Addr Float to $\overline{PSEN}$	t_{AFC2}	1/30 t_{CY} −40	40			ns
ALE to Control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	1/15 t_{CY} −75	420			ns
ALE to Control ($\overline{PSEN}$)	t_{LAFC2}	1/10 t_{CY} −75	170			ns
Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t_{CA1}	1/15 t_{CY} −40	120			ns
Control to ALE ($\overline{PSEN}$)	t_{CA2}	4/15 t_{CY} −40	620			ns
Port Control Setup to $\overline{PROG}$	t_{CP}	1/10 t_{CY} −40	210			ns
Port Control Hold to $\overline{PROG}$	t_{PC}	4/15 t_{CY} −200	460			ns
PROG to P2 Input Valid	t_{PR}	17/30 t_{CY} −120			1300	ns
Input Data Hold from $\overline{PROG}$	t_{PF}	1/10 t_{CY}			250	ns
Output Data Setup	t_{DP}	2/5 t_{CY} −150	850			ns
Output Data Hold	t_{PD}	1/10 t_{CY} −50	200			ns
$\overline{PROG}$ Pulse Width	t_{PP}	7/10 t_{CY} −250	1500			ns
Port 2 I/O Setup to ALE	t_{PL}	4/15 t_{CY} −200	460			ns
Port 2 I/O Hold to ALE	t_{LP}	1/10 t_{CY} −100	150			ns
Port Output from ALE	t_{PV}	3/10 t_{CY} +100			850	ns
Cycle Time	t_{CY}	6 MHz (max.)	2.5		15	μs
TO Rep Rate	t_{OPRR}	3/15 t_{CY}	500			ns

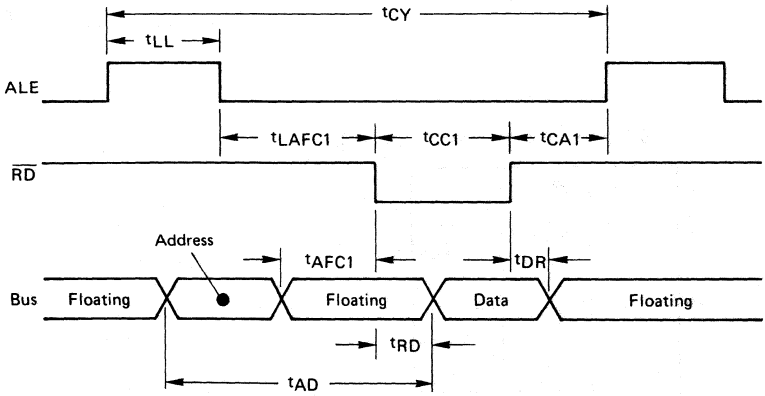
Notes: Control Outputs CL = 80pF
BUS Outputs CL = 150pF
BUS High Impedance Load 20pF

TIMING WAFEFORMS

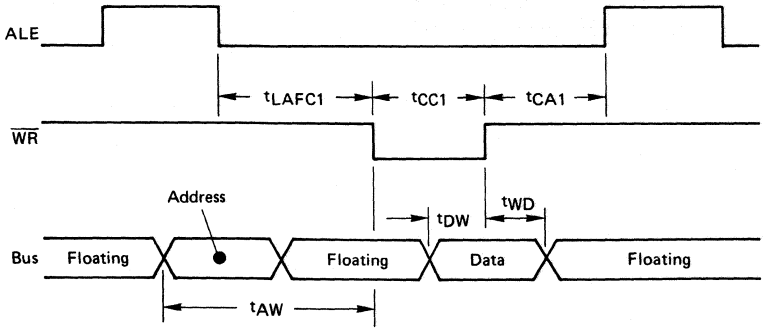
Instruction Fetch from External Memory



Read from External Data Memory

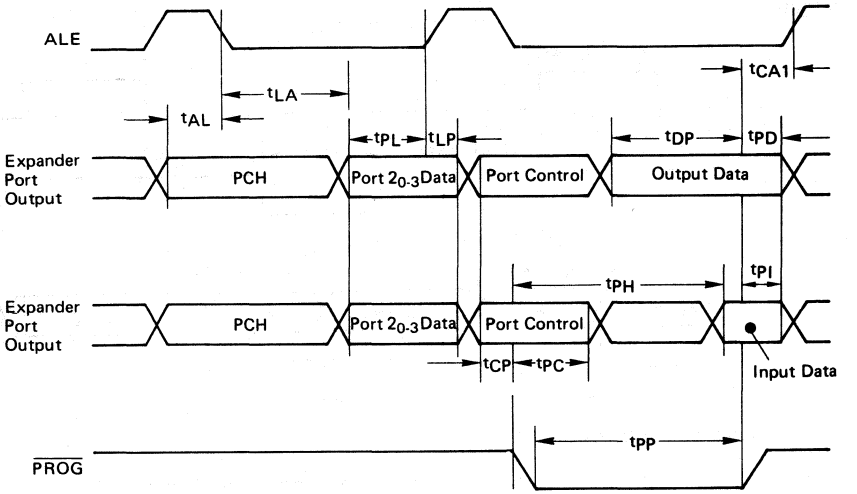


Write to External Memory

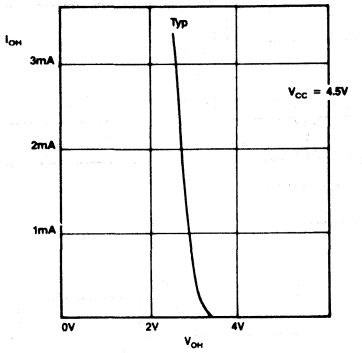


4

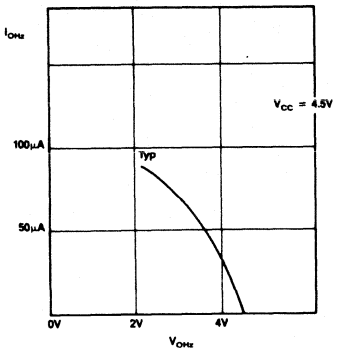
Port 2 Timing



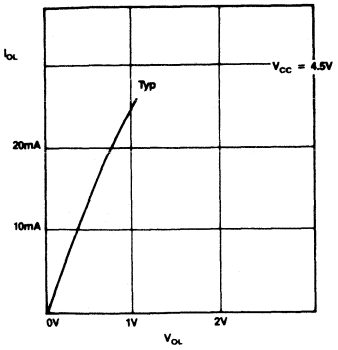
BUS Output High Voltage vs. Source Current



Port P1 and P2 Output
High Voltage vs. Source Current

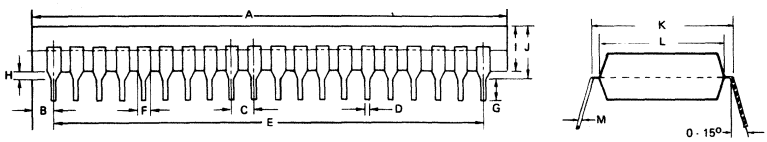


BUS Output Low Voltage vs. Sink Current



40 PIN PLASTIC
μPD8048HC

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.5 MIN	0.06 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



4

SINGLE CHIP 8-BIT MICROCOMPUTERS

DESCRIPTION

The NEC μPD8048, μPD8748 and μPD8035L are single component, 8-bit, parallel microprocessors using N-channel silicon gate MOS technology. The μPD8048/8748/8035 efficiently function in control as well as arithmetic applications. The flexibility of the instruction set allows for the direct set and reset of individual data bits within the accumulator and the I/O port structure. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

The μPD8048/8748/8035L instruction set is comprised of 1 and 2 byte instructions with over 70 % single-byte and requiring only 1 or 2 cycles per instruction with over 50 % single-cycle.

The μPD8048 series of microprocessors will function as stand alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8048 contains the following functions usually found in external peripheral devices: 1024 x 8 bits of ROM program memory; 64 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

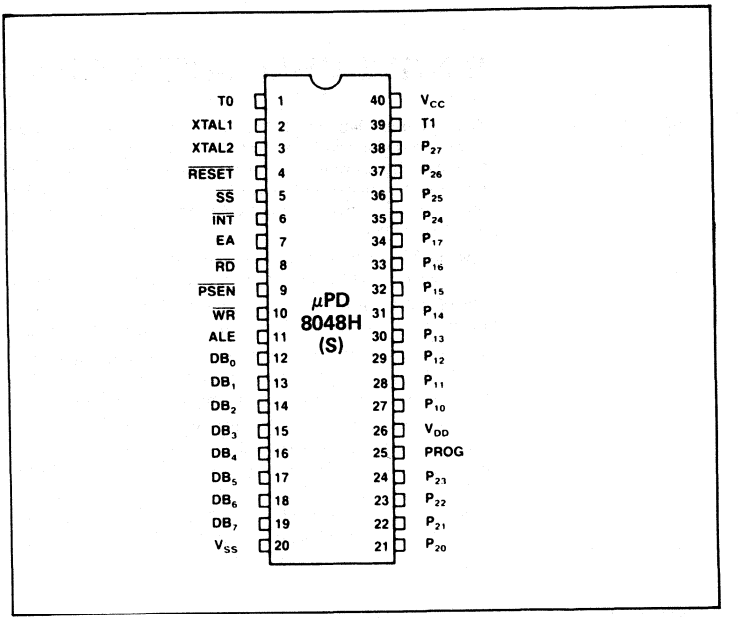
The μPD8748 differs from the μPD8048 only in its 1024 x 8-bit UV erasable EPROM program memory instead of the 1024 x 8-bit ROM memory. It is useful in preproduction or prototype applications where the software design has not yet been finalized or in system designs whose quantities do not require a mask ROM.

The μPD8035L is intended for applications using external program memory only. It contains all the features of the μPD8048 except the 1024 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

FEATURES

- Fully Compatible With Industry Standard 8048
- NMOS Silicon Gate Technology Requiring a Single +5V Supply
- 3.75 μs Cycle Time. All Instruction 1 or 2 Bytes
- Interval Timer/Event Counter
- 64 x 8 bit RAM Data Memory
- Single Level Interrupt
- 96 Instructions: 70 % Single Byte
- 27 I/O Lines
- Internal Clock Generator
- 8 Level Stack
- Compatible With 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40 Pin Packages
- Temp Range −40°C to +110°C

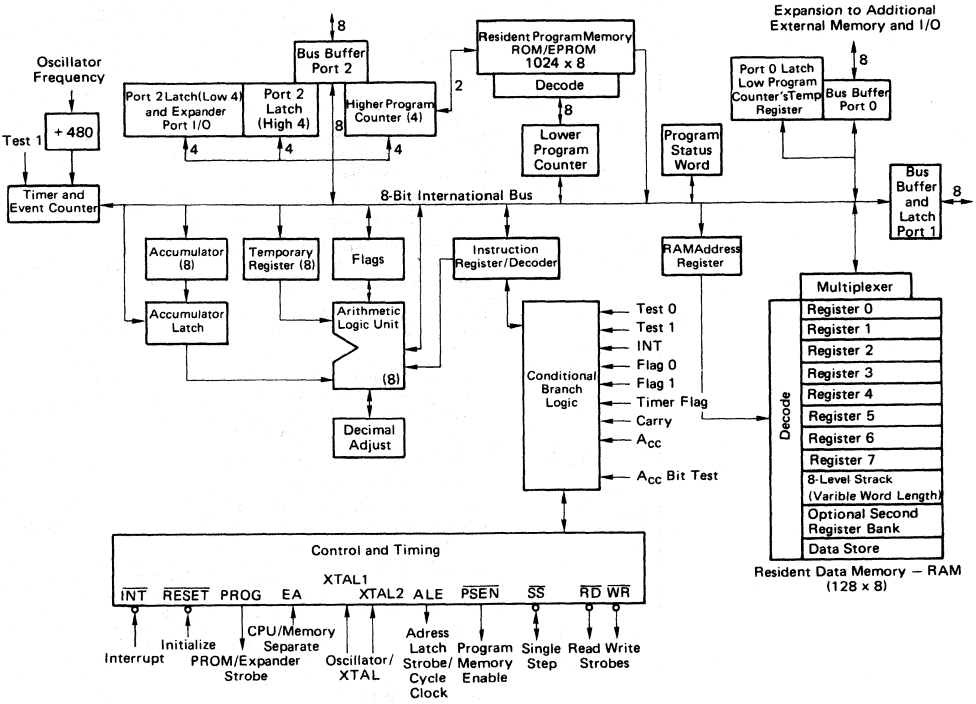
PIN CONFIGURATION



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non-TTL compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{RESET}$	Active low input for processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non-TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe output (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active-high). Occuring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12-19	D_0-D_7 BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the D_0-D_7 BUS can be latched in a static mode. During an external memory fetch, the D_0-D_7 BUS holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the D_0-D_7 BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21-24, 35-38	P_{20}-P_{27}: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in P_{20}-P_{23}. Bits P_{20}-P_{23} are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	Program Pulse. A +25V pulse applied to this input is used for programming the μPD8748. PROG is also used as an output strobe for the μPD8243.
26	V_{DD}	Programming Power Supply. V_{DD} must be set to +25V for programming the μPD8748, and to +5V for the ROM and PROM versions for normal operation. V_{DD} functions as the Low Power Standby input for the μPD8048.
27-34	P_{10}-P_{17}: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power supply. V_{CC} is +5V for programming and operation of the μPD8748, and for operation of the μPD8035L and μPD8048.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature	−40°C to +110°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +150°C
Voltage on Any Pin	−0.5V to +7V①
Power Dissipation	1.5 W

Note: ① With respect to ground.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated unter conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −40°C to +110°C; V_{CC} = V_{DD} = +5V ±10%; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}				0.5	V
Input Low Voltage ($\overline{RESET}$, X1, X2)	V_{IL1}				0.5	V
Input High Voltage (All Except XTAL 1, XTAL 2, RESET)	V_{IH}		2.3			V
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}		3.8			V
Output Low Voltage (BUS)	V_{OL}	I_{OL} = 1.6 mA			0.45	V
Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}	I_{OL} = 1.6 mA			0.45	V
Output Low Voltage (PROG)	V_{OL2}	I_{OL} = 1.6 mA			0.45	V
Output Low Voltage (All Other Outputs)	V_{OL3}	I_{OL} = 1.6 mA			0.45	V
Output High Voltage (BUS)	V_{OH}	I_{OH} = −50 μA	2.4			V
Output High Voltage (RD, WR, PSEN, ALE)	V_{OH1}	I_{OH} = −50 μA	2.4			V
Output High Voltage (All Other Outputs)	V_{OH2}	I_{OH} = −15 μA	2.4			V
Input Leakage Current (T_1, INT)	I_{IL}	$V_{SS} \leq V_{IN} \leq V_{CC}$			±10	μA
Input Leakage Current (P_{10}–P_{17}, P_{20}–P_{27}, EA, $\overline{SS}$)	I_{IL1}	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V			−700	μA
Output Leakage Current (BUS, T_0–High Impedance State)	I_{OL}	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V			±10	μA
Power Down Supply Current	I_{DD}	T_a = 25°C			8	mA
Total Supply Current	$I_{DD}+I_{CC}$	T_a = 25°C			100	mA
RAM Standby Voltage	V_{DD}	Standby Mode. Reset ≤0.5V	4.5		5.5	V

4

AC CHARACTERISTICS

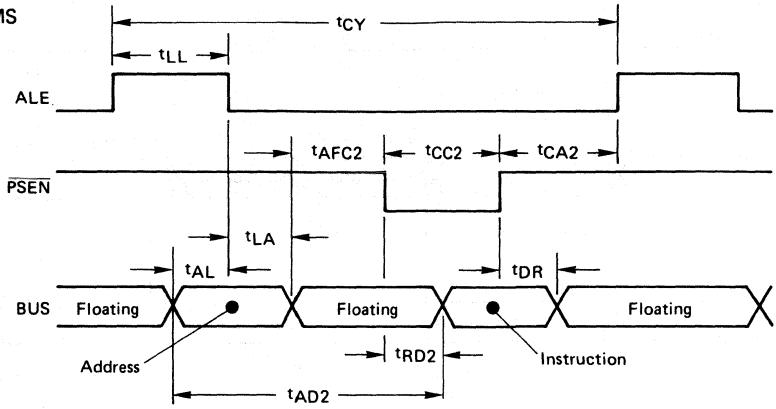
T_a = −40°C to +110°C; V_{CC} = V_{DD} = 5V ± 10 %; V_{SS} = 0V

PARAMETER	SYMBOL	f(t_{CY}) and TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
ALE Pulse Width	t_{LL}	7/30 t_{CY} −170	410			ns
Addr Setup to ALE	t_{AL}	2/15 t_{CY} −110	220			ns
Addr Hold from ALE	t_{LA}	1/15 t_{CY} −40	120			ns
Control Pulse Width (RD, WR)	t_{CC1}	1/2 t_{CY} −200	1050			ns
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}	2/5 t_{CY} −200	800			ns
Data Setup $\overline{WR}$	t_{DW}	13/30 t_{CY} −200	880			ns
Data Hold after $\overline{WR}$	t_{WD}	1/15 t_{CY} −50	110			ns
Data Hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	1/10 t_{CY} −30	0		220	ns
$\overline{RD}$ to Data in	t_{RD1}	2/5 t_{CY} −200			800	ns
$\overline{PSEN}$ to Data in	t_{RD2}	3/10 t_{CY} −200			550	ns
Addr Setup to $\overline{WR}$	t_{AW}	1/3 t_{CY} −150	680			ns
Addr Setup to Data ($\overline{RD}$)	t_{AD1}	11/15 t_{CY} −250			1570	ns
Addr Setup to Data ($\overline{PSEN}$)	t_{AD2}	8/15 t_{CY} −250			1090	ns
Addr Float to $\overline{RD}$, $\overline{WD}$	t_{AFC1}	2/15 t_{CY} −40	290			ns
Addr Float to $\overline{PSEN}$	t_{AFC2}	1/30 t_{CY} −40	40			ns
ALE to Control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	1/15 t_{CY} −75	420			ns
ALE to Control ($\overline{PSEN}$)	t_{LAFC2}	1/10 t_{CY} −75	170			ns
Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t_{CA1}	1/15 t_{CY} −40	120			ns
Control to ALE ($\overline{PSEN}$)	t_{CA2}	4/15 t_{CY} −40	620			ns
Port Control Setup to $\overline{PROG}$	t_{CP}	1/10 t_{CY} −40	210			ns
Port Control Hold to $\overline{PROG}$	t_{PC}	4/15 t_{CY} −200	460			ns
PROG to P2 Input Valid	t_{PR}	17/30 t_{CY} −120			1300	ns
Input Data Hold from $\overline{PROG}$	t_{PF}	1/10 t_{CY}			250	ns
Output Data Setup	t_{DP}	2/5 t_{CY} −150	850			ns
Output Data Hold	t_{PD}	1/10 t_{CY} −50	200			ns
$\overline{PROG}$ Pulse Width	t_{PP}	7/10 t_{CY} −250	1500			ns
Port 2 I/O Setup to ALE	t_{PL}	4/15 t_{CY} −200	460			ns
Port 2 I/O Hold to ALE	t_{LP}	1/10 t_{CY} −100	150			ns
Port Output from ALE	t_{PV}	3/10 t_{CY} +100			850	ns
Cycle Time	t_{CY}	4 MHz (max.)	3.75		15	μs
TO Rep Rate	t_{OPRR}	3/15 t_{CY}	500			ns

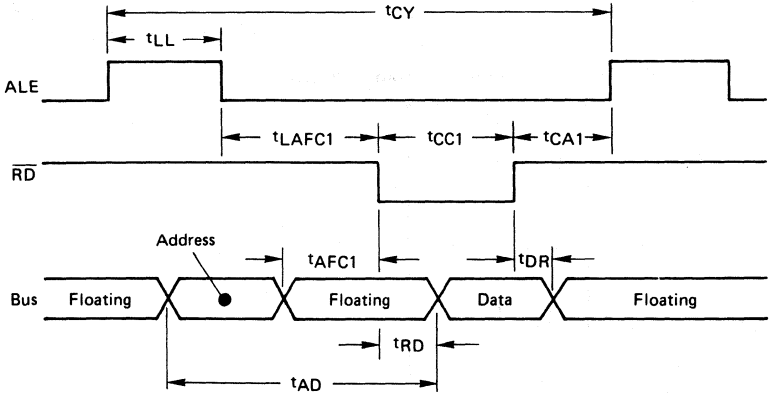
Notes: Control Outputs CL = 80pF
BUS Outputs CL = 150pF
BUS High Impedance Load 20pF

TIMING WAFEFORMS

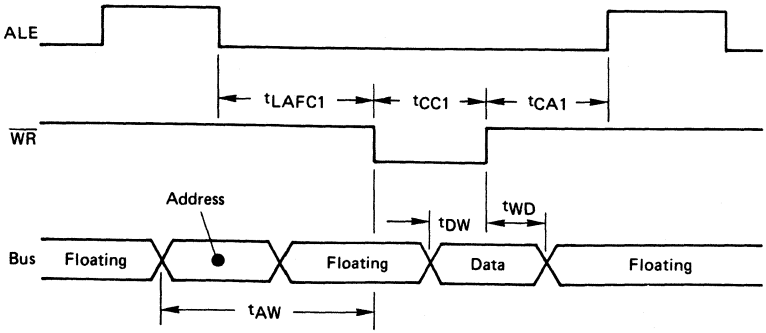
Instruction Fetch from External Memory



Read from External Data Memory

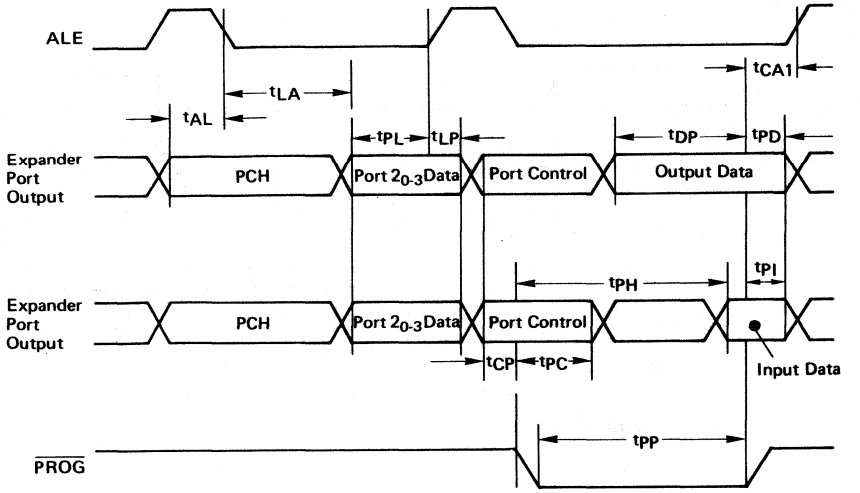


Write to External Memory

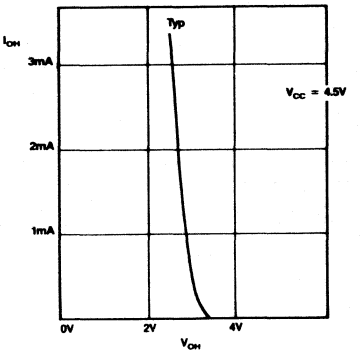


4

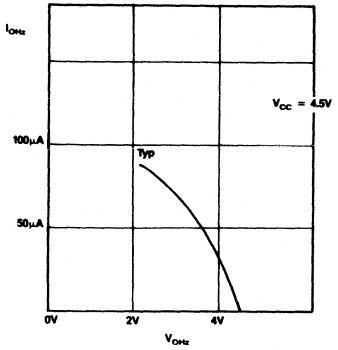
Port 2 Timing



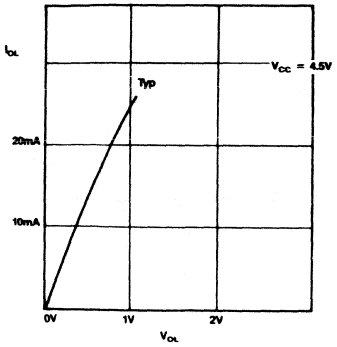
BUS Output High Voltage vs. Source Current



Port P1 and P2 Output
High Voltage vs. Source Current

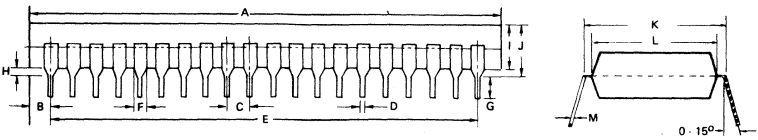


BUS Output Low Voltage vs. Sink Current



40 PIN PLASTIC
μPD8048HC

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62 MAX	0.064 MAX
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.5 MIN	0.06 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24 TYP	0.600 TYP
L	13.2 TYP	0.520 TYP
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



4

HIGH PERFORMANCE SINGLE CHIP 8-BIT MICROCOMPUTERS

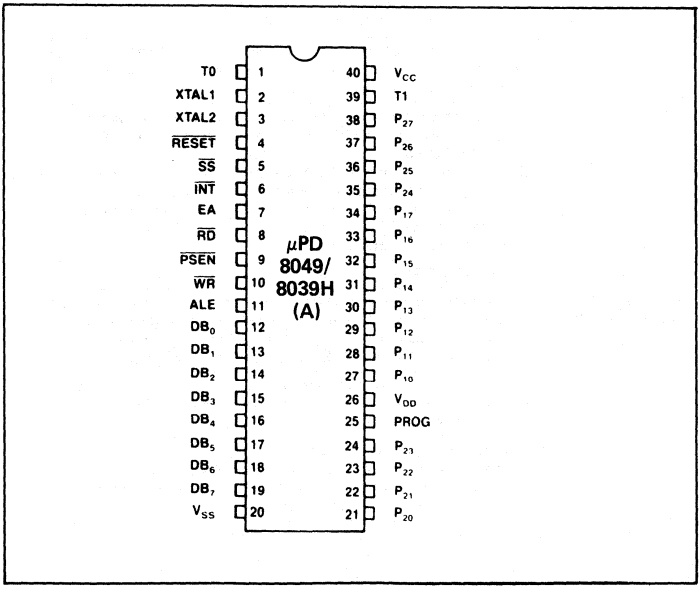
DESCRIPTION

The NEC μPD8049 and μPD8039H are single chip 8-bit microcomputers. The processors differ only in their internal program memory options: the μPD8049 has 2K x 8 bit mask ROM and the μPD8039H has external program memory. Both of these devices feature high performance 11 MHz operation.

FEATURES

- High Performance 11 MHz Operation
- Fully Compatible with Industry Standard 8049/8039
- Pin Compatible with the μPD8048/8748/8035
- NMOS Silicon Gate Technology Requiring a Single +5V ± 10 % Supply
- 1.36 μs Cycle Time. All Instructions 1 or 2 Bytes
- Programmable Interval Timer/Event Counter
- 2K x 8 bit ROM, 128 x 8 bit RAM
- Single Level Interrupt
- 96 Instructions: 70 Percent Single Byte
- 27 I/O Lines
- Internal Clock Generator
- Expandable with 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40-Pin Packages
- Temp Range −40°C to +85°C

PIN CONFIGURATION

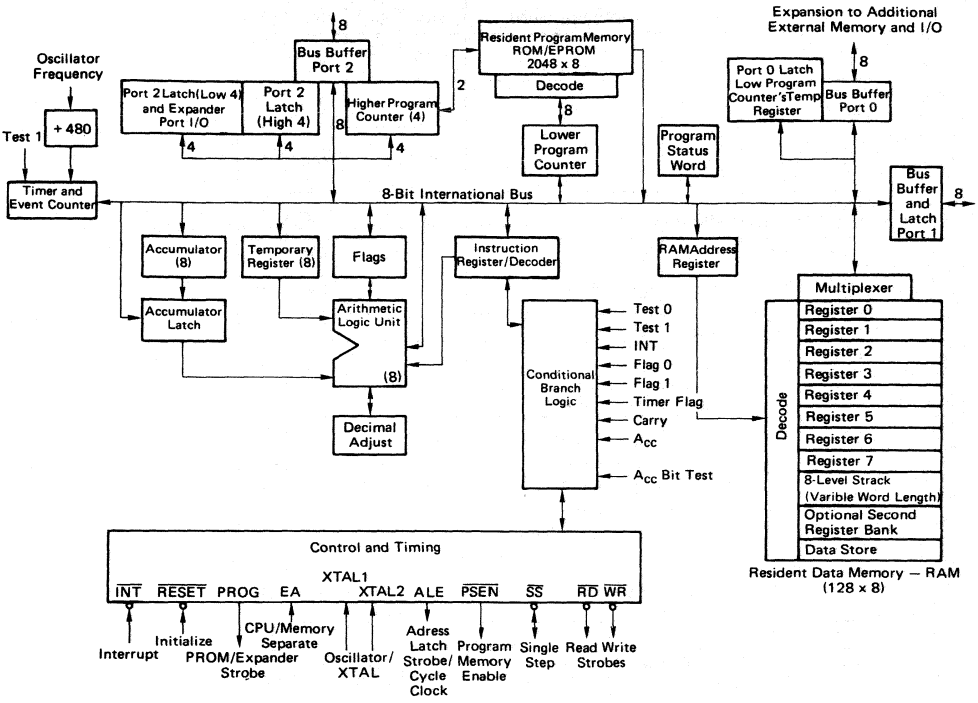


4

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal, LC, or external frequency source. (Non-TTL compatible V_{IH}.)
3	XTAL 2	The other side of the crystal or LC frequency source. For external sources, XTAL 2 must be driven with the logical complement of the XTAL 1 input.
4	$\overline{RESET}$	Active low input from processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non-TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe outputs (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active-high). Occuring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12-19	D_0-D_7 BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the D_0-D_7 BUS can be latched in a static mode. During an external memory fetch, the D_0-D_7 BUS holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the D_0-D_7 BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21-24, 35-38	P_{20}-P_{27}: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in P_{20}-P_{23}. Bits P_{20}-P_{23} are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	PROG is used as an output strobe for μPD8243's during I/O expansion. When the μPD8049 is used in a stand-alone mode the PROG pan can be allowed to float.
26	V_{DD}	V_{DD} is used to provide +5V to the 128 x 8 bit RAM section. During normal operation V_{CC} must also be +5V to provide power to the other functions in the device. During stand-by operation V_{DD} must remain at +5V while V_{CC} is at ground potential.
27-34	P_{10}-P_{17}: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T_1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power supply. V_{CC} is +5V during normal operation.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature	−40°C to +85°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +150°C
Voltage on Any Pin	−0.5V to +7V ①
Power Dissipation	1.5 W

Note: ① With respect to ground.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated unter conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4

DC CHARACTERISTICS

T_a = −40°C to +85°C; V_{CC} = V_{DD} = +5V ± 10 %; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}		−0.5		0.7	V
Input Low Voltage ($\overline{RESET}$, X1, X2)	V_{IL1}		−0.5		0.7	V
Input High Voltage (All Except XTAL 1, XTAL 2, RESET)	V_{IH}		2.3		V_{CC}	V
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}		3.8		V_{CC}	V
Output Low Voltage (BUS)	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
Output Low Voltage (PROG)	V_{OL2}	I_{OL} = 2.0 mA			0.45	V
Output Low Voltage (All Other Outputs)	V_{OL3}	I_{OL} = 2.0 mA			0.45	V
Output High Voltage (BUS)	V_{OH}	I_{OH} = −100 μA	2.4			V
Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, $\overline{ALE}$)	V_{OH1}	I_{OH} = −100 μA	2.4			V
Output High Voltage (All Other Outputs)	V_{OH2}	I_{OH} = −30 μA	2.4			V
Input Leakage Current (T_1, EA, INT)	I_{IL}	$V_{SS} \leq V_{IN} \leq V_{CC}$			±10	μA
Output Leakage Current (BUS, T_0—High Impedance State)	I_{OL}	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V			±10	μA
Power Down Supply Current	I_{DD}	T_a = 25°C		5	10	mA
Total Supply Current	$I_{DD}+I_{CC}$	T_a = 25°C		80	140	mA

AC CHARACTERISTICS

T_a = −40°C to +85°C; V_{CC} = V_{DD} = 5V ± 10 %; V_{SS} = 0V

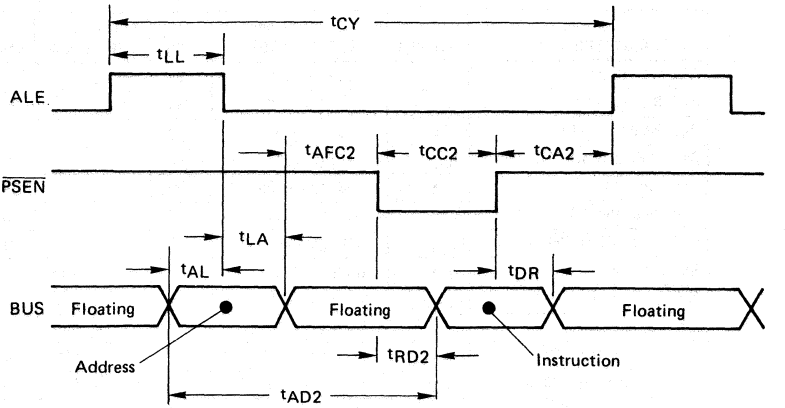
PARAMETER	SYMBOL	f(t_{CY}) and TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
ALE Pulse Width	t_{LL}	7/30 t_{CY} −170	180			ns
Addr Setup to ALE	t_{AL}	2/15 t_{CY} −110	90			ns
Addr Hold from ALE	t_{LA}	1/15 t_{CY} −40	60			ns
Control Pulse Width (RD, WR)	t_{CC1}	1/2 t_{CY} −200	550 400			ns
Data Setup $\overline{WR}$	t_{DW}	13/30 t_{CY} −200	450			ns
Data Hold after $\overline{WR}$	t_{WD}	1/15 t_{CY} −50	50			ns
Data Hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	1/10 t_{CY} −30	0		120	ns
$\overline{RD}$ to Data in	t_{RD1}	2/5 t_{CY} −200			400	ns
$\overline{PSEN}$ to Data in	t_{RD2}	3/10 t_{CY} −200			250	ns
Addr Setup to $\overline{WR}$	t_{AW}	1/3 t_{CY} −150	350			ns
Addr Setup to Data ($\overline{RD}$)	t_{AD1}	11/15 t_{CY} −250			850	ns
Addr Setup to Data ($\overline{PSEN}$)	t_{AD2}	8/15 t_{CY} −250			550	ns
Addr Float to $\overline{RD}$, $\overline{WD}$	t_{AFC1}	2/15 t_{CY} −40	160			ns
Addr Float to $\overline{PSEN}$	t_{AFC2}	1/30 t_{CY} −40	10			ns
ALE to Control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	1/5 t_{CY} −75	420			ns
ALE to Control ($\overline{PSEN}$)	t_{LAFC2}	1/10 t_{CY} −75	170			ns
Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t_{CA1}	1/15 t_{CY} −40	120			ns
Control to ALE ($\overline{PSEN}$)	t_{CA2}	4/15 t_{CY} −40	620			ns
Port Control Setup to $\overline{PROG}$	t_{CP}	1/10 t_{CY} −40	110			ns
Port Control Hold to $\overline{PROG}$	t_{PC}	4/15 t_{CY} −200	200			ns
PROG to P2 Input Valid	t_{PR}	17/30 t_{CY} −120			730	ns
Input Data Hold from $\overline{PROG}$	t_{PF}	1/10 t_{CY}			150	ns
Output Data Setup	t_{DP}	2/5 t_{CY} −150	450			ns
Output Data Hold	t_{PD}	1/10 t_{Cy} −50	100			ns
$\overline{PROG}$ Pulse Width	t_{PP}	7/10 t_{CY} −250	800			ns
Port 2 I/O Setup to ALE	t_{PL}	4/15 t_{CY} −200	200			ns
Port 2 I/O Hold to ALE	t_{LP}	1/10 t_{CY} −100	50			ns
Port Output from ALE	t_{PV}	3/10 t_{CY} +100			850	ns
Cycle Time	t_{CY}	6 MHz	1.5		15.0	μs
TO Rep Rate	t_{OPRR}	3/15 t_{CY}	500			ns

Notes: Output Outputs CL = 80pF
BUS Outputs CL = 150pF
BUS High Impedance Load 20pF

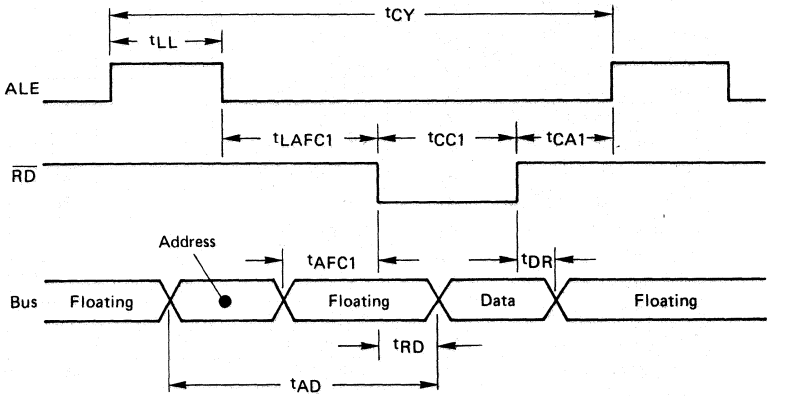
4

TIMING WAFEFORMS

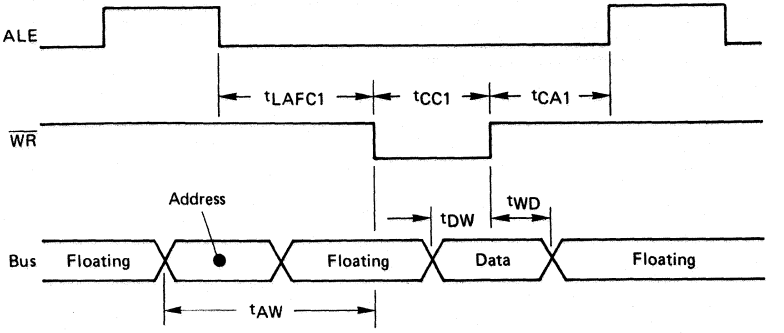
Instruction Fetch from External Memory



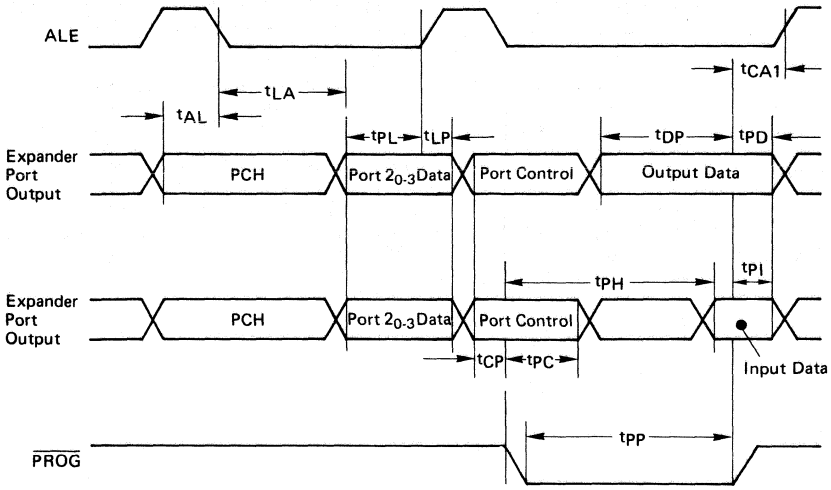
Read from External Data Memory



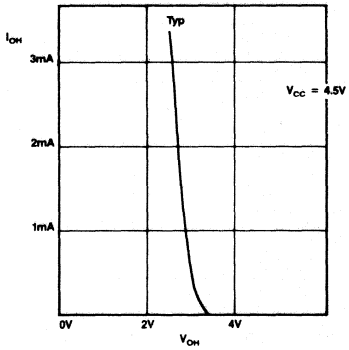
Write to External Memory



Port 2 Timing

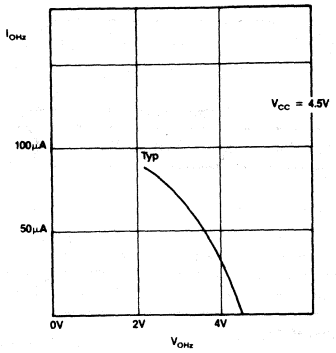


BUS Output High Voltage vs. Source Current

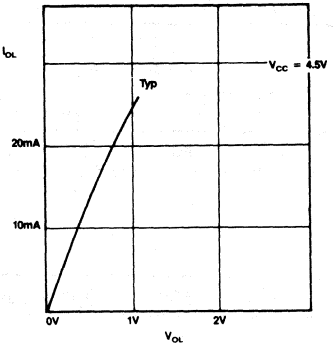


4

Port P1 and P2 Output
High Voltage vs. Source Current

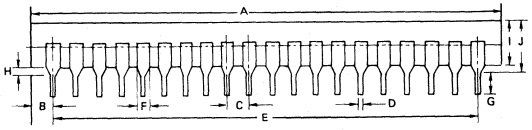


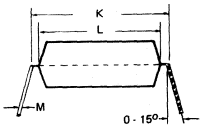
BUS Output Low Voltage vs. Sink Current



ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62 MAX	0.064 MAX
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.5 MIN	0.06 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24 TYP	0.600 TYP
L	13.2 TYP	0.520 TYP
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

40 PIN PLASTIC
μPD8049HC/
μPD8039HLC/
μPD8749HC





THE μCOM84 CMOS FAMILY

μPD80C48/μPD80C35/μPD48
μPD80C49/μPD80C39/μPD49
μPD80C49H/μPD80C39H/μPD49H
μPD80C42
μPD80C50H/μPD80C40H

GENERAL INFORMATION

CMOS MICROCOMPUTER SELECTION GUIDE

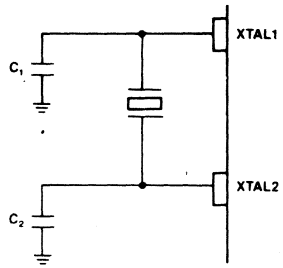
SINGLE CHIP 8-BIT MICROCOMPUTERS

DEVICE	SPECIAL FEATURES	ROM	RAM	I/O	PROCESS	CYCLE	SUPPLY VOLTAGE	PINS
μPD80C35	CMOS 8035	External	64x8	27	CMOS	6 MHz	+2.5 to 6	40/52
μPD80C48	CMOS 8048	1024x8	64x8	27	CMOS	6 MHz	+2.5 to 6	40/44/52
μPD80C39	CMOS 8039	External	128x8	27	CMOS	8 MHz	+2.5 to 6	40/52
μPD80C39H	CMOS 8039H	External	128x8	27	CMOS	12 MHz	+2.5 to 6	40
μPD80C49	CMOS 8049	2048x8	128x8	27	CMOS	8 MHz	+2.5 to 6	40/44/52
μPD80C49H	CMOS 8049H	2048x8	128x8	27	CMOS	12 MHz	+2.5 to 6	40/44
μPD80C49H (S)	CMOS 8049H (S)*	2048x8	128x8	27	CMOS	10 MHz	+2.5 to 6	40
μPD80C42	INTERFACE WITH SLAVE BUS	2048x8	128x8	18	CMOS	12 MHz	+2.5 to +6	40
μPD80C40H	LARGE MEMORY	4096x8	256x8	16	CMOS	12 MHz	2.5 to +6	40
μPD80C50H	LARGE MEMORY	4096x8	256x8	16	CMOS	12 MHz	2.5 to +6	40/44

NOTE SPECIAL S GRADE VERSION

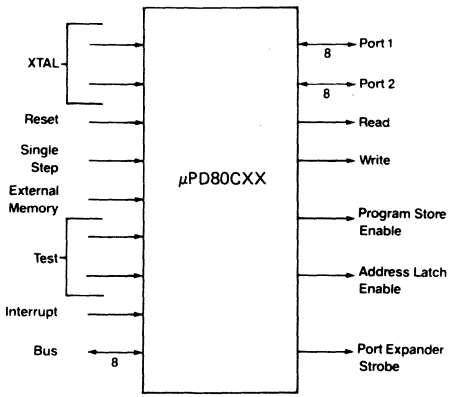
*	NORMAL	(S) GRADE
1st electrical test	at room temp	at 110°C
burn in	4 hours	16 hours
2nd electrical test	at room temp	at room temp

Crystal Resonator Frequency Reference Circuit

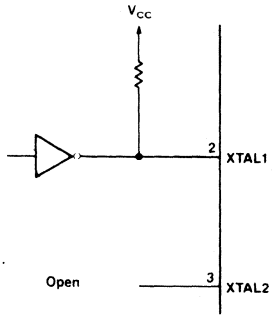


① Crystal oscillator constants of f_{OSC} = 6 MHz / R_{max} = 50Ω / C_L = 16 ± 0.2 pF / P = 1 ± 0.2 mW
② Operating frequency less than 4 MHz / $0 < C_1 < 20$ pF / $0 < C_2 < 20$ pF / $|C_2 - C_1| < 10$ pF
③ Operating frequency more than 4 MHz / $0 < C_1 < 10$ pF / $0 < C_2 < 10$ pF / $|C_2 - C_1| < 5$ pF

MAJOR INPUT AND OUTPUT SIGNALS



External Clock Frequency Reference Circuit



Note: A minimum voltage of V_{CC}-1 is required for XTAL1 to go HIGH.

4

INSTRUCTION SET

INSTRUCTION SET SYMBOL DEFINITIONS

SYMBOL	DESCRIPTION
A	Accumulator
AC	Auxiliary Carry Flag
addr	Program or data memory address (a_0–a_7) or (a_0–a_{10})
b	Accumulator bit (b = 0–7)
BS	Bank Swith
BUS	Bus
C	Carry Flag
CLK	Clock
CNT	Counter
data	8-bit binary data (d_0–d_7)
DBF	Memory Bank Flip-Flop
F0, F1	Flag 0, Flag 1
INT	Interrupt pin
	Indicates the hex number of the specified register or port
PC	Program Counter
P_p	Port 1, Port 2, or Port 4–7 ($_p$ = 1, 2, or 4–7)
PSW	Program Status Word
R_r	Register R_0–R_7 ($_r$ = 0–7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T0, T1	Test 0, Test 1 pin
#	Immediate data indication
@	Indirect address indication
x	Indicates the hex number corresponding to the accumulator bit or page number specified in the operand
(x)	Contents of RAM
((x))	Contents of memory addressed by (x)
←	Transfer direction, result
∧	Logical product (logical AND)
∨	Logical sum (logical OR)
∀	Exclusive OR
–	Complement

4

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Accumulator													
ADD A, # data	(A) ← (A) + data	Adds immediate data d_0–d_7 to the accumulator. Sets or clears both carry flags.②	03	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADD A, R$_r$	(A) ← (A) + (R$_r$) r = 0–7	Adds the contents of register R$_r$ to the accumulator. Sets or clears both carry flags.②	6n④	0	1	1	0	1	r	r	r	1	1
ADD A, @ R$_r$	(A) ← (A) + ((R$_r$)) r = 0–1	Adds the contents of the internal data memory location specified by bits 0–5 of register R$_r$ to the accumulator. Sets or clears both carry flags.②	6n④	0	1	1	0	0	0	0	r	1	1
ADDC A, # data	(A) ← (A) + data + (C)	Adds, with carry, immediate data d_0–d_7 to the accumulator. Sets or clears both carry flags.②	13	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADDC A, R$_r$	(A) ← (A) + (R$_r$) + (C) r = 0–7	Adds, with carry, the contents of register R$_r$ to the accumulator. Sets or clears both carry flags.②	7n④	0	1	1	1	1	r	r	r	1	1
ADDC A, @ R$_r$	(A) ← (A) + ((R$_r$)) + (C) r = 0–1	Adds, with carry, the contents of the internal data memory location specified by bits 0–5 of register R$_r$, to the accumulator. Sets or clears both carry flags.②	7n④	0	1	1	1	0	0	0	r	1	1
ANL A, # data	(A) ← (A)∧data	Takes the logical product (logical AND) of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	53	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ANL A, R$_r$	(A) ← (A)∧(R$_r$) r = 0–7	Takes the logical product (logical AND) of the contents of register R$_r$ and the accumulator, and stores the result in the accumulator.	5n④	0	1	0	1	1	r	r	r	1	1
ANL A, @ R$_r$	(A) ← (A)∧((R$_r$)) r = 0–1	Takes the logical product (logical AND) of the contents of the internal data memory location specified by bits 0–5 of register R$_r$, and the accumulator, and stores the result in the accumulator.	5n④	0	1	0	1	0	0	0	r	1	1
CPL A	(A) ← $\overline{(A)}$	Takes the complement of the contents of the accumulator.	37	0	0	1	1	0	1	1	1	1	1
CLR A	(A) ← 0	Clears the contents of the accumulator.	27	0	0	1	0	0	1	1	1	1	1
DA A		Converts the contents of the accumulator to BCD. Sets or clears the carry flags. When the lower 4 bits (A_{0-3}) are greater than 9, or if the Auxiliary Carry Flag has been set, adds 6 to A_{0-3}. When the upper 4 bits (A_{4-7}) are greater than 9 or if the Carry Flag (C) has been set, adds 6 to A_{4-7}. If an overflow occurs at this point, C is set.②	57	0	1	0	1	0	1	1	1	1	1
DEC A	(A) ← (A) − 1	Decrements the contents of the accumulator by 1.	07	0	0	0	0	0	1	1	1	1	1
INC A	(A) ← (A) + 1	Increments the contents of the accumulator by 1.	17	0	0	0	1	0	1	1	1	1	1
ORL A, # data	(A) ← (A)∨data	Takes the logical sum (logical OR) of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	43	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ORL A, R$_r$	(A) ← (A)∨(R$_r$) r = 0–7	Takes the logical sum (logical OR) of register R$_r$ and the contents of the accumulator, and stores the result in the accumulator.	4n④	0	1	0	0	1	r	r	r	1	1
ORL A, @ R$_r$	(A) ← (A)∨((R$_r$)) r = 0–1	Takes the logical sum (logical OR) of the contents of the internal data memory location specified by bits 0–5 in register R$_r$, and the contents of the accumulator, and stores the result in the accumulator.	4n④	0	1	0	0	0	0	0	r	1	1
RL A	(Ab + 1) ← (Ab) (A$_0$) ← (A$_7$) b = 0–6	Rotates the contents of the accumulator one bit to the left. The MSB is rotated into the LSB.	E7	1	1	1	0	0	1	1	1	1	1
RLC A	(Ab + 1) ← (Ab) (A$_0$) ← (C) (C) ← (A$_7$) b = 0–6	Rotates the contents of the accumulator one bit to the left through carry.	F7	1	1	1	1	0	1	1	1	1	1
RR A	(Ab) ← (Ab + 1) (A$_7$) ← (A$_0$) b = 0–6	Rotates the contents of the accumulator one bit to the right. The LSB is rotated into the MSB.	77	0	1	1	1	0	1	1	1	1	1
RRC A	(Ab) ← (Ab + 1) (A$_7$) ← (C) (C) ← (A$_0$) b = 0–6	Rotates the contents of the accumulator one bit to the right through carry.	67	0	1	1	0	0	1	1	1	1	1
SWAP A	(A$_{4-7}$) ↔ (A$_{0-3}$)	Exchanges the contents of the lower 4 bits of the accumulator with the upper 4 bits of the accumulator.	47	0	1	0	0	0	1	1	1	1	1
XRL A, # data	(A) ← (A)∀data	Takes the exclusive OR of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	D3	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
XRL A, R$_r$	(A) ← (A)∀(R$_r$) r = 0–7	Takes the exclusive OR of the contents of register R$_r$ and the accumulator, and stores the result in the accumulator.	Dn④	1	1	0	1	1	r	r	r	1	1
XRL A, @ R$_r$	(A) ← (A)∀((R$_r$)) r = 0–1	Takes the exclusive OR of the contents of the location in data memory specified by bits 0–5 in register R$_r$, and the accumulator, and stores the result in the accumulator.	Dn④	1	1	0	1	0	0	0	r	1	1
Branch													
DJNZ R$_r$, addr	(R$_r$) ← (R$_r$) − 1 If (R$_r$) ≠ 0, then (PC$_{0-7}$) ← addr r = 0–7	Decrements the contents of register R$_r$ by 1, and if the result is not equal to 0, jumps to the address indicated by a_0–a_7.	En	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2
JBb addr	(PC$_{0-7}$) ← addr if b = 1 (PC) = (PC) + 2 if b = 0	Jumps to the address specified by a_0–a_7 if the bit in the accumulator specified by b_0–b_2 is set.	x2⑤	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Branch (Cont.)													
JC addr	$(PC_{0-7}) \leftarrow$ addr if C = 1 $(PC) \leftarrow (PC) + 2$ if C = 0	Jumps to the address specified by a_0-a_7 if the Carry Flag is set.	F6	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF0 addr	$(PC_{0-7}) \leftarrow$ addr if F0 = 1 $(PC) \leftarrow (PC) + 2$ if F0 = 0	Jumps to the address specified by a_0-a_7 if F0 is set.	B6	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF1 addr	$(PC_{0-7}) \leftarrow$ addr if F1 = 1 $(PC) \leftarrow (PC) + 2$ if F1 = 0	Jumps to the address specified by a_0-a_7 if F1 is set.	76	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JMP addr	$(PC_{8-10}) \leftarrow$ addr$_{8-10}$ $(PC_{0-7}) \leftarrow$ addr$_{0-7}$ $(PC_{11}) \leftarrow$ DBF	Jumps directly to the address specified by a_0-a_{10} and the DBF.	x4④	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
JMPP @ A	$(PC_{0-7}) \leftarrow ((A))$	Replaces the lower 8 bits of the Program Counter with the contents of program memory specified by the contents of the accumulator, producing a jump to the specified address within the current page.	B3	1	0	1	1	0	0	1	1	2	1
JNC addr	$(PC_{0-7}) \leftarrow$ addr if C = 0 $(PC) \leftarrow (PC) + 2$ if C = 1	Jumps to the address specified by a_0-a_7 if the Carry Flag is not set.	E6	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNI addr	$(PC_{0-7}) \leftarrow$ addr if I = 0 $(PC) \leftarrow (PC) + 2$ if I = 1	Jumps to the address specified by a_0-a_7 if the Interrupt Flag is not set.	86	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT0 addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 0 $(PC) \leftarrow (PC) + 2$ if T0 = 1	Jumps to the address specified by a_0-a_7 if Test 0 is LOW.	26	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT1 addr	$(PC_{0-7}) \leftarrow$ addr if T1 = 0 $(PC) \leftarrow (PC) + 2$ if T1 = 1	Jumps to the address specified by a_0-a_7 if Test 1 is LOW.	46	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNZ addr	$(PC_{0-7}) \leftarrow$ addr if A ≠ 0 $(PC) \leftarrow (PC) + 2$ if A = 0	Jumps to the address specified by a_0-a_7 if the contents of the accumulator are not equal to 0.	96	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JTF addr	$(PC_{0-7}) \leftarrow$ addr if TF = 1 $(PC) \leftarrow (PC) + 2$ if TF = 0	Jumps to the address specified by a_0-a_7 if the Timer Flag is set. The Timer Flag is cleared after the instruction is executed.	16	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT0 addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 1 $(PC) \leftarrow (PC) + 2$ if T0 = 0	Jumps to the address specified by a_0-a_7 if Test 0 is HIGH.	36	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT1 addr	$(PC_{0-7}) \leftarrow$ addr if T1 = 1 $(PC) \leftarrow (PC) + 2$ if T1 = 0	Jumps to the address specified by a_0-a_7 if Test 1 is HIGH.	56	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JZ	$(PC_{0-7}) \leftarrow$ addr if A = 0 $(PC) \leftarrow (PC) + 2$ if A = 1	Jumps to the address specified by a_0-a_7 if the contents of the accumulator are equal to 0.	C6	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
Control													
EN I		Enables external interrupts. When external interrupts are enabled, a low-level input to the INT pin causes the processor to vector to the interrupt service routine.	05	0	0	0	0	0	1	0	1	1	1
DIS I		Disables external interrupts. When external interrupts are disabled, low-level inputs to the INT pin have no effect on program execution.	15	0	0	0	1	0	1	0	1	1	1
ENT0 CLK		Enables clock output to pin T0.	75	0	1	1	1	0	1	0	1	1	1
SEL MB0	(DBF) ← 0	Clears the Memory Bank Flip-Flop, selecting Program Memory Bank 0 [program memory addresses $0-2047_{(10)}$]. Clears PC_{11} after the next JMP or CALL instruction.	E5	1	1	1	0	0	1	0	1	1	1
SEL MB1	(DBF) ← 1	Sets the Memory Bank Flip-Flop, selecting Program Memory Bank 1 [program memory addresses $2048-4095_{(10)}$]. Sets PC_{11} after the next JMP or CALL instruction.	F5	1	1	1	1	0	1	0	1	1	1
SEL RB0	(BS) ← 0	Selects Data Memory Bank 0 by clearing bit 4 (Bank Switch) of the PSW. Specifies data memory addresses $0-7_{(10)}$ as registers 0–7 of Data Memory Bank 0.	C5	1	1	0	0	0	1	0	1	1	1
SEL RB1	(BS) ← 1	Selects Data Memory Bank 1 by setting bit 4 (Bank Switch) of the PSW. Specifies data memory $24-31_{(10)}$ as registers 0–7 of Data Memory Bank 1.	D5	1	1	0	1	0	1	0	1	1	1
HALT		Initiates Halt mode.	01	0	0	0	0	0	0	0	1	1	1
STOP	(not all devices)	Initiates Software Stop mode	82	1	0	0	0	0	0	1	0	1	1
Data Moves													
MOV A, # data	(A) ← data	Moves immediate data d_0-d_7 into the accumulator.	23	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
MOV A, R$_r$	(A) ← (R$_r$) $r = 0-7$	Moves the contents of register R_r into the accumulator.	Fn④	1	1	1	1	1	r	r	r	1	1
MOV A, @ R$_r$	(A) ← ((R$_r$)) $r = 0-1$	Moves the contents of internal data memory specified by bits 0–5 in register R_r, into the accumulator.	Fn④	1	1	1	1	0	0	0	r	1	1
MOV A, PSW	(A) ← (PSW)	Moves the contents of the Program Status Word into the accumulator.	C7	1	1	0	0	0	1	1	1	1	1
MOV R$_r$, # data	(R$_r$) ← data $r = 0-7$	Moves immediate data d_0-d_7 into register R_r.	Bn④	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2
MOV R$_r$, A	(R$_r$) ← (A) $r = 0-7$	Moves the contents of the accumulator into register R_r.	An④	1	0	1	0	1	r	r	r	1	1
MOV @ R$_r$, A	((R$_r$)) ← (A) $r = 0-1$	Moves the contents of the accumulator into the data memory location specified by bits 0–5 in register R_r.	An④	1	0	1	0	0	0	0	r	1	1
MOV @ R$_r$, # data	((R$_r$)) ← data $r = 0-1$	Moves immediate data d_0-d_7 into the data memory location specified by bits 0–5 in register R_r.	Bn④	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2
MOV PSW, A	(PSW) ← (A)	Moves the contents of the accumulator into the Program Status Word.	D7	1	1	0	1	0	1	1	1	1	1

4

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Data Moves (Cont.)													
MOVP A, @ A	$(PC_{8-7}) \leftarrow (A)$ $(A) \leftarrow ((PC))$	Moves the contents of the program memory location specified by PC_{8-11} concatenated with the contents of the accumulator, into the accumulator.	A3	1	0	1	0	0	0	1	1	2	1
MOVP3 A, @ A	$(PC_{8-7}) \leftarrow (A)$ $(PC_{8-11}) \leftarrow 001$ $(A) \leftarrow ((PC))$	Moves the contents of the program memory location specified by 0011 (PC_{8-11}, page 3 of Program Memory Bank 0) and the contents of the accumulator, into the accumulator.	E3	1	1	1	0	0	0	1	1	2	1
MOVX A, @ R	$(A) \leftarrow ((R_r))$ $r = 0–1$	Moves the contents of the external data memory location specified by register R_r, into the accumulator.	8n④	1	0	0	0	0	0	0	r	2	1
MOVX @ R, A	$((R_r)) \leftarrow (A)$ $r = 0–1$	Moves the contents of the accumulator into the external data memory location specified by register R_r.	9n④	1	0	0	1	0	0	0	r	2	1
XCH A, R$_r$	$(A) \leftrightarrow (R_r)$ $r = 0–7$	Exchanges the contents of the accumulator and register R_r.	2n④	0	0	1	0	1	r	r	r	1	1
XCH A, @ R$_r$	$(A) \leftrightarrow ((R_r))$ $r = 0–1$	Exchanges the contents of the accumulator and the contents of the data memory location specified by bits 0–5 in register R_r.	2n④	0	0	1	0	0	0	0	r	1	1
XCHD A, @ R$_r$	$(A_{6-3}) \leftrightarrow ((R_{6-3}))$ $r = 0–1$	Exchanges the contents of the lower 4 bits of the accumulator with the contents of the lower 4 bits of the internal data memory location specified by bits 0–5 in register R_r.	3n④	0	0	1	1	0	0	0	r	1	1
Flags													
CPL C	$(C) \leftarrow \overline{(C)}$	Takes the complement of the Carry bit.	A7	1	0	1	0	0	1	1	1	1	1
CPL F0	$(F0) \leftarrow \overline{(F0)}$	Takes the complement of Flag 0.	95	1	0	0	1	0	1	0	1	1	1
CPL F1	$(F1) \leftarrow \overline{(F1)}$	Takes the complement of Flag 1.	B5	1	0	1	1	0	1	0	1	1	1
CLR C	$(C) \leftarrow 0$	Clears the Carry bit.	97	1	0	0	1	0	1	1	1	1	1
CLR F0	$(F0) \leftarrow 0$	Clears Flag 0.	85	1	0	0	0	0	1	0	1	1	1
CLR F1	$(F1) \leftarrow 0$	Clears Flag 1.	A5	1	0	1	0	0	1	0	1	1	1
Input/Output													
ANL BUS, # data	$(BUS) \leftarrow (BUS) \wedge data$	Takes the logical AND of the contents of the bus and immediate data $d_0–d_7$, and sends the result to the bus.	98	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ANL P$_p$, # data	$(P_p) \leftarrow (P_p) \wedge data$ $p = 1–2$	Takes the logical AND of the contents of designated port P_p and immediate data $d_0–d_7$, and sends the result to port P_p for output.	9n⑤	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
ANLD P$_p$, A	$(P_p) \leftarrow (P_p) \wedge (A_{3-0})$ $p = 4–7$	Takes the logical AND of the contents of designated port P_p and the lower 4 bits of the accumulator, and sends the result to port P_p for output.	9n⑤	1	0	0	1	1	1	p	p	2	1
IN A, P$_p$	$(A) \leftarrow (P_p)$ $p = 1–2$	Loads the accumulator with the contents of designated port P_p.	0n⑤	0	0	0	0	1	0	p	p	2	1
INS A, BUS	$(A) \leftarrow (BUS)$	Loads the contents of the bus into the accumulator on the rising edge of RD.	08	0	0	0	0	1	0	0	0	2	1
MOVD A, P$_p$	$(A_{3-0}) \leftarrow (P_p)$ $(A_{7-4}) \leftarrow 0$ $p = 4–7$	Moves the contents of designated port P_p to the lower 4 bits of the accumulator, and clears the upper 4 bits.	0n⑤	0	0	0	0	1	1	p	p	2	1
MOVD P$_p$, A	$(P_p) \leftarrow (A_{3-0})$ $p = 4–7$	Moves the lower 4 bits of the accumulator to designated port P_p. The upper 4 bits of the accumulator are not changed.	3n⑤	0	0	1	1	1	1	p	p	2	1
ORL BUS, # data	$(BUS) \leftarrow (BUS) \vee data$	Takes the logical OR of the contents of the bus and immediate data $d_0–d_7$, and sends the result to the bus.	88	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ORLD P$_p$, A	$(P_p) \leftarrow (P_p) \vee (A_{3-0})$ $p = 4–7$	Takes the logical OR of the contents of designated port P_p and the lower 4 bits of the accumulator, and sends the result to port P_p for output.	8n⑤	1	0	0	0	1	1	p	p	2	1
ORL P$_p$, # data	$(P_p) \leftarrow (P_p) \vee data$ $p = 1–2$	Takes the logical OR of the contents of designated port P_p and immediate data $d_0–d_7$, and sends the result to port P_p for output.	9n⑤	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
OUTL BUS, A	$(BUS) \leftarrow (A)$	Latches the contents of the accumulator onto the bus on the rising edge of WR. Note: Never use the OUTL BUS instruction when using external program memory, as this will permanently latch the bus.	02	0	0	0	0	0	0	1	0	2	1
OUTL P$_p$, A	$(P_p) \leftarrow (A)$ $p = 1–2$	Latches the contents of the accumulator into designated port P_p for output.	3n⑤	0	0	1	1	1	0	p	p	2	1
Registers													
DEC R$_r$	$(R_r) \leftarrow (R_r) - 1$ $r = 0–7$	Decrements the contents of register R_r by 1.	Cn④	1	1	0	0	1	r	r	r	1	1
INC R$_r$	$(R_r) \leftarrow (R_r) + 1$ $r = 0–7$	Increments the contents of register R_r by 1.	1n④	0	0	0	1	1	r	r	r	1	1
INC @ R$_r$	$((R_r)) \leftarrow ((R_r)) + 1$ $r = 0–1$	Increments by 1 the contents of the data memory location specified by bits 0–5 in register R_r.	1n④	0	0	0	1	0	0	0	r	1	1

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Subroutine													
CALL addr	((SP)) ← (PC), (PSW$_{4-7}$) (SP) ← (SP) + 1 (PC$_{8-10}$) ← addr$_{8-10}$ (PC$_{0-7}$) ← addr$_{0-7}$ (PC$_{11}$) ← DBF	Stores the contents of the Program Counter and the upper 4 bits of the PSW in the address indicated by the Stack Pointer, and increments the contents of the Stack Pointer, calling the subroutine specified by address a_0–a_{10} and the DBF.	x4④	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
RET	(SP) ← (SP) − 1 (PC) ← ((SP))	Decrements the contents of the Stack Pointer by 1 and stores, in the Program Counter, the contents of the location specified by the Stack Pointer, executing a return from subroutine without restoring the PSW.	83	1	0	0	0	0	0	1	1	2	1
RETR	(SP) ← (SP) − 1 (PC) ← ((SP)) (PSW$_{4-7}$) ← ((SP))	Decrements the contents of the Stack Pointer by 1 and stores, in the Program Counter, the contents of the upper 4 bits of the PSW and the contents of the location specified by the Stack Pointer, executing a return from subroutine with restoration of the PSW.	93	1	0	0	1	0	0	1	1	2	1
Timer/Counter													
EN TCNTI		Enables internal interrupt of timer/event counter. If an overflow condition occurs, then an interrupt will be generated.	25	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disables internal interrupt of timer/event counter.	35	0	0	1	1	0	1	0	1	1	1
MOV A, T	(A) ← (T)	Moves the contents of the timer/counter into the accumulator.	42	0	1	0	0	0	0	1	0	1	1
MOV T, A	(T) ← (A)	Moves the contents of the accumulator into the timer/counter.	62	0	1	1	0	0	0	1	0	1	1
STOP TCNT		Stops the operation of the timer/event counter.	65	0	1	1	0	0	1	0	1	1	1
STRT CNT		Starts the event counter operation of the timer/counter when T1 changes from a low-level input to a high-level input.	45	0	1	0	0	0	1	0	1	1	1
STRT T		Starts the timer operation of the timer/counter. The timer is incremented every 32 machine cycles.	55	0	1	0	1	0	1	0	1	1	1
Miscellaneous													
NOP		Uses one machine cycle without performing any operation.	00	0	0	0	0	0	0	0	0	1	1

Notes: ① Binary instruction code designations $_a$ and $_b$ represent encoded values or the lowest-order bit value of specified registers and ports, respectively.

② Execution of the ADD, ADDC, and DA instructions affect the carry flags, which are not shown in the respective function equations. These instructions set the carry flags when there is an overflow in the accumulator (the Auxiliary Carry Flag is set when there is an overflow of bit 3 of the accumulator) and clear the carry flags when there is no overflow. Flags that are specifically addressed by flag instructions are shown in the function equations for those instructions.

③ References to addresses and data are specified in byte 1 and/or 2 in the opcode of the corresponding instruction.

④ The hex value of n for specific registers is as follows:

a) Direct addressing
R_0: n = 8 R_2: n = A R_4: n = C R_6: n = E
R_1: n = 9 R_3: n = B R_5: n = D R_7: n = F

b) Indirect addressing
@ R_0: n = 0 @ R_1: n = 1

⑤ The hex value of n for specific ports is as follows:
P_1: n = 9 P_4: n = C P_6: n = E
P_2: n = A P_5: n = D P_7: n = F

⑥ The hex value of x for specific accumulator or address bits is as follows:

a) JBb instruction
B_0: x = 1 B_2: x = 5 B_4: x = 9 B_6: x = D
B_1: x = 3 B_3: x = 7 B_5: x = B B_7: x = F

b) JMP instruction
Page 0: x = 0 Page 2: x = 4 Page 4: x = 8 Page 6: x = C
Page 1: x = 2 Page 3: x = 6 Page 5: x = A Page 7: x = E

c) CALL instruction
Page 0: x = 1 Page 2: x = 5 Page 4: x = 9 Page 6: x = D
Page 1: x = 3 Page 3: x = 7 Page 5: x = B Page 7: x = F

CMOS 8-BIT SINGLE-CHIP MICROCOMPUTER

CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

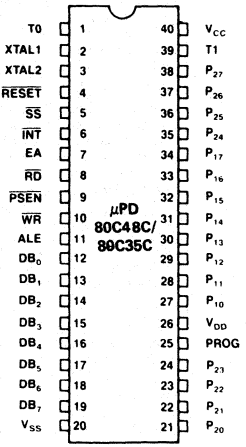
The NEC μPD80C48 is a true stand-alone 8-bit microcomputer fabricated using CMOS technology. All of the functional blocks necessary for an integrated microcomputer are incorporated, including a 1K-byte ROM, a 64-byte RAM, 27 I/O lines, an 8-bit timer/event counter, and a clock generator. This integrated capability permits use in stand-alone applications. For designs requiring extra capability, the μPD80C48 can be expanded using peripherals and memory compatible with industry-standard 8080A/8085A processors. A version of the μPD80C48 without ROM is offered by the μPD80C35.

Providing compatibility with industry-standard 8048, 8748, and 8035 processors, the μPD80C48 features significant savings in power consumption. In addition to the power savings gained through CMOS technology, the μPD80C48 is distinct in offering two standby modes (Halt mode and Stop mode) to further minimize power drain.

FEATURES

- 8-bit CPU with ROM, RAM, and I/O on a single chip
- Hardware/software-compatible with industry-standard 8048, 8748, and 8035 processors
- 1K x 8 ROM
- 64 x 8 RAM
- 27 I/O lines
- 2.5 μs cycle time (6 MHz crystal)
- All instructions executable in 1 or 2 cycles
- 97 instructions: 70 percent are single-byte instructions
- Internal timer/event counter
- 2 interrupts (an external interrupt and a timer interrupt)
- Easily expandable memory and I/O
- Bus compatible with 8080A/8085A peripherals
- Power-efficient CMOS technology requiring a single +2.5V to +6V power supply
- Available in 40-pin DIP, 44-pin flat pack, and 52-pin flat pack
- Halt mode
  - 1 mA typical supply current
  - Maintenance of internal logic values and control states
  - Mode initialization via HALT instruction
  - Mode release via external interrupt or reset
- Stop mode
  - 1 μA typical supply current
  - Disabling of internal clock generation and internal logic
  - Maintenance of RAM contents
  - Mode initialization via hardware (V_{DD})
  - Mode release via reset

PIN CONFIGURATION μPD80C48C/μPD80C35C (40 PIN PLASTIC DIP)



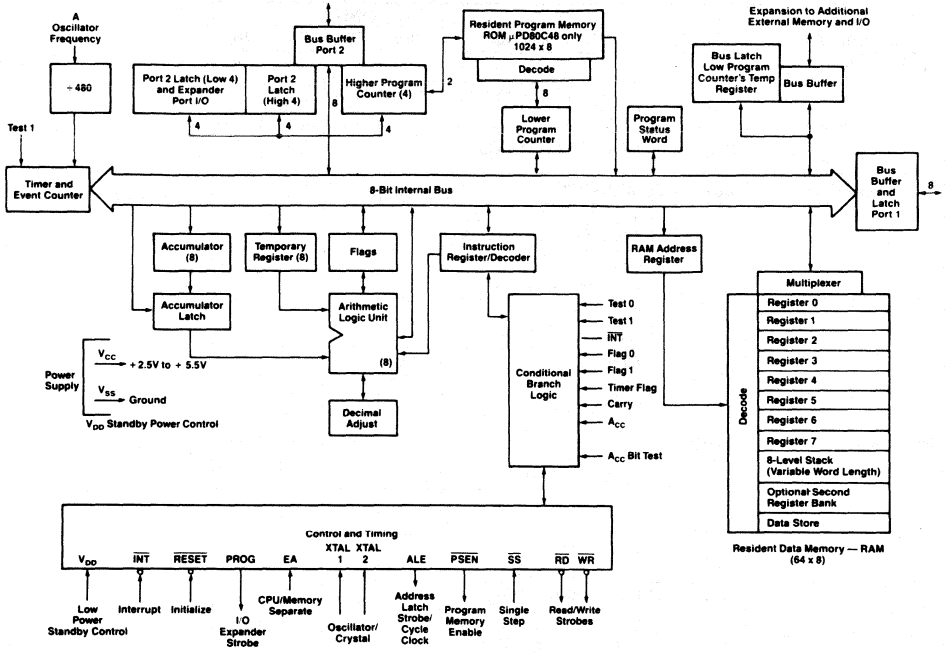
PIN IDENTIFICATION

A.
μPD80C48C/μPD80C35C
(40 PIN PLASTIC DIP)

PIN			
A.	SYMBOL	NAME	FUNCTION
1	T0	Test 0	Testable input using conditional jump instructions JT0 and JNT0. Also enables clock output via the ENT0 CLK instruction.
2	XTAL1	Crystal 1	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. May also be used as an input for external clock signals. (Non-TTL-compatible V_{IH}.)
3	XTAL2	Crystal 2	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. (Non-TTL-compatible V_{IH}.)
4	$\overline{RESET}$	Reset	Active-low input line that initializes the processor. Also used to release both the Halt and Stop modes. ①
5	$\overline{SS}$	Single Step	Active-low input line, that, in conjunction with ALE, causes the processor to single-step through a program one instruction at a time.
6	$\overline{INT}$	Interrupt	Active-low input line that causes an interrupt if an enable instruction has been executed. A reset disables the interrupt. May be used as a testable input with a conditional jump instruction. Can also be used to release the Halt mode.
7	EA	External Access	Input line that inhibits internal program memory fetches and initiates access of external program memory. Essential for system testing and may also be used for program debugging.
8	$\overline{RD}$	Read	Active-low output strobe line that is used to read data from external data memory.
9	$\overline{PSEN}$	Program Store Enable	Active-low output line that is used to fetch instructions from external program memory.
10	$\overline{WR}$	Write	Active-low output strobe line that is used to write data into external data memory.
11	ALE	Address Latch Enable	Output line for address latch enable. At the falling edge of ALE, the address of either external data memory or external program memory is available on the bus.
12-19	DB_0-DB_7	Bus	These I/O lines constitute an 8-bit bidirectional data/address bus. Synchronous read and write operations can be performed on this bus using $\overline{RD}$ and $\overline{WR}$ signals. Data driven out on the bus by an OUTL BUS instruction is statically latched. The address of external memory is available on the bus at the falling edge of ALE when reading from external program memory or writing to and reading from external data memory. During external program memory fetches, the least-significant 8 bits of the external program memory address are driven out on the bus and the addressed instruction is fetched using $\overline{PSEN}$. When no external memory is used, the bus can serve as a true bidirectional 8-bit port. Information is strobed in or out by the $\overline{RD}$ and $\overline{WR}$ signals.
20	V_{SS}	Ground	Ground potential.
21-24, 35-38	P_{20}-P_{27}	Port 2	These lines constitute Port 2, an 8-bit quasi-bidirectional port. During external program memory fetches P_{20}-P_{23} output the most-significant 4 bits of the external program memory address. Lines P_{20}-P_{23} can also be used as a 4-bit I/O expander bus to interface with the optional μPD82C43 I/O expander.
25	PROG	Program Pulse	This line is used as an output strobe when interfacing with the optional μPD82C43 I/O expander.
26	V_{DD}	Oscillator Control Voltage Line	This input line is used to control oscillator stopping and restarting in Stop mode. Stop mode is enabled by forcing V_{DD} Low during a reset.
27-34	P_{10}-P_{17}	Port 1	These lines constitute Port 1, an 8-bit, generalpurpose quasi-bidirectional port.
39	T1	Test 1	Testable input using conditional jump instructions JT1 and JNT1. Can also be used as the timer/counter input line via the STRT CNT instruction.
40	V_{CC}	Primary Power Supply	Power supply. V_{CC} must be between +2.5V to +6V for normal operation. In Stop mode, V_{CC} must be at least +2V to ensure data retention.

Note: ①The pulse width of $\overline{RESET}$ must be a minimum of 5 machine cycles in length following oscillator stabilization to reinitialize the processor and stabilize CPU operation. At power-up, the states of the output lines are undefined until completion of reset.

BLOCK DIAGRAM



4

ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature, T_{opt}	−40°C to +85°C
Storage Temperature (Plastic Package), T_{stg}	−65°C to +150°C
Voltage on Any Pin, $V_{I/O}$	V_{SS} −0.3V to V_{CC} +0.3V
Supply Voltage, V_{CC}	V_{SS} −0.3 to +10V
Power Dissipation, P_D with I_{CC} = max. 8 mA and V_{CC} = 5V nominal P_D = 40 mW	40 mW

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS **Standard Voltage Range**

T_a = −40°C to +85°C; V_{CC} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		0.8	V
Input High Voltage	V_{IH}	All except XTAL1, XTAL2, $\overline{RESET}$	V_{CC} −2		V_{CC}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2	V_{CC} −1		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output High Voltage	V_{OH}	Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; I_{OH} = −100 μA	2.4			V
	V_{OH1}④	Port 1, Port 2; I_{OH} = −5 μA (Type 0)	2.4			V
		Port 1, Port 2; I_{OH} = −50 μA (Type 1)				
	V_{OH2}	All outputs; I_{OH} = −0.2 μA	V_{CC} −0.5			V
Input Current	I_{ILP}④	Port 1, Port 2; $V_{IN} \leqslant V_{IL}$ (Type 0)		−15	−40	μA
		Port 1, Port 2; $V_{IN} \leqslant V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_{IN} \leqslant V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, V_{DD}; $V_{SS} \leqslant V_{IN} \leqslant V_{CC}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqslant V_{IN} \leqslant V_{CC}$			±3	μA
Output Leakage Current	I_{LO}	Bus, T0, High-Impedance State; $V_{SS} \leqslant V_O \leqslant V_{CC}$			±1	μA
Standby Current	I_{CC1}	Halt mode; t_{CY} = 2.5 μs		0.4	0.8	mA
	I_{CC2}	Stop mode②		1	20	μA
Supply Current	I_{CC}	t_{CY} = 2.5 μs		4	8	mA
Data Retention Voltage	V_{CCDR}	Stop mode (V_{DD}, $\overline{RESET}$ ⩽0.4V)	2.0			V

DC CHARACTERISTICS **Extended Voltage Range**

T_a = −40°C to +85°C; V_{CC} = +2.5V to +6V; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		0.18 V_{CC}	V
Input High Voltage (All Except XTAL 1, XTAL 2)	V_{IN}		0.7 V_{CC}		V_{CC}	V
Input High Voltage (XTAL 1, XTAL 2)	V_{IH1}		0,8 V_{CC}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 1.0 mA			0.45	V
Output High Voltage (Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0	V_{OH}	I_{OH} = −100 μA	0.75 V_{CC}			V
Output High Voltage (All other Outputs)	V_{OH1}	Port 1, Port 2; I_{OH} = −1μA (Type 0)	0.7 V_{CC}			V
		Port 1, Port 2; I_{OH} = −10 μA (Type 1)				
Output High Voltage (All Outputs)	V_{OH2}	I_{OH} = −0.2 μA	V_{CC} −0.5			V
Input Leakage Current (Port 1, Port 2)	I_{ILP}	$V_{IN} \leq V_{IL}$ (Type 0)		−15	−40	μA
		$V_{IN} \leq V_{IL}$ (Type 1)			−500	μA
Input Leakage Current ($\overline{SS}$, $\overline{RESET}$)	I_{ILC}	$V_{IN} \leq V_{IL}$			−40	μA
Input Leakage Current (T1, $\overline{INT}$)	I_{IL1}	$V_{SS} < V_{IN} < V_{CC}$			±1	μA
Input Leakage Current (EA)	I_{IL2}	$V_{SS} < V_{IN} < V_{CC}$			±3	μA
Output Leakage Current (Bus, T0 – High Impedance State)	I_{OL}	$V_{SS} < V_O < V_{CC}$			±1	μA
Supply Current	I_{CC}	V_{CC} = 3V, t_{CY} = 10 μs		0.8	1.6	mA
		V_{CC} = 6V, t_{CY} = 2.5 μs		6	12	mA
Halt Mode Standby Current	I_{CC1}	V_{CC} = 3V, t_{CY} = 10 μs		100	200	μA
		V_{CC} = 6V, t_{CY} = 2.5 μs		0.6	1.2	mA
Stop Mode Standby Current	I_{CC2}	V_{CC} = 3V		1	20	μA
		V_{CC} = 6V		1	50	μA

Notes: (1.) Type 0 and type 1 options apply only to the μPD80C48; the μPD80C35 is type 0 only. Input Pin Voltage is V_{IN}, V_{IL}, or V_{IN}, V_{IH}.

(2.) Type 0 is mask version with I_{OH} = −5 μA for each Port Line. Type 1 is mask version with I_{OH} = −50 μA for each Port Line.

4

AC CHARACTERISTICS Read, Write and Instruction Fetch: External Data and Program Memory

T_a = −40°C to +85°C; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} = +5V ± 10%			V_{CC} = +2.5V to 6V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ALE Pulse Width	t_{LL}	①	400			2160			ns
Address Setup before ALE	t_{AL}	①	120			1620			ns
Address Hold from ALE	t_{LA}	①	80			330			ns
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}	①	700			3700			ns
Data Setup before $\overline{WR}$	t_{DW}	①	500			3500			ns
Data Hold after $\overline{WR}$	t_{WD}	②	120			370			ns
Cycle Time	t_{CY}	①	2.5		150	10		150	μs
Data Hold	t_{DR}	①	0		200	0		950	ns
$\overline{PSEN}$, $\overline{RD}$ to Data in	t_{RD}	①			500			2750	ns
Address Setup before $\overline{WR}$	t_{AW}	①	230			3230			ns
Address Setup before Data in	t_{AD}	①			950			5450	ns
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	①	0			500			ns
Control Pulse to ALE	t_{CA}	①	10			10			ns

AC CHARACTERISTICS Port 2 Timing

T_a = −40°C to +85°C; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} = +5V ± 10%			V_{CC} = +2.5V to 6V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Port Control Setup before Falling Edge of PROG	t_{CP}	③	110			860			ns
Port Control Hold after Falling Edge of PROG	t_{PC1}	③, ⑤	0		80	0		200 ④	ns
	t_{PC2}	③, ⑥	460			2400			ns
PROG to Time P2 Input must be Valid	t_{PR}	③			810			5310	ns
Output Data Setup Time	t_{DP}	③	250			3250			ns
Output Data Hold Time	t_{PD}	③	65			820			ns
Input Data Hold Time	t_{PF}	③	0		150	0		900	ns
PROG Pulse Width	t_{PP}	③	1200			6450			ns
Port 2 I/O Data Setup	t_{PL}	③	350			2100			ns
Port 2 I/O Data Hold	t_{LP}	③	150			1400			ns

Notes: ① For Control Outputs: C_L = 80 pF; for Bus Outputs: C_L = 150 pF.
② C_L = 20 pF
③ For Control Outputs: C_L = 80 pF
④ Refer to the operating characteristic curves for Supply Voltage and Port Control Hold.
⑤ t_{CY} = 2.5 μs with V_{CC} = 5V ± 10%
⑥ t_{CY} = 10 μs with V_{CC} = +2.5V to +5.5V

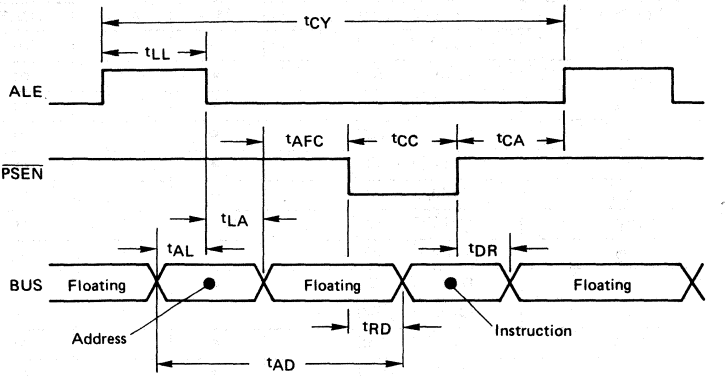
BUS Timing Requirements

SYMBOL	TIMING FORMULA	MIN	MAX	UNIT
t_{LL}	(7/30) T – 170	•		ns
t_{AL}	(1/5) T – 380	•		ns
t_{LA}	(1/30) T	•		ns
t_{CC}	(2/5) T – 300	•		ns
t_{DW}	(2/5) T – 500	•		ns
t_{WD}	(1/30) T + 40	•		ns
t_{DR}	(1/10) T – 50		•	ns
t_{RD}	(3/10) T – 250		•	ns
t_{AW}	(2/5) T – 770	•		ns
t_{AD}	(3/5) T – 550		•	ns
t_{AFC}	(1/15) T – 165	•		ns
t_{CP}	(1/10) T – 140	•		ns
t_{PR}	(3/5) T – 690		•	ns
t_{PF}	(1/10) T – 100		•	ns
t_{DP}	(2/5) T – 750	•		ns
t_{PD}	(1/10) T – 180	•		ns
t_{PP}	(7/10) T – 550	•		ns
t_{PL}	(7/30) T – 230	•		ns
t_{LP}	(1/6) T – 265	•		ns

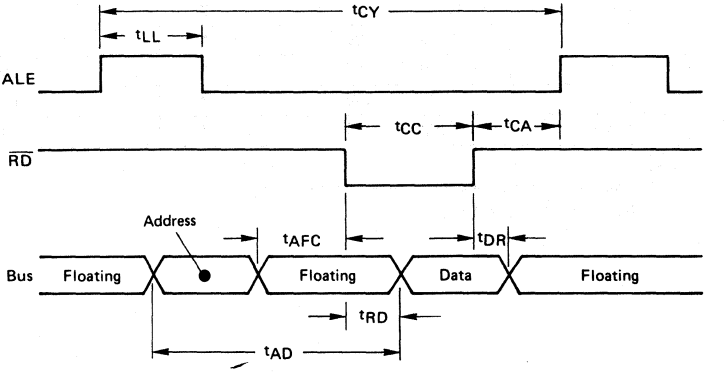
Notes: T = t_{CY}
Unlisted parameters are not affected by cycle time
$t_{CY} = (1/f_{XTAL}) \times 15$

4

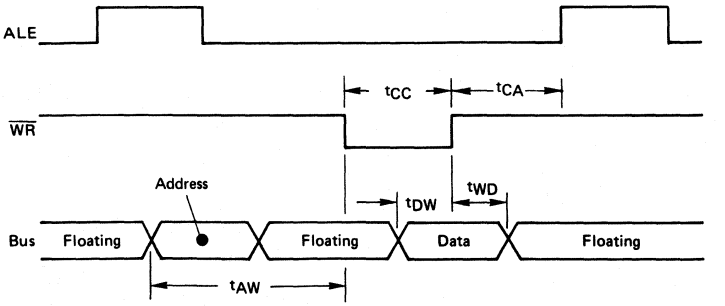
Instruction Fetch from External Memory



Read from External Data Memory

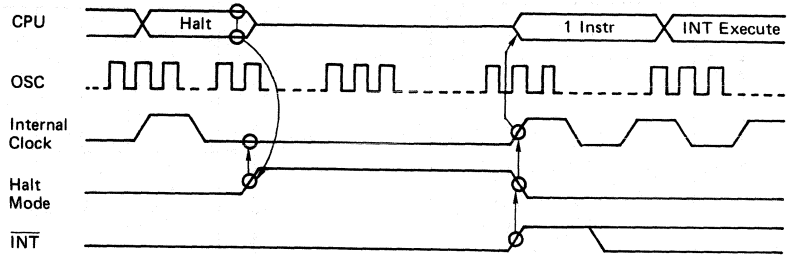


Write to External Memory

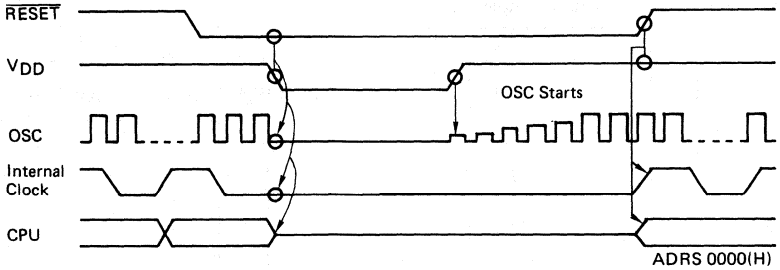


Low Power Standby Operation

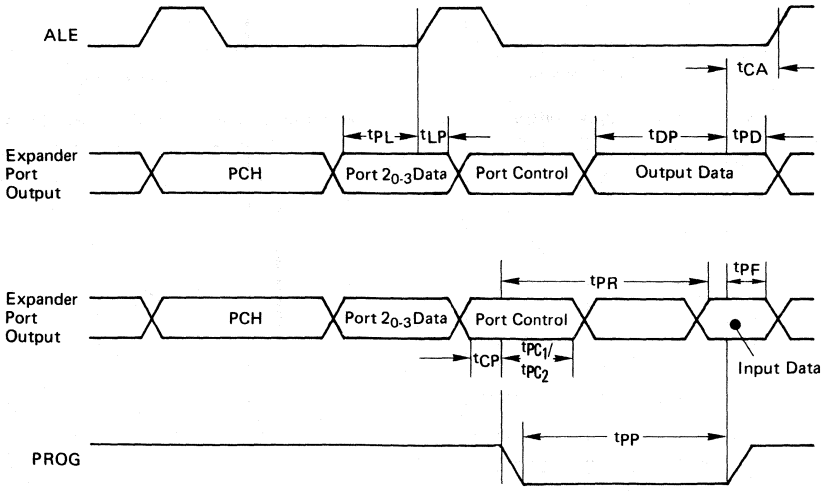
1) Halt Mode (When EI)



2) Stop Mode



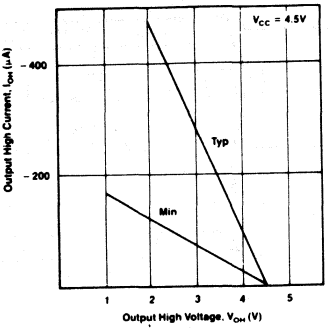
Port 2 Timing



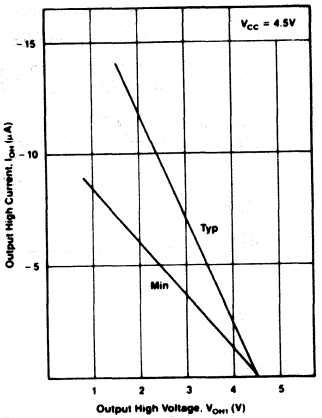
4

OPERATING CHARACTERISTIC CURVES

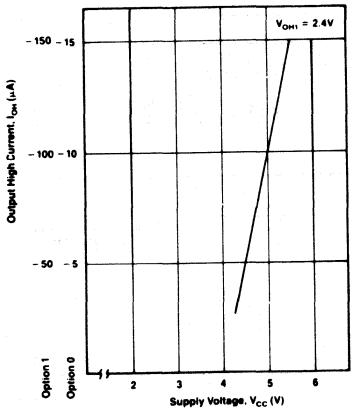
Output High Current vs. Output High Voltage



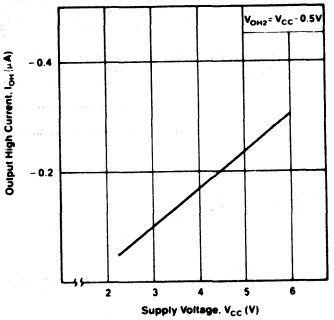
Output High Current vs. Output High Voltage



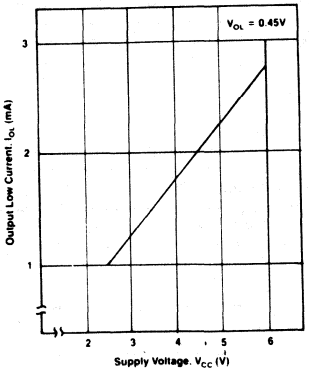
Output High Current vs. Supply Voltage



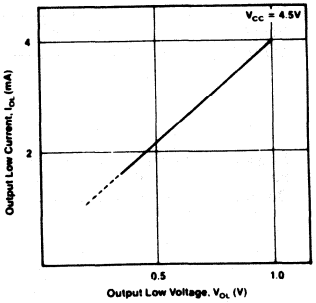
Output High Current vs. Supply Voltage



Output Low Current vs. Supply Voltage

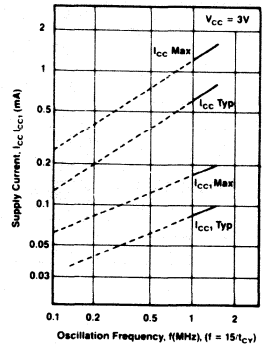


Output Low Current vs. Output Low Voltage

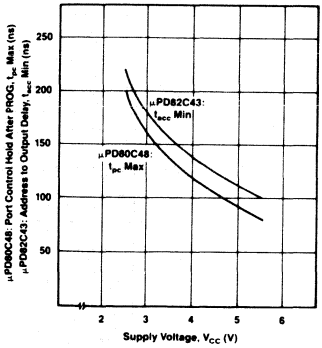


OPERATING CHARACTERISTIC CURVES (Cont.)

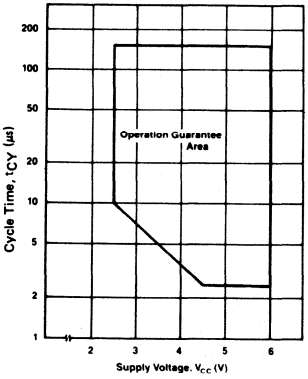
Supply Current vs. Oscillation Frequency



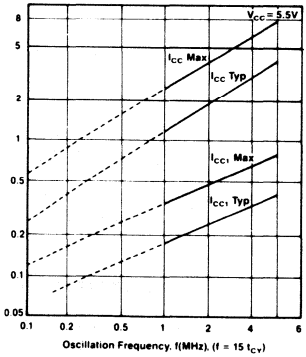
Port Control Hold After PROG, t_{pc} Max (μPD80C48), and Address to Output Delay, t_{acc} Min (μPD82C43), vs. Supply Voltage



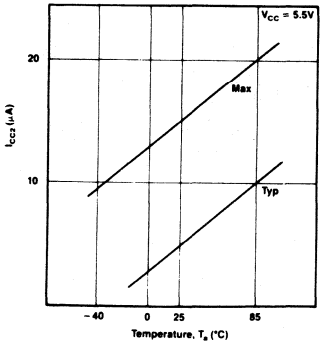
Cycle Time vs. Supply Voltage



Supply Current vs. Oscillation Frequency ①



Current Consumption as a Function of Temperature — Stop Mode



Note: ① External oscillation is assumed for frequency less than 1 MHz. Internal oscillation requires more power.

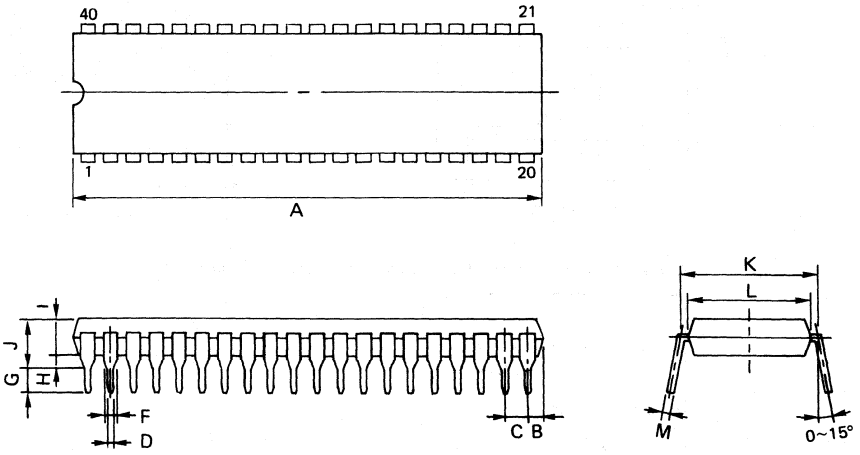
4

PACKAGE DIMENSIONS
μPD80C35C/C48C
40 PIN PLASTIC DIP

ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T. P.)	0.100 (T. P.)
D	0.50 ± 0.10	0.020 $^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6 ± 0.3	0.142 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T. P.)	0.600 (T. P.)
L	13.2	0.520
M	0.25 $^{+0.10}_{-0.05}$	0.010 $^{+0.004}_{-0.003}$
N	0.25	0.01

Notes: 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T. P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.



CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

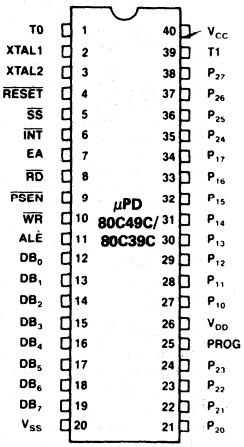
The NEC μPD80C49 is a true stand-alone 8-bit microcomputer fabricated using CMOS technology. All of the functional blocks necessary for an integrated microcomputer are incorporated, including a 2K-byte ROM, a 128-byte RAM, 27 I/O lines, an 8-bit timer/event counter, and a clock generator. This integrated capability permits use in stand-alone applications. For designs requiring extra capability, the μPD80C49 can be expanded using peripherals and memory compatible with industry-standard 8080A/8085A processors. A version of the μPD80C48 without ROM is offered by the μPD80C39.

Providing compatibility with industry-standard 8049, 8749, and 8039 processors, the μPD80C49 features significant savings in power consumption. In addition to the power savings gained through CMOS technology, the μPD80C49 is distinct in offering two standby modes (Halt mode and Stop mode) to further minimize power drain.

FEATURES

- 8-bit CPU with ROM, RAM, and I/O on a single chip
- Hardware/software-compatible with industry-standard 8049, 8749, and 8039 processors
- 2K x 8 ROM
- 128 x 8 RAM
- 27 I/O lines
- 1.875 μs cycle time (8 MHz crystal)
- All instructions executable in 1 or 2 cycles
- 97 instructions: 70 percent are single-byte instructions
- Internal timer/event counter
- 2 interrupts (an external interrupt and a timer interrupt)
- Easily expandable memory and I/O
- Bus compatible with 8080A/8085A peripherals
- Power-efficient CMOS technology requiring a single +2.5V to +6V power supply
- Available in 40-pin DIP, 44-pin flat pack (80C49 only), and 52-pin flat pack
- Halt mode
  - 1 mA typical supply current
  - Maintenance of internal logic values and control states
  - Mode initialization via HALT instruction
  - Mode release via external interrupt or reset
- Stop mode
  - 1 μA typical supply current
  - Disabling of internal clock generation and internal logic
  - Maintenance of RAM contents
  - Mode initialization via hardware (V_{DD})
  - Mode release via reset

PIN CONFIGURATION μPD80C49C/μPD80C39C (40 PIN PLASTIC DIP)



4

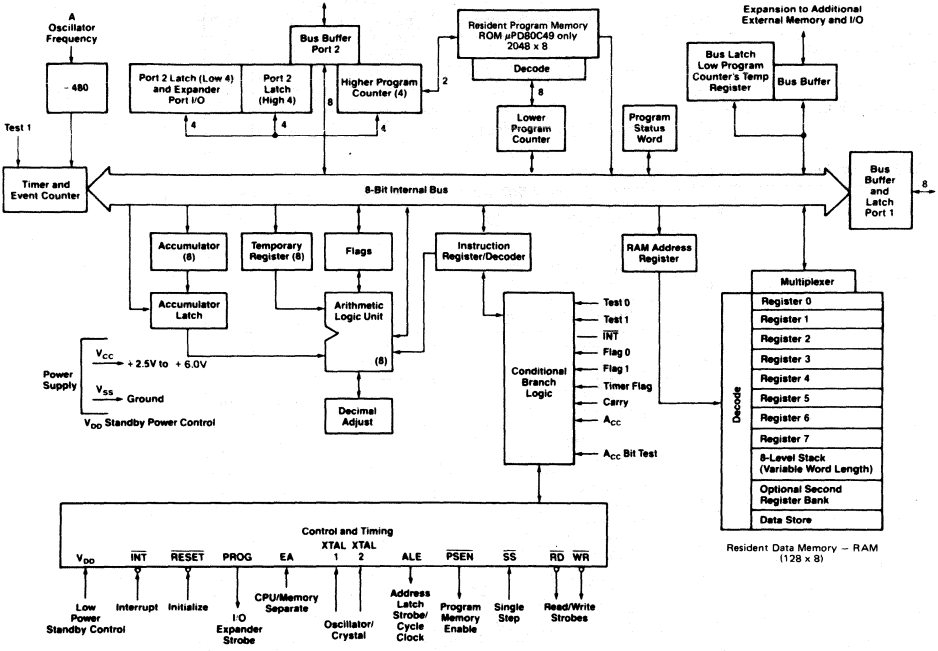
PIN IDENTIFICATION

A.
μPD80C49C/μPD80C39C
(40 PIN PLASTIC DIP)

PIN A.	SYMBOL	NAME	FUNCTION
1	T0	Test 0	Testable input using conditional jump instructions JT0 and JNT0. Also enables clock output via the ENT0 CLK instruction.
2	XTAL1	Crystal 1	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. May also be used as an input for external clock signals. (Non-TTL-compatible V_{IH}.)
3	XTAL2	Crystal 2	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. (Non-TTL-compatible V_{IH}.)
4	$\overline{RESET}$	Reset	Active-low input line that initializes the processor. Also used to release both the Halt and Stop modes. ①
5	$\overline{SS}$	Single Step	Active-low input line, that, in conjunction with ALE, causes the processor to single-step through a program one instruction at a time.
6	$\overline{INT}$	Interrupt	Active-low input line that causes an interrupt if an enable instruction has been executed. A reset disables the interrupt. May be used as a testable input with a conditional jump instruction. Can also be used to release the Halt mode.
7	EA	External Access	Input line that inhibits internal program memory fetches and initiates access of external program memory. Essential for system testing and may also be used for program debugging.
8	$\overline{RD}$	Read	Active-low output strobe line that is used to read data from external data memory.
9	$\overline{PSEN}$	Program Store Enable	Active-low output line that is used to fetch instructions from external program memory.
10	$\overline{WR}$	Write	Active-low output strobe line that is used to write data into external data memory.
11	ALE	Address Latch Enable	Output line for address latch enable. At the falling edge of ALE, the address of either external data memory or external program memory is available on the bus.
12-19	DB_0-DB_7	Bus	These I/O lines constitute an 8-bit bidirectional data/address bus. Synchronous read and write operations can be performed on this bus using $\overline{RD}$ and $\overline{WR}$ signals. Data driven out on the bus by an OUTL BUS instruction is statically latched. The address of external memory is available on the bus at the falling edge of ALE when reading from external program memory or writing to and reading from external data memory. During external program memory fetches, the least-significant 8 bits of the external program memory address are driven out on the bus and the addressed instruction is fetched using $\overline{PSEN}$. When no external memory is used, the bus can serve as a true bidirectional 8-bit port. Information is strobed in or out by the $\overline{RD}$ and $\overline{WR}$ signals.
20	V_{SS}	Ground	Ground potential.
21-24, 35-38	P_{20}-P_{27}	Port 2	These lines constitute Port 2, an 8-bit quasi-bidirectional port. During external program memory fetches P_{20}-P_{23} output the most-significant 4 bits of the external program memory address. Lines P_{20}-P_{23} can also be used as a 4-bit I/O expander bus to interface with the optional μPD82C43 I/O expander.
25	PROG	Program Pulse	This line is used as an output strobe when interfacing with the optional μPD82C43 I/O expander.
26	V_{DD}	Oscillator Control Voltage Line	This input line is used to control oscillator stopping and restarting in Stop mode. Stop mode is enabled by forcing V_{DD} Low during a reset.
27-34	P_{10}-P_{17}	Port 1	These lines constitute Port 1, an 8-bit, generalpurpose quasi-bidirectional port.
39	T1	Test 1	Testable input using conditional jump instructions JT1 and JNT1. Can also be used as the timer/counter input line via the STRT CNT instruction.
40	V_{CC}	Primary Power Supply	Power supply. V_{CC} must be between +2.5V to +6V for normal operation. In Stop mode, V_{CC} must be at least +2V to ensure data retention.

Note: ①The pulse width of $\overline{RESET}$ must be a minimum of 5 machine cycles in length following oscillator stabilization to reinitialize the processor and stabilize CPU operation. At power-up, the states of the output lines are undefined until completion of reset.

BLOCK DIAGRAM



4

ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature, T_{opt}	−40°C to +85°C
Storage Temperature (Plastic Package), T_{stg}	−65°C to +150°C
Voltage on Any Pin, $V_{I/O}$	V_{SS} −0.3V to V_{CC} +0.3V
Supply Voltage, V_{CC}	V_{SS} −0.3 to +10V
Power Dissipation, P_D with I_{CC} = max. 8 mA and V_{CC} = 5V nominal P_D = 40 mW	40 mW

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS **Standard Voltage Range**

T_a = −40°C to +85°C; V_{CC} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		0.8	V
Input High Voltage	V_{IH}	All except XTAL1, XTAL2, $\overline{RESET}$	V_{CC} −2		V_{CC}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2	V_{CC} −1		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output High Voltage	V_{OH}	Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; I_{OH} = −100 μA	2.4			V
	V_{OH1}①	Port 1, Port 2; I_{OH} = −5 μA (Type 0)	2.4			V
		Port 1, Port 2; I_{OH} = −50 μA (Type 1)				
	V_{OH2}	All outputs; I_{OH} = −0.2 μA	V_{CC} −0.5			V
Input Current	I_{ILP}①	Port 1, Port 2; $V_{IN} \leqslant V_{IL}$ (Type 0)		−15	−40	μA
		Port 1, Port 2; $V_{IN} \leqslant V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_{IN} \leqslant V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, V_{DD}; $V_{SS} \leqslant V_{IN} \leqslant V_{CC}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqslant V_{IN} \leqslant V_{CC}$			±3	μA
Output Leakage Current	I_{LO}	Bus, T0, High-Impedance State; $V_{SS} \leqslant V_O \leqslant V_{CC}$			±1	μA
Standby current	I_{CC1}	Halt mode; t_{CY} = 2.5 μs		0.4	0.8	mA
	I_{CC1}	Halt mode; t_{CY} = 1.875 μs		0.5	1.0	mA
	I_{CC2}	Stop mode ②		1	20	μA
Supply Current	I_{CC}	t_{CY} = 2.5 μs		5	10	mA
	I_{CC}	t_{CY} = 1.875 μs		6	12	mA
Data Retention Voltage	V_{CCDR}	Stop mode (V_{DD}, $\overline{RESET}$ ⩽ 0.4V)	2.0			V

DC CHARACTERISTICS **Extended Voltage Range**

T_a = −40°C to +85°C; V_{CC} = +2.5V to 6.0V; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		0.18 V_{CC}	V
Input High Voltage (All Except XTAL 1, XTAL 2)	V_{IN}		0.7 V_{CC}		V_{CC}	V
Input High Voltage (XTAL 1, XTAL 2)	V_{IH1}		0.8 V_{CC}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 1.0 mA			0.45	V
Output High Voltage (Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0	V_{OH}	I_{OH} = −100 μA	0.75 V_{CC}			V
Output High Voltage (All other Outputs)	V_{OH1}	Port 1, Port 2; I_{OH} = −1 μA (Type 0)	0.7 V_{CC}			V
		Port 1, Port 2: I_{OH} = −10 μA (Type 1)				
Input Leakage Current (Port 1, Port 2)	I_{ILP}	$V_{IN} \leq V_{IL}$ (Type 0)		−15	−40	μA
		$V_{IN} \leq V_{IL}$ (Type 1)			−500	μA
Input Leakage Current ($\overline{SS}$, $\overline{RESET}$)	I_{ILC}	$V_{IN} \leq V_{IL}$			−40	μA
Input Leakage Current (T1, $\overline{INT}$)	I_{IL1}	$V_{SS} < V_{IN} < V_{CC}$			±1	μA
Input Leakage Current (EA)	I_{IL2}	$V_{SS} < V_{IN} < V_{CC}$			±5	μA
Output Leakage Current (Bus, T0 – High Impedance State)	I_{OL}	$V_{SS} < V_O < V_{CC}$			±1	μA
Supply Current	I_{CC}	V_{CC} = 3V, t_{CY} = 10 μs		0.8	1.6	mA
		V_{CC} = 6V, t_{CY} = 2.5 μs		8	15	mA
		V_{CC} = 6V, t_{CY} = 1.875 μs		10	20	mA
Halt Mode Standby Current	I_{CC1}	V_{CC} = 3V, t_{CY} = 10μs		100	200	μA
		V_{CC} = 6V, t_{CY} = 2.5 μs		0.6	1.2	mA
		V_{CC} = 6V, t_{CY} = 1.875 μs		0.7	1.4	mA
Stop Mode Standby Current	I_{CC2}	V_{CC} = 3V		1	20	μA
		V_{CC} = 6V		1	50	μA

Notes: (1.) Type 0 and type 1 options apply only to the μPD80C49; the μPD80C39 is type 0 only. Input Pin Voltage is V_{IN}, V_{IL}, or V_{IN}, V_{IH}.

(2.) Type 0 is mask version with I_{OH} = −5 μA for each Port Line. Type 1 is mask version with I_{OH} = −50 μA for each Port Line.

4

AC CHARACTERISTICS Read, Write and Instruction Fetch: External Data and Program Memory

T_a = −40°C to +85°C; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} = +5V ± 10%			V_{CC} = +2.5V to 6V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ALE Pulse Width	t_{LL}		270			2160			ns
Address Setup before ALE	t_{AL}		90			1620			ns
Address Hold from ALE	t_{LA}	①	60			330			ns
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}		450			3700			ns
Data Setup before $\overline{WR}$	t_{DW}		250			3500			ns
Data Hold after $\overline{WR}$	t_{WD}	②	100			370			ns
Cycle Time	t_{CY}		1.875		150	10		150	μs
Data Hold	t_{DR}		0		130	0		950	ns
$\overline{PSEN}$, $\overline{RD}$ to Data in	t_{RD}				310			2750	ns
Address Setup before $\overline{WR}$	t_{AW}	①	150			3230			ns
Address Setup before Data in	t_{AD}				575			5450	ns
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}		0			500			ns
Control Pulse to ALE	t_{CA}		10			10			ns

AC CHARACTERISTICS Port 2 Timing

T_a = −40°C to +85°C; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} = +5V ± 10%			V_{CC} = +2.5V to 6V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Port Control Setup before Falling Edge of PROG	t_{CP}	③	110			860			ns
Port Control Hold after Falling Edge of PROG	t_{PC1}	③, ⑤	0		80	0		200 ⑤	ns
	t_{PC2}	③, ⑥	300			2400			ns
PROG to Time P2 Input must be Valid	t_{PR}				650			5310	ns
Output Data Setup Time	t_{DP}	③	200			3250			ns
Output Data Hold Time	t_{PD}		20			820			ns
Input Data Hold Time	t_{PF}		0		85	0		900	ns
PROG Pulse Width	t_{PP}		760			6450			ns
Port 2 I/O Data Setup	t_{PL}		205			2100			ns
Port 2 I/O Data Hold	t_{LP}		45			1400			ns

Notes: ① For Control Outputs: C_L = 80 pF; for Bus Outputs: C_L = 150 pF.
② C_L = 20 pF
③ For Control Outputs: C_L = 80 pF
④ Refer to the operating characteristic curves for Supply Voltage and Port Control Hold.
⑤ t_{CY} = 2.5 μs with V_{CC} = 5V ± 10%
⑥ t_{CY} = 10 μs with V_{CC} = +2.5V to +5.5V

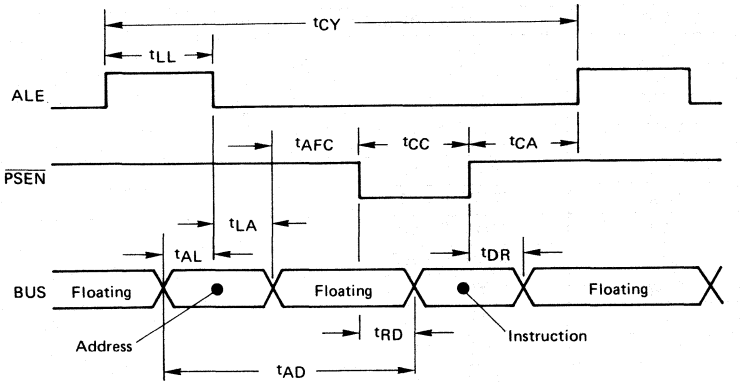
BUS Timing Requirements

SYMBOL	TIMING FORMULA	MIN	MAX	UNIT
t_{LL}	(7/30) T – 167	•		ns
t_{AL}	(1/5) T – 285	•		ns
t_{LA}	(1/30) T	•		ns
t_{CC}	(2/5) T – 300	•		ns
t_{DW}	(2/5) T – 500	•		ns
t_{WD}	(1/30) T + 40	•		ns
t_{DR}	(1/10) T – 50		•	ns
t_{RD}	(3/10) T – 250		•	ns
t_{AW}	(2/5) T – 600	•		ns
t_{AD}	(3/5) T – 550		•	ns
t_{AFC}	(1/15) T – 125	•		ns
t_{CP}	(1/10) T – 87	•		ns
t_{PR}	(3/5) T – 475		•	ns
t_{PF}	(1/10) T – 100		•	ns
t_{DP}	(2/5) T – 550	•		ns
t_{PD}	(1/10) T – 167	•		ns
t_{PP}	(7/10) T – 550	•		ns
t_{PL}	(7/30) T – 230	•		ns
t_{LP}	(1/6) T – 265	•		ns

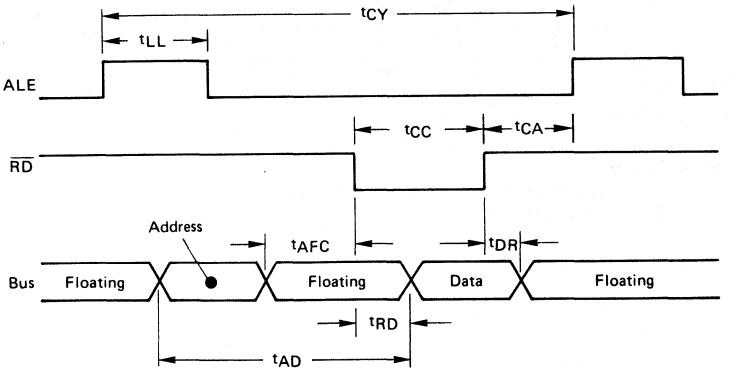
Notes: $T = t_{CY}$
Unlisted parameters are not affected by cycle time
$t_{CY} = (1/f_{XTAL}) \times 15$

4

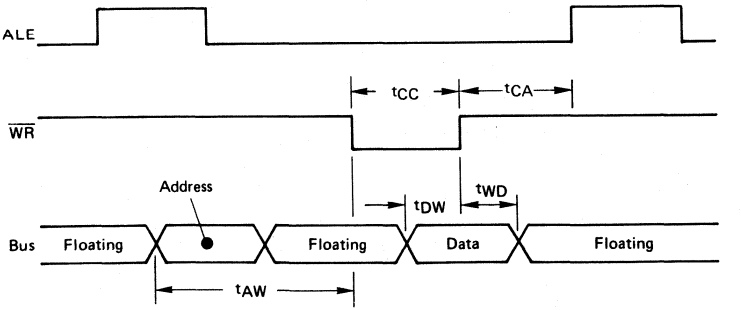
Instruction Fetch from External Memory



Read from External Data Memory

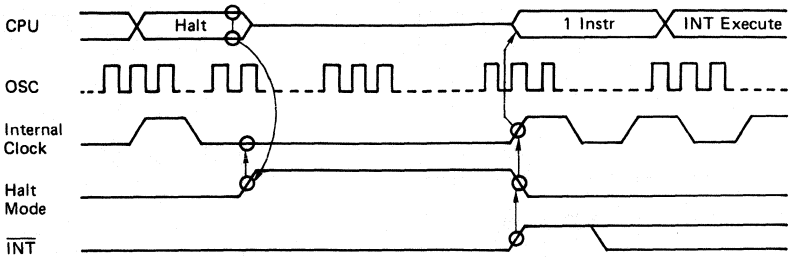


Write to External Memory

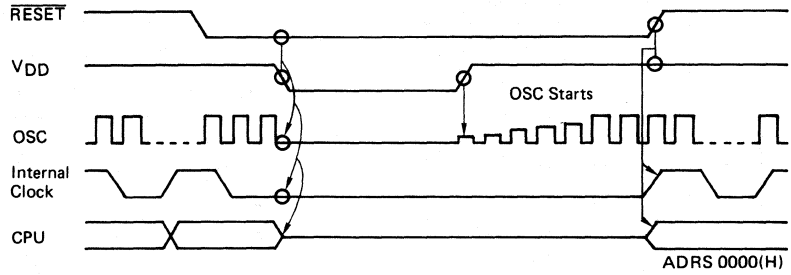


Low Power Standby Operation

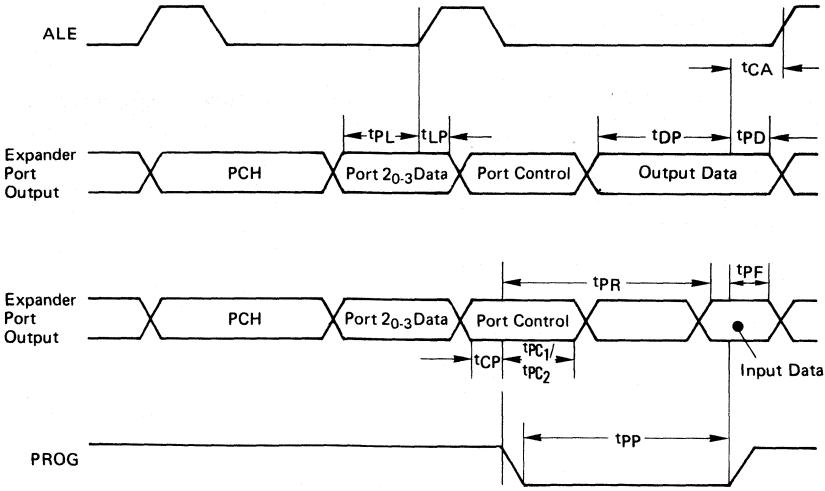
1) Halt Mode (When EI)



2) Stop Mode

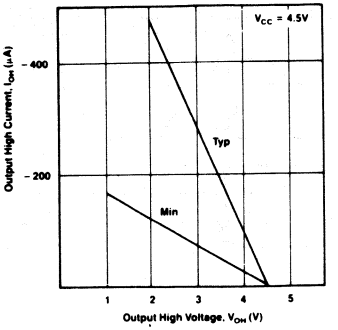


Port 2 Timing

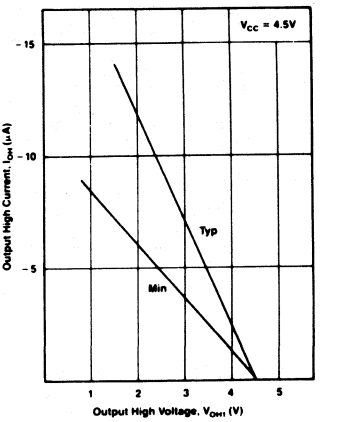


OPERATING CHARACTERISTIC CURVES

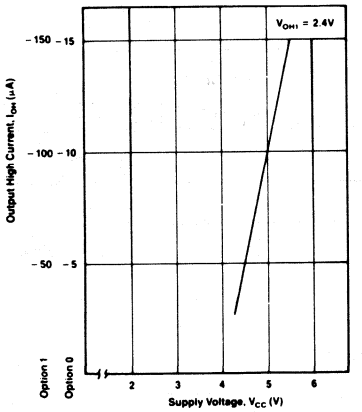
Output High Current vs. Output High Voltage



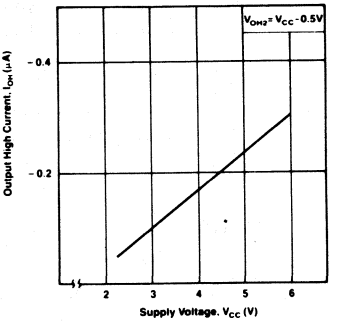
Output High Current vs. Output High Voltage



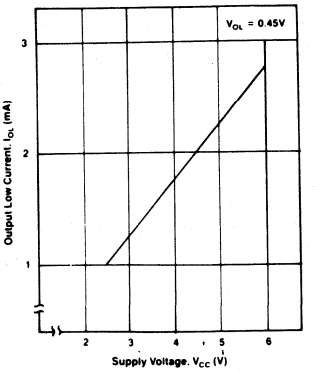
Output High Current vs. Supply Voltage



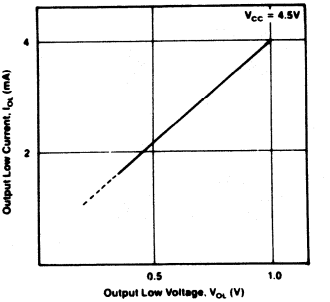
Output High Current vs. Supply Voltage



Output Low Current vs. Supply Voltage

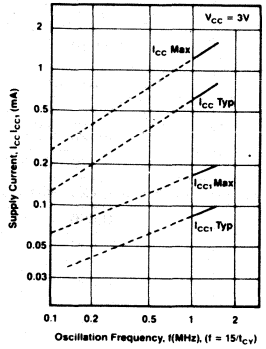


Output Low Current vs. Output Low Voltage

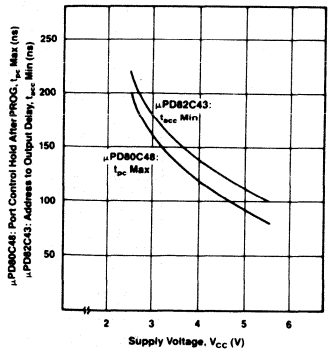


OPERATING CHARACTERISTIC CURVES (Cont.)

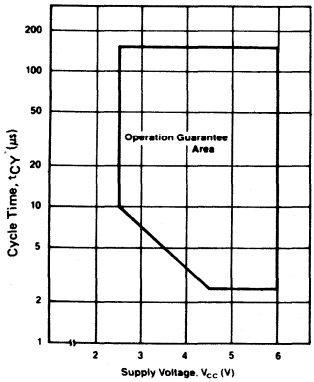
Supply Current vs. Oscillation Frequency



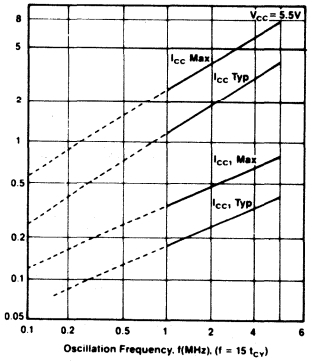
Port Control Hold After PROG, t_{pc} Max (μPD80C48), and Address to Output Delay, t_{acc} Min (μPD82C43), vs. Supply Voltage



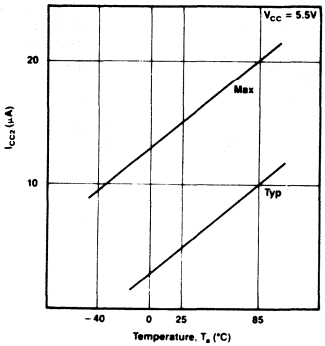
Cycle Time vs. Supply Voltage



Supply Current vs. Oscillation Frequency ①



Current Consumption as a Function of Temperature — Stop Mode



Note: ① External oscillation is assumed for frequency less than 1 MHz. Internal oscillation requires more power.

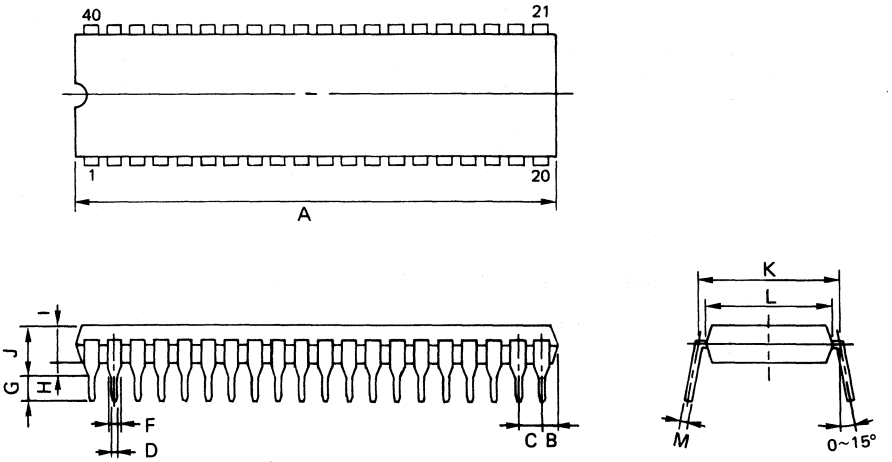
4

PACKAGE DIMENSIONS
μPD80C49C/C39C
40 PIN PLASTIC

ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T. P.)	0.100 (T. P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6 ± 0.3	0.142 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T. P.)	0.600 (T. P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01

Notes: 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T. P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.



CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

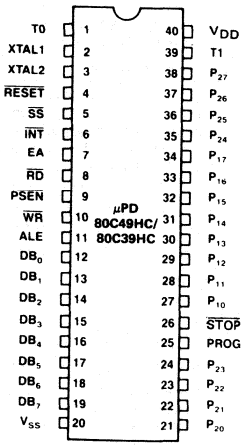
The NEC μPD80C49H is a true stand-alone 8-bit microcomputer fabricated using CMOS technology. All of the functional blocks necessary for an integrated microcomputer are incorporated, including a 2K-byte ROM, a 128-byte RAM, 27 I/O lines, an 8-bit timer/event counter, and a clock generator. This integrated capability permits use in stand-alone applications. For designs requiring extra capability, the μPD80C49H can be expanded using peripherals and memory compatible with industry-standard 8080A/8085A processors. A version of the μPD80C49H without ROM is offered by the μPD80C39H.

Providing compatibility with industry-standard 8049, 8749, and 8039 processors, the μPD80C49H features significant savings in power consumption. In addition to the power savings gained through CMOS technology, the μPD80C49H is distinct in offering two standby modes (HALT mode and STOP mode) to further minimize power drain.

FEATURES

- 8-bit CPU with ROM, RAM, and I/O on a single chip
- Hardware/software-compatible with industry-standard 8049, 8749, and 8039 processors
- 2K x 8 ROM
- 128 x 8 RAM
- 27 I/O lines
- 1.25 μs cycle time (12 MHz crystal)
- All instructions executable in 1 or 2 cycles
- 97 instructions: 70 percent are single-byte instructions
- Internal timer/event counter
- 2 interrupts (an external interrupt and a timer interrupt)
- Easily expandable memory and I/O
- Bus compatible with 8080A/8085A peripherals
- Power-efficient CMOS technology requiring a single +2.5V to 6V power supply
- Available in 40-pin DIP, 44-pin flat pack (80C49H only)
- Halt mode
  - 1 mA typical supply current
  - Maintenance of internal logic values and control states
  - Mode initialization via HALT instruction
  - Mode release via external interrupt or reset
- Stop mode
  - 1 μA typical supply current
  - Disabling of internal clock generation and internal logic
  - Maintenance of RAM contents
  - Mode initialization via hardware ($\overline{STOP}$)
  - Mode release via reset

PIN CONFIGURATION μPD80C49HC/ μPD80C39HC (40 PIN PLASTIC DIP)



4

PIN IDENTIFICATION

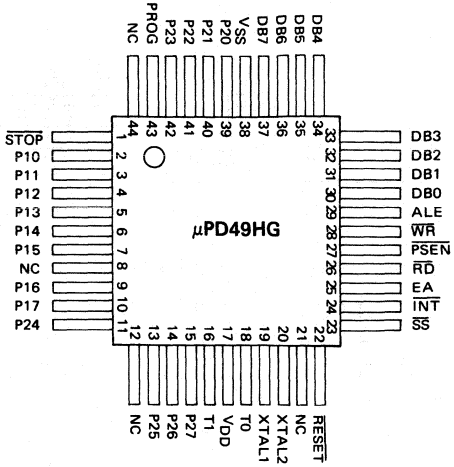
A.
μPD80C49HC/
μPD80C39HC
(40 PIN PLASTIC DIP)

B.
μPD49HG
(44 PIN PLASTIC
FLAT PACK)

PIN				FUNCTION
B.	A.	SYMBOL	NAME	
18	1	T0	Test 0	Testable input using conditional jump instructions JT0 and JNT0. Also enables clock output via the ENT0 CLK instruction.
19	2	XTAL1	Crystal 1	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. May also be used as an input for external clock signals. (Non-TTL-compatible V_{IH}.)
20	3	XTAL2	Crystal 2	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. (Non-TTL-compatible V_{IH}.)
22	4	$\overline{RESET}$	Reset	Active-low input line that initializes the processor. Also used to release both the Halt and Stop modes. ①
23	5	$\overline{SS}$	Single Step	Active-low input line, that, in conjunction with ALE, causes the processor to single-step through a program one instruction at a time.
24	6	$\overline{INT}$	Interrupt	Active-low input line that causes an interrupt if an enable instruction has been executed. A reset disables the interrupt. May be used as a testable input with a conditional jump instruction. Can also be used to release the Halt mode.
25	7	EA	External	Input line that inhibits internal program memory fetches and initiates access of external program memory. Essential for system testing and may also be used for program debugging.
26	8	$\overline{RD}$	Read	Active-low output strobe line that is used to read data from external data memory.
27	9	$\overline{PSEN}$	Program Store Enable	Active-low output line that is used to fetch instructions from external program memory.
28	10	$\overline{WR}$	Write	Active-low output strobe line that is used to write data into external data memory.
29	11	ALE	Address Latch Enable	Output line for address latch enable. At the falling edge of ALE, the address of either external data memory or external program memory is available on the bus.
30-37	12-19	DB_0-DB_7	Bus	These I/O lines constitute an 8-bit bidirectional data/address bus. Synchronous read and write operations can be performed on this bus using $\overline{RD}$ and $\overline{WR}$ signals. Data driven out on the bus by an OUTL BUS instruction is statically latched. The address of external memory is available on the bus at the falling edge of ALE when reading from external program memory or writing to and reading from external data memory. During external program memory fetches, the least-significant 8 bits of the external program memory address are driven out on the bus and the addressed instruction is fetched using $\overline{PSEN}$. When no external memory is used, the bus can serve as a true bidirectional 8-bit port. Information is strobed in or out by the $\overline{RD}$ and $\overline{WR}$ signals.
38	20	V_{SS}	Ground	Ground potential.
39-42, 11, 13-15	21-24, 35-38	P_{20}-P_{27}	Port 2	These lines constitute Port 2, an 8-bit quasi-bidirectional port. During external program memory fetches P_{20}-P_{23} output the most-significant 4 bits of the external program memory address. Lines P_{20}-P_{23} can also be used as a 4-bit I/O expander bus to interface with the optional μPD82C43 I/O expander.
43	25	PROG	Program Pulse	This line is used as an output strobe when interfacing with the optional μPD82C43 I/O expander.
1	26	$\overline{STOP}$	Stop	Used to control the hardware STOP mode.
2- 7, 9-10	27-34	P_{10}-P_{17}	Port 1	These lines constitute Port 1, an 8-bit, generalpurpose quasi-bidirectional port.
16	39	T1	Test 1	Testable input using conditional jump instructions JT1 and JNT1. Can also be used as the timer/counter input line via the STRT CNT instruction.
17	40	V_{DD}	Primary Power Supply	Power supply. V_{CC} must be between +2.5V to +6V for normal operation. In Stop mode, V_{CC} must be at least +2V to ensure data retention.

Note: ① The pulse width of RESET must be a minimum of 5 machine cycles in length following oscillator stabilization to reinitialize the processor and stabilize CPU operation. At power-up, the states of the output lines are undefined until completion of reset.

PIN CONFIGURATION
μPD49HG
(44 PIN FLAT PACKAGE)

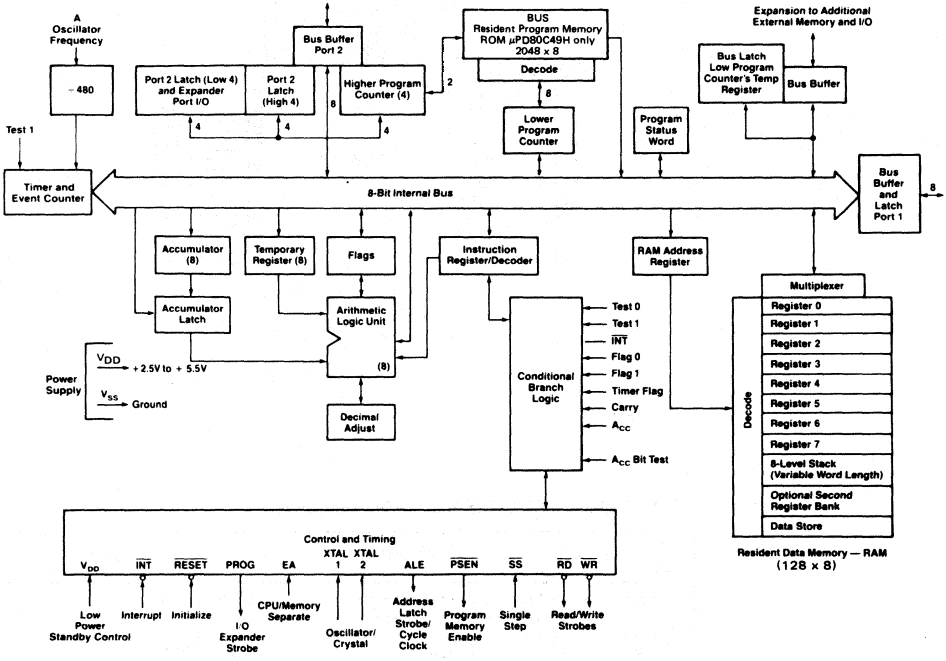


DIFFERENCES BETWEEN μPD49H and μPD49

Item \ Type	μPD49H	μPD49
Instruction set	98 instructions (including an additional STOP instruction)	97 instructions
Instruction cycle	1.25 μs/12 MHz	1.875 μs/8 MHz
Standby facility	Three modes; HALT, hardware STOP and software STOP	Two modes; HALT and STOP
	Stops inactive in the same timing in all of the HALT, hardware STOP, and software STOP modes, regardless of control signals executing internal ROM or external ROM (with ALE being high level).	Stops in different timings between the HALT and STOP modes.
Port option (pull-up resistance)	• Type 0 (I_{OH} = −5 μA: V_{DD} = 5V ± 10%) • Type 1 (I_{OH} = −50 μA: V_{DD} = 5V ± 10%) • Type 2 (without pull-up resistance)	− Type 0 (I_{OH} = −5 μA: V_{DD} = 5V ± 10%) − Type 1 (I_{OH} = −50 μA: V_{DD} = 5V ± 10%)

4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature, T_{opt}	−40°C to +85°C
Storage Temperature (Plastic Package), T_{stg}	−65°C to +150°C
Voltage on Any Pin, $V_{I/O}$	V_{SS} −0.3V to V_{DD} +0.3V
Supply Voltage, V_{DD}	V_{SS} −0.3 to +7V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS T_a = −40 to +85°C, V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		0.8	V
Input High Voltage	V_{IH}	(All except XTAL1, XTAL2, $\overline{RESET}$ $\overline{SS}$)	V_{DD} −2		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$	V_{DD} −1		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output High Voltage	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; I_{OH} = −400 μA	2.4			V
	V_{OH1} ③	PORT1, PORT2; I_{OH} = −5 μA (Type 0)	2.4			V
	V_{OH1} ③	PORT1, PORT2; I_{OH} = 50 μA (Type 1)	2.4			V
	V_{OH2}	All outputs; I_{OH} = −0.2 μA	V_{DD} −0.5			V
Input Current	I_{ILP} ③	PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 0)		−15	−40	μA
		PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqslant V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±3	μA
Output Leakage Current	I_{LO}	BUS, T0, High impedance state (2) $V_{SS} \leqslant V_O \leqslant V_{DD}$			±1	μA
Standby Current	I_{DD1}	HALT mode; t_{CY} = 1.25 μs		1.5	3.0	mA
	I_{DD2}	STOP mode (1)		1	20	μA
Supply Current	I_{DD}	t_{CY} = 1.25 μs		6	15	mA
Data Holding Voltage	V_{DDDR}	Hardware STOP mode ($\overline{STOP}$, $\overline{RESET} \leqslant$0.4V) or reset ($\overline{RESET} \leqslant$0.4V)	2.0			V

Notes:

(1) Input pin voltage $V_I \leqslant V_{IL}$ or $V_I \geqslant V_{IH}$.

(2) Includes PORT1 and PORT2 pins optionally specified with type 2.

(3) Type 0 and Type 1 options apply only to the μPD80C49H; the μPD80C39H is type 0 only.

4

DC CHARACTERISTICS T_a = −40 to +85°C, V_{DD} = +2.5V to +6.0V, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		0.18 V_{DD}	V
Input High Voltage	V_{IH}	(All except XTAL1, XTAL2, $\overline{RESET}$, $\overline{SS}$)	0.7 V_{DD}		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$	0.8 V_{DD}		V_{DD}	V
Input Low Voltage	V_{OL}	I_{OL} = 1.0 mA			0.45	V
Output High Voltage	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; I_{OH} = −100 μA	0.75 V_{DD}			V
	V_{OH1} ③	PORT1, PORT2; I_{OH} = −1 μA (Type 0)	0.7 V_{DD}			V
		PORT1, PORT2; I_{OH} = −10 μA (Type 1)	0.7 V_{DD}			V
Input Current	I_{ILP} ③	PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 0)		−15	−40	μA
		PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqslant V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±5	μA
Output Leakage Current	I_{LO}	BUS, T0, High impedance state (2) $V_{SS} \leqslant V_O \leqslant V_{DD}$			±1	μA
Standby Current	I_{DD1}	HALT mode: V_{DD} = 3V; t_{CY} = 5 μs		0.3	0.6	mA
		HALT mode: V_{DD} = 6V; t_{CY} = 1.25 μs		2.0	4.0	mA
	I_{DD2}	STOP mode (1): V_{DD} = 3V		1	20	μA
		STOP mode (1): V_{DD} = 6V		1	50	μA
Supply Current	I_{DD}	V_{DD} = 3V; t_{CY} = 5 μs		2.0	4.0	mA
		V_{DD} = 6V; t_{CY} = 1.25 μs		10	20	mA

Notes:

(1) Input pin voltage $V_I \leqslant V_{IL}$ or $V_I \geqslant V_{IH}$.

(2) Includes PORT1 and PORT2 pins optionally specified with type 2.

(3) Type 0 and Type 1 options apply only to the μPD80C49H; the μPD80C39H is type 0 only.

AC CHARACTERISTICS

T_a = −40 to +85°C, V_{SS} = 0V

PARAMETER	SYMBOL	CONDITION	V_{DD} = +5V ±10%			V_{DD} = +2.5 to +6.0V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Cycle Time	t_{CY}		1.25		150	5		150	μs
ALE Pulse Width	t_{LL}	③	125			995			ns
Address Setup to ALE	t_{AL}		140			890			ns
Address Hold from ALE	t_{LA}		45			295			ns
Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}		425			2300			ns
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}		300			1400			ns
Data Setup before $\overline{WR}$	t_{DW}		340			1965			ns
Data Hold after $\overline{WR}$	t_{WD}	④	45			295			ns
Data Hold after $\overline{RD}$, $\overline{PSEN}$	t_{DR}	③	0		95	0		470	ns
$\overline{RD}$ to Data in	t_{RD1}				300			1800	ns
$\overline{PSEN}$ to Data in	t_{RD2}				175			1300	ns
Address Setup to $\overline{WR}$	t_{AW}		350			1850			ns
Address Setup to $\overline{RD}$ Data in	t_{AD1}				700			3585	ns
Address Setup to $\overline{PSEN}$ data in	t_{AD2}				500			2750	ns
Address Float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}		105			600			ns
Address Float to $\overline{PSEN}$	t_{AFC2}		5			125			ns
ALE to $\overline{RD}$, $\overline{WR}$ delay	t_{LAFC1}		175			925			ns
ALE to $\overline{PSEN}$ delay	t_{LAFC2}		50			425			ns
$\overline{RD}$, $\overline{WR}$, PROG to ALE delay	t_{CA1}		35			285			ns
$\overline{PSEN}$ to ALE delay	t_{CA2}		280			1285			ns
Port Control Setup to PROG	t_{CP}	⑤	85			460			ns
Port Control Hold from PROG	t_{PC1}	⑤, ⑥	0		80	0		200 ⑧	ns
	t_{PC2}	⑤, ⑦	135			1135			ns
Input Data Setup to PROG	t_{PR}	⑤			585			2715	ns
Input Data Hold from PROG	t_{PF}		0		125	0		500	ns
Output Data Setup to PROG	t_{DP}		350			1850			ns
Output Data Hold from PROG	t_{PD}		75			450			ns
PROG Pulse Width	t_{PP}		625			3250			ns
Port 2 I/O Data Setup to ALE	t_{PL}		135			1135			ns
Port 2 I/O Data Hold from ALE	t_{LP}		5			125			ns
ALE to Port Output	t_{PV}				475			1600	ns
T0 Output Cycle Time	t_{OPRR}		250			1000			ns

Notes:

③ Control Outputs C_L = 80 pF; BUS Output: C_L = 150 pF

④ C_L = 20 pF

⑤ Control Outputs: C_L = 80 pF

⑥ During Execution of MOVD A, Pp

⑦ During Execution of MOVD Pp, A, ANLD Pp, A, ORLD Pp, A

⑧ See supply voltage and port Control hold time characteristic curves

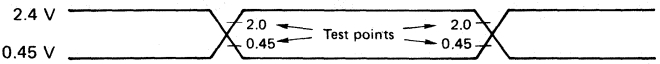
4

t_{CY}-DEPENDENT BUS TIMING DEFINITIONS

PARAMETER	CALCULATION FORMULA	MIN	MAX	UNIT
t_{LL}	(7/30) T – 170	●		ns
t_{AL}	(1/ 5) T – 110	●		ns
t_{LA}	(1/15) T – 40	●		ns
t_{CC1}	(1/ 2) T – 200	●		ns
t_{CC2}	(2/ 5) T – 200	●		ns
t_{DW}	(13/30) T – 200	●		ns
t_{WD}	(1/15) T – 40	●		ns
t_{DR}	(1/10) T – 30		●	ns
t_{RD1}	(2/ 5) T – 200		●	ns
t_{RD2}	(3/10) T – 200		●	ns
t_{AW}	(2/ 5) T – 150	●		ns
t_{AD1}	(23/30) T – 250		●	ns
t_{AD2}	(3/ 5) T – 250		●	ns
t_{AFC1}	(2/15) T – 65	●		ns
t_{AFC2}	(1/30) T – 40	●		ns
t_{LAFC1}	(1/ 5) T – 75	●		ns
t_{LAFC2}	(1/10) T – 75	●		ns
t_{CA1}	(1/15) T – 50	●		ns
t_{CA2}	(4/15) T – 50	●		ns
t_{CP}	(1/10) T – 40	●		ns
t_{PC2}	(4/15) T – 200	●		ns
t_{PR}	(17/30) T – 120		●	ns
t_{PF}	(1/10) T		●	ns
t_{DP}	(2/ 5) T – 150	●		ns
t_{PD}	(1/10) T – 50	●		ns
t_{PP}	(7/10) T – 250	●		ns
t_{PL}	(4/15) T – 200	●		ns
t_{LP}	(1/30) T – 40	●		ns
t_{PV}	(3/10) T + 100		●	ns
t_{OPRR}	(1/ 5) T	●		ns
t_{CY}	$(1/f_{XTAL})$ x 15			μs

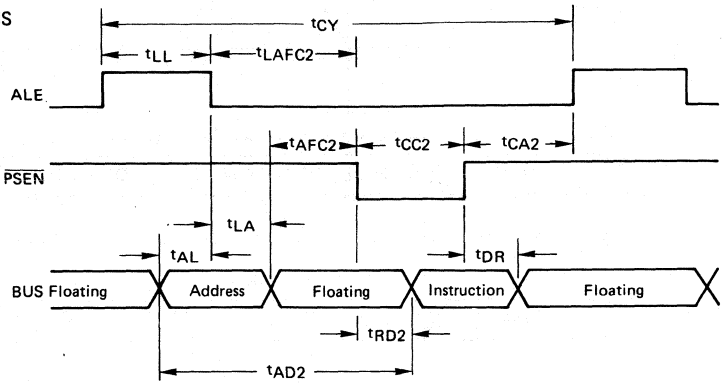
Remarks: T = t_{CY}

AC TEST I/O WAVEFORM

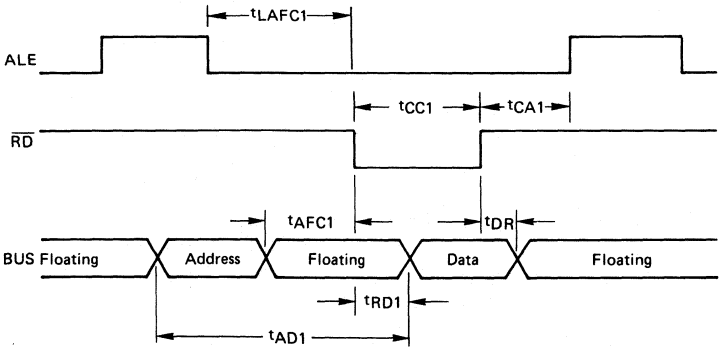


TIMING WAFEFORMS

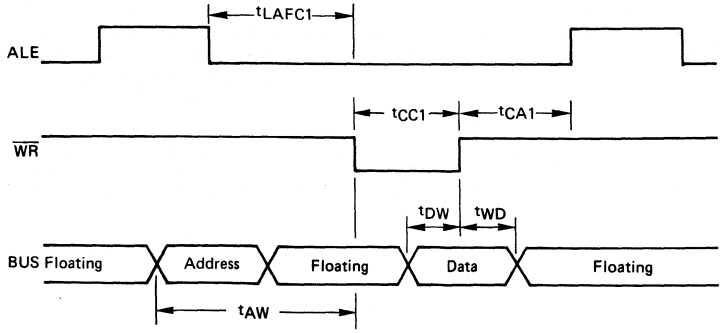
Instruction fetch from external program memory



Read from external data memory

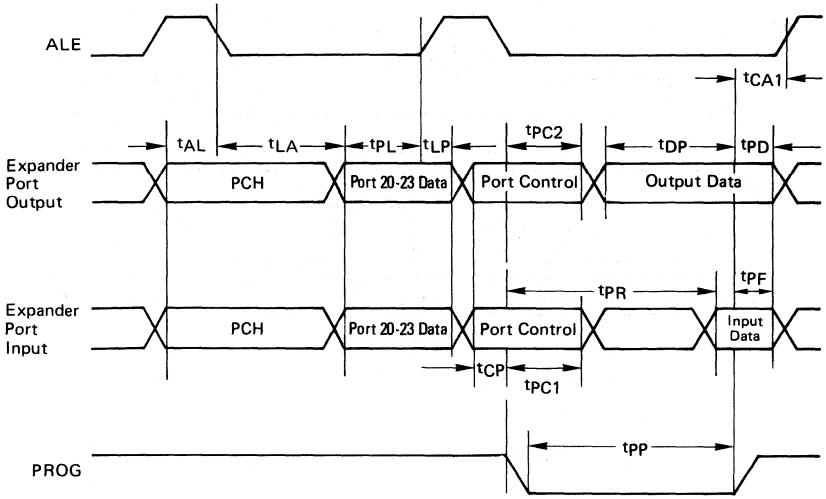


Write to external data memory

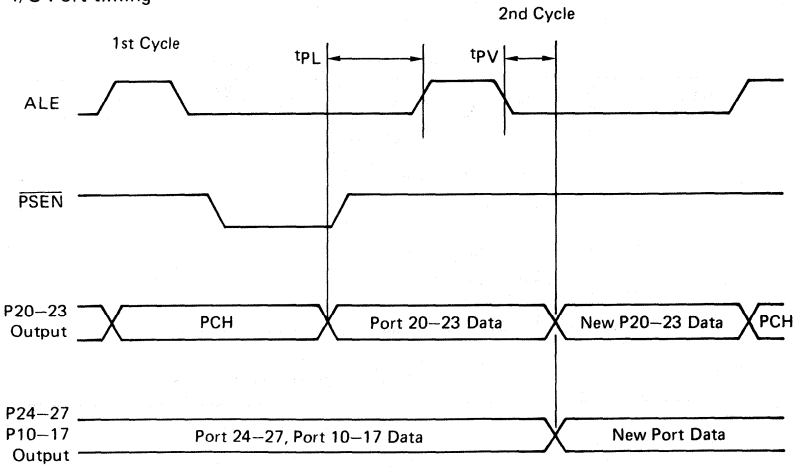


4

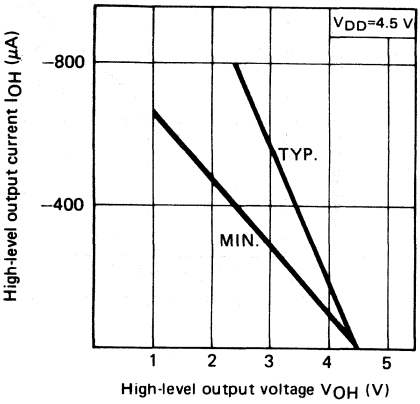
Port 2 extended timing

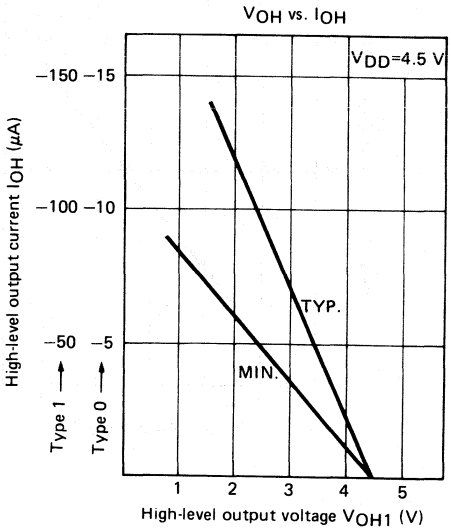


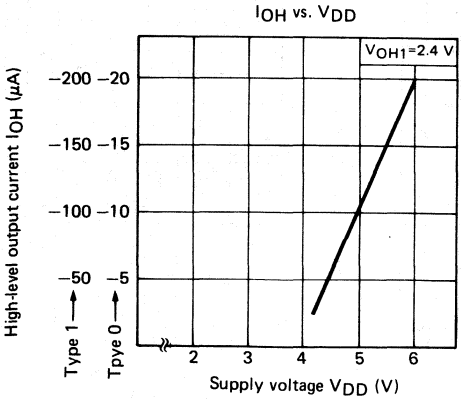
I/O Port timing

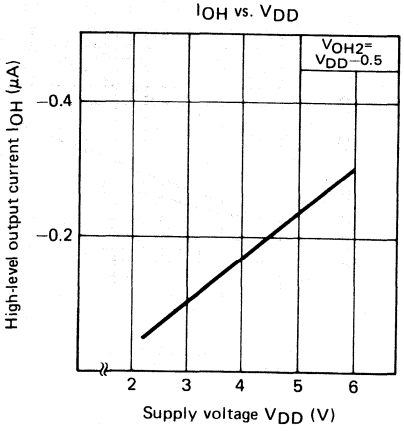


CHARACTERISTIC CURVES (T_a = 25° C)





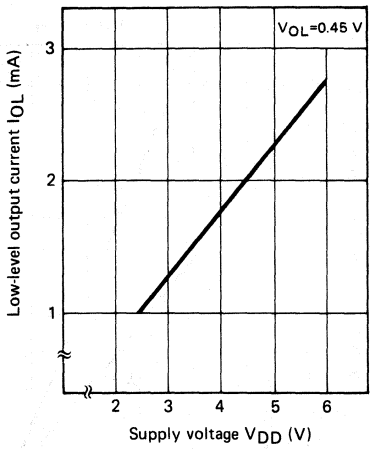




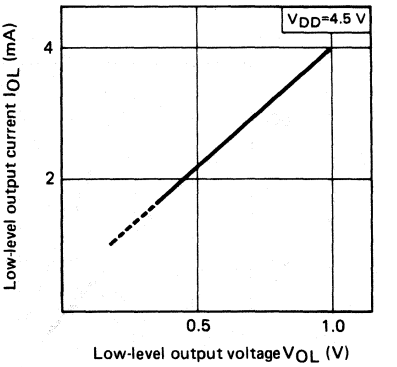
4

CHARACTERISTIC CURVES (Continued)

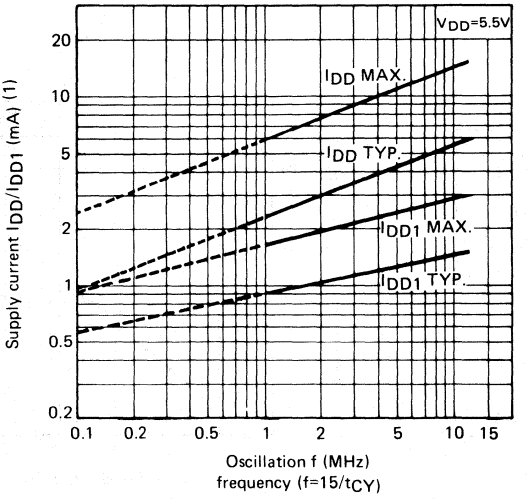
I_{OL} vs. V_{DD}



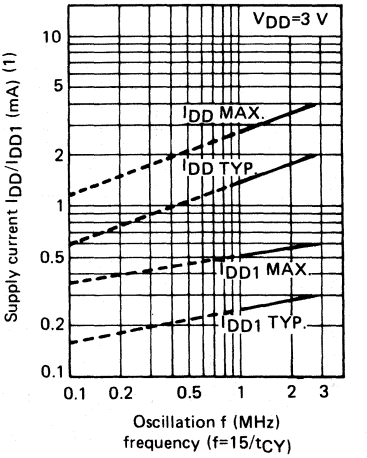
I_{OL} vs. V_{OL}



I_{DD}/I_{DD1} vs. f



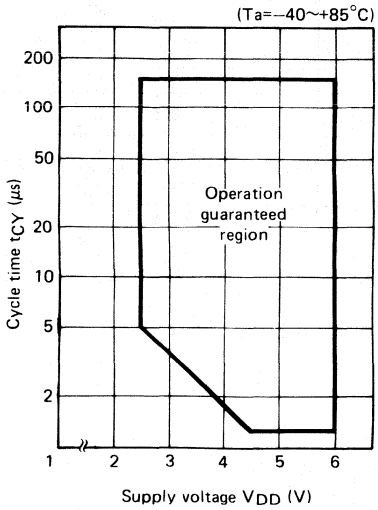
I_{DD}/I_{DD1} vs. f



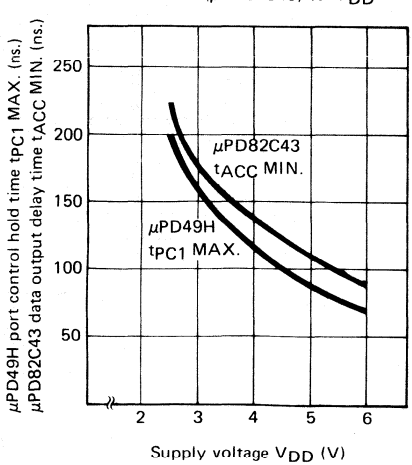
Note:
1) Less than 1 MHz for external oscillation. Power consumption is larger with internal oscillation than with external oscillation.

CHARACTERISTIC CURVES (Continued)

t_{CY} vs. V_{DD}



t_{PC1} MAX. (μPD49H)/t_{ACC} MIN. (μPD82C43) vs. V_{DD}

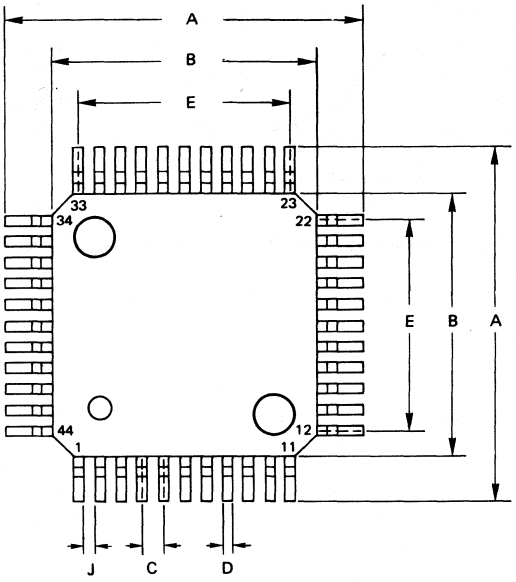


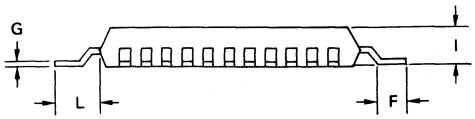
Remarks: The operation guaranteed region and characteristics curves not shown are all reference values.

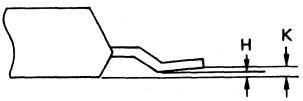
4

PACKAGE DIMENSIONS
μPD49HG
44 PIN PLASTIC
FLAT PACK

ITEM	MILLIMETERS	INCHES
A	13.6 ± 0.4	0.54 ± 0.016
B	10	.394
C	0.8 ± 0.15	.03 ± 0.006
D	.35 $^{+0.3}_{-0.1}$	.014 $^{+.01}_{-.004}$
E	8.0 ± 0.3	.315 ± .012
F	1.0 ± 0.2	.39 ± .008
G	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
H	0.0 ± 0.1	0.0 ± .004
I	1.4 $^{+0.2}_{-0.1}$	0.06 $^{+0.008}_{-0.004}$
J	0.2 min	0.008 min
K	0.0 ± 0.2	0.0 ± 0.008
L	1.8 ± 0.2	0.071 ± 0.008







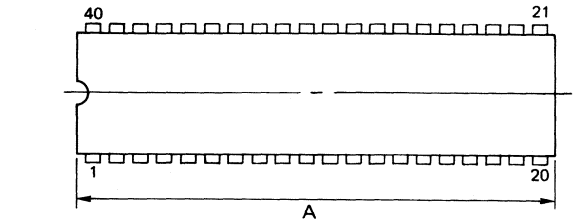
Lead bend (enlarged view)

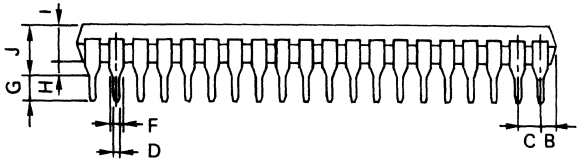
PACKAGE DIMENSIONS
μPD80C49HC/
μPD80C39HC
40 PIN PLASTIC DIP

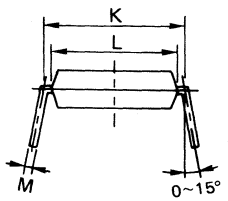
ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T. P.)	0.100 (T. P.)
D	0.50 ± 0.10	0.020 $^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6 ± 0.3	0.142 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T. P.)	0.600 (T. P.)
L	13.2	0.520
M	0.25 $^{+0.10}_{-0.05}$	0.010 $^{+0.004}_{-0.003}$
N	0.25	0.01

Notes: 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T. P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.







4

CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

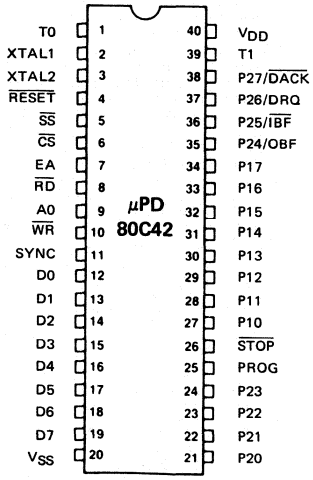
DESCRIPTION

The μPD80C42 is designed to function as a slave CPU, particularly as an intelligent peripheral controller in the microcomputer system using the μCOM84/84C or μCOM85 as a master CPU. Interface with the system data bus can be easily made via the internal interface register (data bus buffer register, status register). The program memory is 2K x 8 bits. The data memory is 128 x 8 bits. 16 I/O ports (2 x 8 bits) compatible with TTL can be easily extended by using the μPD82C43 that is directly connectable to the μPD80C42.

FEATURES

- Single-chip microcomputer
- Compatible with the μCOM84/84C and μCOM85
- Instruction cycle: 1.25 μs/12 MHz
- Program memory (ROM) : 2K x 8 bits
- Data memory (RAM) : 128 x 8 bits
- Input/output port (P_{10-17}, P_{20-27}) : 2 x 8 bits
- Asynchronous slave – Master interface
  2 data registers: DBBIN, DBBOUT
  8-bit status
- Internal timer/counter: 8 bits
- 2 pairs of working registers (2 x 8 x 8 bits)
- 8-level stack
- Internal clock generator
- Interrupt function
- DMA function
- Easy expandable I/O port
- Single-step operation available
- Standby function
- CMOS
- Single power supply: +2.5V ~ +6.0V
- Intel 8042 pin compatible
- 40-pin plastic DIP

PIN CONFIGURATION

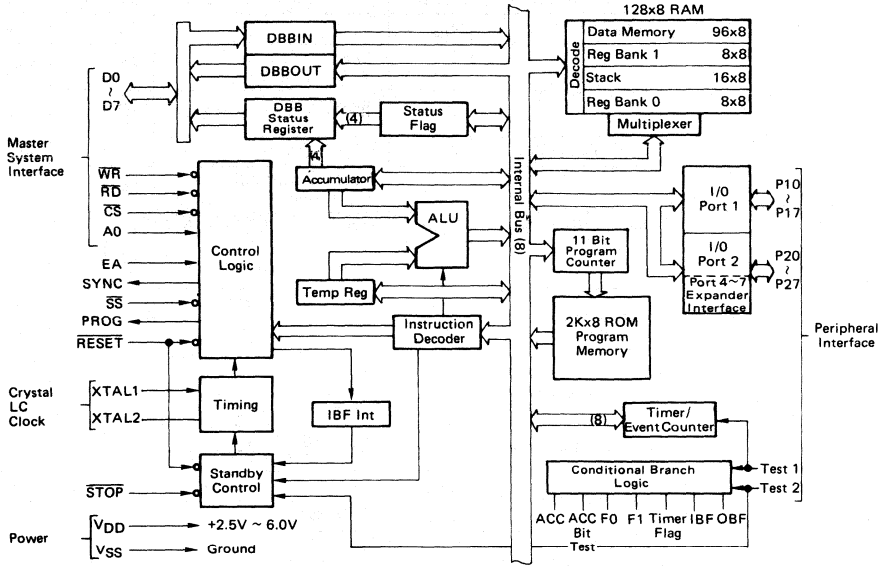


PIN IDENTIFICATION

NO.	PIN SYMBOL	PIN NAME	FUNCTION
1	T0	Test 0	Testable input using conditional jump instructions JT0 and JNT0. Also enables clock output via the ENTO CLK instruction.
2	XTAL1	Crystal 1	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. May also be used as an input for external clock signals. (Non-TTL-compatible V_{IH}.)
3	XTAL2	Crystal 2	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. (Non-TTL-compatible V_{IH}.)
4	$\overline{RESET}$	Reset	Active-low input line that initializes the processor. Also used to release both the Halt and Stop modes.
5	$\overline{SS}$	Single Step	Active-low input line, that, in conjunction with ALE, causes the processor to single-step through a program one instruction at a time.
6	$\overline{CS}$	Chip Select	This is an input for chip select signal. When 0 (low-level) is input to this pin, the data bus is enabled.
7	EA	External Access	Input line that inhibits internal program memory fetches and initiates access of external program memory. Essential for system testing and may also be used for program debugging.
8	$\overline{RD}$	Read	Active-low output strobe line that is used to read data from external data memory.
9	A0		Indicates the address input from the master CPU and the kind of data on the data bus. • Read cycle A0 = 0: Data A0 = 1: Status • Write cycle A0 = 0: Data A0 = 1: Command
10	$\overline{WR}$	Write	Active-low output strobe line that is used to write data into external data memory.
11	SYNC		This is an output pin for a signal output at each machine cycle, and used for strobe of external circuit or single-step operation.
12-19	DB_0-DB_7	Bus	These I/O lines constitute an 8-bit bidirectional data/address bus. Synchronous read and write operations can be performed on this bus using $\overline{RD}$ and $\overline{WR}$ signals. Data driven out on the bus by an OUTL BUS instruction is statically latched. The address of external memory is available on the bus at the falling edge of ALE when reading from external program memory or writing to and reading from external data memory. During external program memory fetches, the least-significant 8 bits of the external program memory address are driven out on the bus and the addressed instruction is fetched using $\overline{PSEN}$. When no external memory is used, the bus can serve as a true bidirectional 8-bit port. Information is strobed in or out by the $\overline{RD}$ and $\overline{WR}$ signals.
20	V_{SS}	Ground	Ground potential.
21-24, 35-38	P_{20}-P_{27}	Port 2	These lines constitute Port 2, an 8-bit quasi-bidirectional port. During external program memory fetches P_{20}-P_{23} output the most-significant 4 bits of the external program memory address. Lines P_{20}-P_{23} can also be used as a 4-bit I/O expander bus to interface with the optional μPD82C43 I/O expander.
25	PROG	Program Pulse	This line is used as an output strobe when interfacing with the optional μPD82C43 I/O expander.
26	$\overline{STOP}$	Stop	Used for controlling the hardware STOP mode.
27-34	P_{10}-P_{17}	Port 1	These lines constitute Port 1, an 8-bit, generalpurpose quasi-bidirectional port.
39	T1	Test 1	Testable input using conditional jump instructions JT1 and JNT1. Can also be used as the timer/counter input line via the STRT CNT instruction.
40	V_{DD}	Primary Power Supply	Power supply. V_{CC} must be between +2.5V to +6V for normal operation. In Stop mode, V_{CC} must be at least +2V to ensure data retention.

Note: $\overline{CS}$, A0, $\overline{RD}$, $\overline{WR}$, TEST0 and TEST1 pins must not be floated to prevent a malfunction.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature, T_{opt}	−40°C to +85°C
Storage Temperature (Plastik Package), T_{stg}	−65°C to +150°C
Voltage on Any Pin, $V_{I/O}$	V_{SS} −0.3V to V_{DD} +0.3V
Supply Voltage, V_{DD}	V_{SS} −0.3 to +7V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS $T_a = -40°C \sim +85°C$, $V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Low	V_{IL}		−0.3		+0.8	V
Input Voltage High	V_{IH}	Except $\overline{RESET}$, XTAL1, XTAL2	2.2		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2	V_{DD} −1		V_{DD}	V
Output Voltage Low	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output Voltage High	V_{OH}	D0-D7, SYNC, PROG I_{OH} = −400 μA	2.4			V
	V_{OH1}	PORT1, PORT2, I_{OH} = −50 μA	2.4			V
	V_{OH2}	All Outputs, I_{OH} = −0.2 μA	V_{DD} −0.5			V
Input Current	I_{ILP}	PORT1, PORT2; $V_I \leqslant V_{IL}$			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqslant V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T0, T1, $\overline{STOP}$, $\overline{CS}$, A0, $\overline{RD}$, $\overline{WR}$; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±3	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqslant V_O \leqslant V_{DD}$ High Impedance, D0-D7, PORT			±1	μA
Standby Current	I_{DD1}	HALT Mode; t_{CY} = 1.25 μs		1.5	3.0	mA
	I_{DD2}	STOP Mode*		1	20	μA
Supply Current	I_{DD}	t_{CY} = 1.25 μs		10	20	mA
Data Retention Voltage	V_{DDDR}	$\overline{STOP}$ mode ($\overline{STOP}$, $\overline{RESET} \leqslant 0.4V$) or $\overline{RESET}$ ($\overline{RESET} \leqslant 0.4V$)	2.0			V

Note *: The input pin voltage is $V_I \leqslant V_{IL}$ or $V_I \geqslant V_{IH}$.

AC CHARCTERISTICS $T_a = -40$ to $+85°C$, $V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

DBB READ:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$, A0 Setup to $\overline{RD}$ ↓	t_{AR}		0			ns
$\overline{CS}$, A0 Hold from $\overline{RD}$ ↑	t_{RA}		0			ns
$\overline{RD}$ Pulse Width	t_{RR}		200			ns
$\overline{CS}$, A0 to Data Output Delay	t_{AD}	*1			150	ns
$\overline{RD}$ ↓ to Data Output Delay	t_{RD}	*1			140	ns
$\overline{RD}$ ↑ to Data Float Delay	t_{DF}				85	ns
Cycle Time	t_{CY}		1.25		15	μs

DBB WRITE:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$, A0 Setup to $\overline{WR}$ ↓	t_{AW}		0			ns
$\overline{CS}$, A0 Hold from $\overline{WR}$ ↑	t_{WA}		0			ns
$\overline{WR}$ Pulse Width	t_{WW}		200			ns
Data Setup to $\overline{WR}$ ↑	t_{DW}		130			ns
Data Hold from $\overline{WR}$ ↑	t_{WD}		0			ns

PORT2:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Port Control Setup to PROG ↓	t_{CP}	*2	100			ns
Port Control Hold from PROG ↓	t_{PC}	*3	0		80	ns
Input Data Setup to PROG ↓	t_{PR}	*2			650	ns
Input Data Hold from PROG ↑	t_{PF}	*3	0		150	ns
Output Data Setup to PROG ↑	t_{DP}	*2	200			ns
Output Data Hold from PROG ↑	t_{PD}	*3	60			ns
PROG Pulse Width	t_{PP}		700			ns

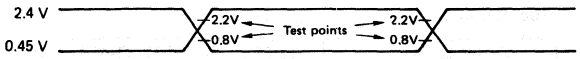
DMA:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{DACK}$ Setup to $\overline{RD}$, $\overline{WR}$	t_{ACC}		0			ns
$\overline{DACK}$ Hold from $\overline{RD}$, $\overline{WR}$	t_{CAC}		0			ns
$\overline{DACK}$ to Data Output Delay	t_{ACD}				140	ns
$\overline{RD}$, $\overline{WR}$ to DRQ Clear Delay	t_{CRQ}	*4			130	ns

*1: $C_L = 100$ pF
*2: $C_L = 80$ pF
*3: $C_L = 20$ pF
*4: $C_L = 150$ pF

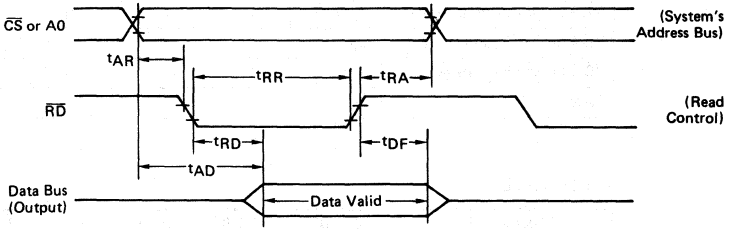
4

AC TEST INPUT/OUTPUT WAVEFORM

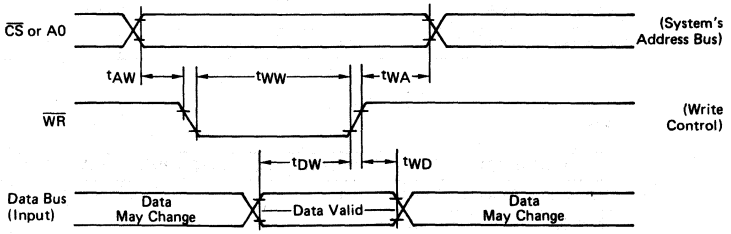


TIMING WAVEFORMS

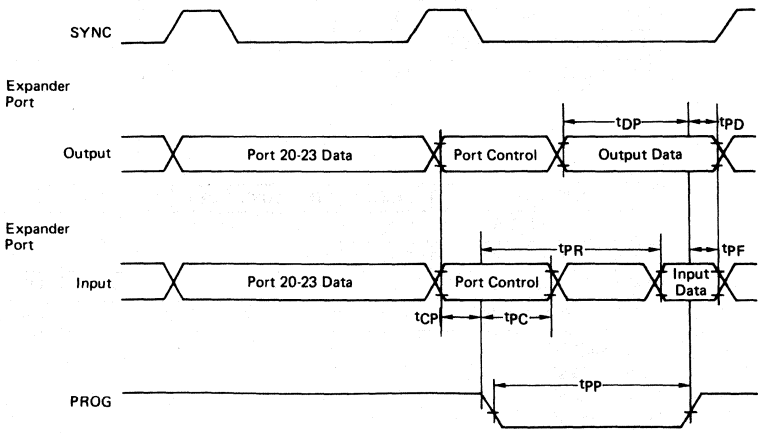
Read Operation (DBBOUT Register)



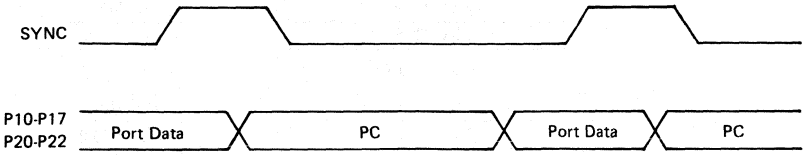
Write Operation (DBBIN Register)



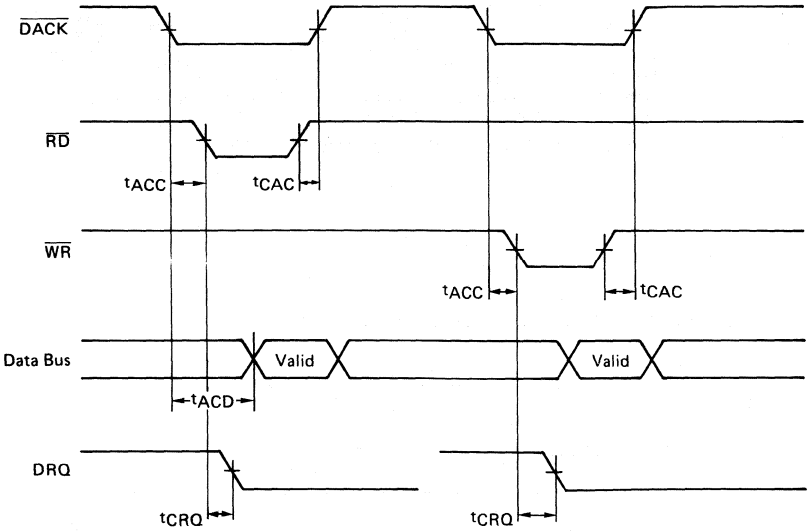
Port 2



Port (EA=1)



DMA



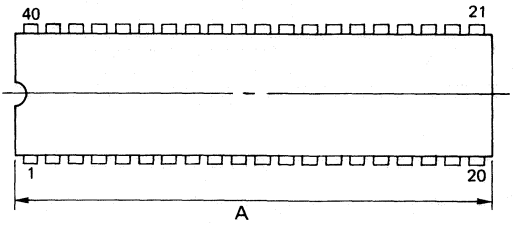
4

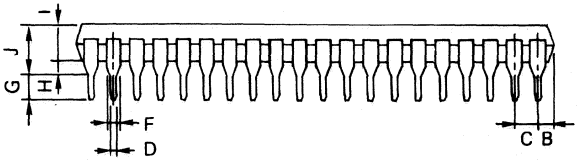
PACKAGE DIMENSIONS
μPD80C42C
40 PIN PLASTIC DIP

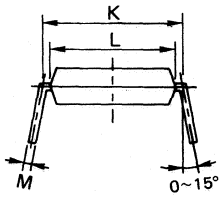
ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T. P.)	0.100 (T. P.)
D	0.50 ± 0.10	0.020 $^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6 ± 0.3	0.142 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T. P.)	0.600 (T. P.)
L	13.2	0.520
M	0.25 $^{+0.10}_{-0.05}$	0.010 $^{+0.004}_{-0.003}$
N	0.25	0.01

Notes: 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T. P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.







CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

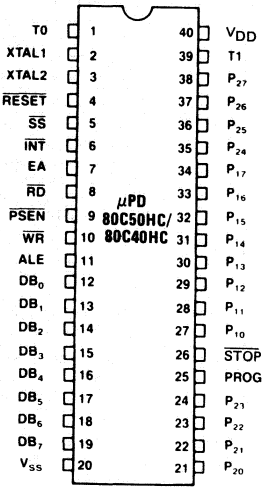
DESCRIPTION

The μPD80C50H is a single chip 8-bit microcomputer containing 8-bit CPU, ROM, RAM, I/O ports and control circuit on one CMOS chip. The μPD80C40H is the product in which the ROM is eliminated from the μPD80C50H. The μPD80C50H/40H, fabricated by CMOS technology, realizes low power consumption and data retention is also available with less power consumption.

FEATURES

- Single chip 8-bit microcomputer
- 98 instructions
- Instruction cycle: 1.25 μs/12 MHz
- Operating function
  Addition, logic operation, and decimal adjust
- ROM 4K x 8 bits (μPD80C50H)
- RAM 256 x 8 bits
- Stand-by function
- 8-level stack
- Two sets of working registers
- Interrupt capability
- Two test inputs
- Internal Timer/Event Counter
- Easy expandable Memory and I/O ports
- Input/Output ports
  Input/Output ports: 8 bits x 2
  Data bus (alternative for I/O ports): 8 bits x 1
- Single step function
- Internal Clock generator
- CMOS
- Single power supply: +2.5 ~ +6.0V
- 40 pin plastic DIP (μPD80C50HC/80C40HC) and 44 pin plastic FLAT Pack (μPD80C50HG)
- Intel 8050H, 8040H pin compatible

PIN CONFIGURATION



PIN IDENTIFICATION

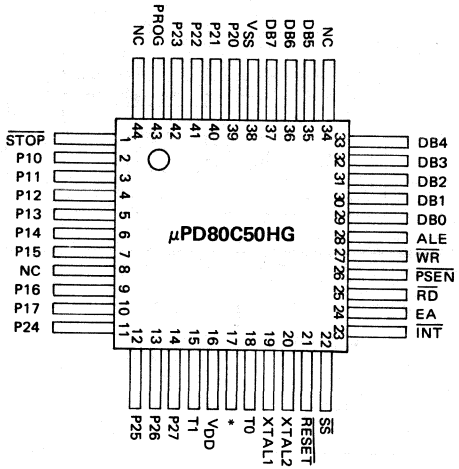
A.
μPD80C50HC/
μPD80C40HC
(40 PIN PLASTIC DIP)

B.
μPD80C50HG
(44 PIN PLASTIC
FLAT PACK)

PIN				
B.	A.	SYMBOL	NAME	FUNCTION
18	1	T0	Test 0	Testable input using conditional jump instructions JT0 and JNT0. Also enables clock output via the ENT0 CLK instruction.
19	2	XTAL1	Crystal 1	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. May also be used as an input for external clock signals. (Non-TTL-compatible V_{IH}.)
20	3	XTAL2	Crystal 2	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. (Non-TTL-compatible V_{IH}.)
21	4	$\overline{RESET}$	Reset	Active-low input line that initializes the processor. Also used to release both the Halt and Stop modes. ①
22	5	$\overline{SS}$	Single Step	Active-low input line, that, in conjunction with ALE, causes the processor to single-step through a program one instruction at a time.
23	6	$\overline{INT}$	Interrupt	Active-low input line that causes an interrupt if an enable instruction has been executed. A reset disables the interrupt. May be used as a testable input with a conditional jump instruction. Can also be used to release the Halt mode.
24	7	EA	External	Input line that inhibits internal program memory fetches and initiates access of external program memory. Essential for system testing and may also be used for program debugging.
25	8	$\overline{RD}$	Read	Active-low output strobe line that is used to read data from external data memory.
26	9	$\overline{PSEN}$	Program Store Enable	Active-low output line that is used to fetch instructions from external program memory.
27	10	$\overline{WR}$	Write	Active-low output strobe line that is used to write data into external data memory.
28	11	ALE	Address Latch Enable	Output line for address latch enable. At the falling edge of ALE, the address of either external data memory or external program memory is available on the bus.
29-33, 35-37	12-19	DB_0-DB_7	Bus	These I/O lines constitute an 8-bit bidirectional data/address bus. Synchronous read and write operations can be performed on this bus using $\overline{RD}$ and $\overline{WR}$ signals. Data driven out on the bus by an OUTL BUS instruction is statically latched. The address of external memory is available on the bus at the falling edge of ALE when reading from external program memory or writing to and reading from external data memory. During external program memory fetches, the least-significant 8 bits of the external program memory address are driven out on the bus and the addressed instruction is fetched using $\overline{PSEN}$. When no external memory is used, the bus can serve as a true bidirectional 8-bit port. Information is strobed in or out by the $\overline{RD}$ and $\overline{WR}$ signals.
38	20	V_{SS}	Ground	Ground potential.
39-42, 11-14	21-24, 35-38	P_{20}-P_{27}	Port 2	These lines constitute Port 2, an 8-bit quasi-bidirectional port. During external program memory fetches P_{20}-P_{23} output the most-significant 4 bits of the external program memory address. Lines P_{20}-P_{23} can also be used as a 4-bit I/O expander bus to interface with the optional μPD82C43 I/O expander.
43	25	PROG	Program Pulse	This line is used as an output strobe when interfacing with the optional μPD82C43 I/O expander.
1	26	$\overline{STOP}$	Stop	Used to control the hardware STOP mode.
2- 7,	27-34	P_{10}-P_{17}	Port 1	These lines constitute Port 1, an 8-bit, generalpurpose quasi-bidirectional port.
15	39	T1	Test 1	Testable input using conditional jump instructions JT1 and JNT1. Can also be used as the timer/counter input line via the STRT CNT instruction.
16	40	V_{DD}	Primary Power Supply	Power supply. V_{CC} must be between +2.5V to +6V for normal operation. In Stop mode, V_{CC} must be at least +2V to ensure data retention.

Note: ① The pulse width of RESET must be a minimum of 5 machine cycles in length following oscillator stabilization to reinitialize the processor and stabilize CPU operation. At power-up, the states of the output lines are undefined until completion of reset.

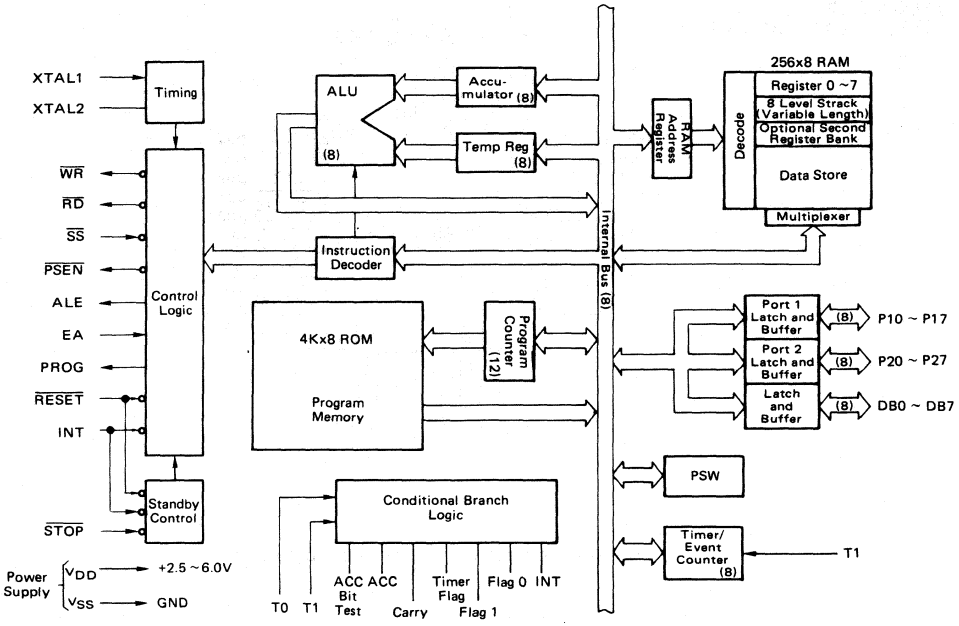
PIN CONFIGURATION
μPD80C50HG
(44 PIN FLAT PACKAGE)



* INTERNAL CONNECTION IT IS PROHIBITED TO USE PIN 17

4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature, T_{opt}	−40°C to +85°C
Storage Temperature (Plastic Package), T_{stg}	−65°C to +150°C
Voltage on Any Pin, $V_{I/O}$	V_{SS} −0.3V to V_{DD} +0.3V
Supply Voltage, V_{DD}	V_{SS} −0.3 to +7V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS $T_a = -40°C \sim +85°C$, $V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		+0.8	V
Input High Voltage	V_{IH}	Except XTAL1, XTAL2, $\overline{RESET}$, $\overline{SS}$	$V_{DD}-2$		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$	$V_{DD}-1$		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA			+0.45	V
Output High Voltage	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; I_{OH} = −400 μA	2.4			V
	V_{OH1} ①	PORT1, PORT2; I_{OH} = −5 μA (Type 0)	2.4			V
		PORT1, PORT2; I_{OH} = −50 μA (Type 1)	2.4			V
Input Current	I_{ILP} ①	PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 0)		−15	−40	μA
		PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqslant V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±3	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqslant V_O \leqslant V_{DD}$ High Impedance, BUS, T0 ③			±1	μA
Standby Current	I_{DD1}	HALT mode; t_{CY} = 1.25 μs		1.5	3.0	mA
	I_{DD2}	STOP Mode ②		1	20	μA
Supply Current (Total)	I_{DD}	t_{CY} = 1.25 μs		6	18	mA
Data Retention Voltage	V_{DDDR}	at the hardware STOP mode ($\overline{STOP}$, $\overline{RESET}$ ⩽0.4V) or or $\overline{RESET}$ ($\overline{RESET}$ ⩽0.4V)	2.0			V

4

DC CHARACTERISTICS $T_a = -40°C \sim +85°C$, $V_{DD} = +2.5V \sim +6.0V$, $V_{SS} = 0V$

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL}			−0.3		0.18 V_{DD}	V
Input High Voltage	V_{IH}	Except XTAL1, XTAL2, $\overline{RESET}$, $\overline{SS}$		0.7 V_{DD}		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$		0.8 V_{DD}		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 1.0 mA				0.45	V
Output High Voltage	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; I_{OH} = −100 μA		0.75 V_{DD}			V
	V_{OH1} ①	PORT1, PORT2; I_{OH} = −1 μA (Type 0)		0.7 V_{DD}			V
		PORT1, PORT2; I_{OH} = −10 μA (Type 1)		0.7 V_{DD}			V
Input Current	I_{ILP} ①	PORT1, PORT2; $V_I \leq V_{IL}$ (Type 0)			−15	−40	μA
		PORT1, PORT2; $V_I \leq V_{IL}$ (Type 1)				−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leq V_{IL}$				−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leq V_I \leq V_{DD}$				±1	μA
	I_{LI2}	EA; $V_{SS} \leq V_I \leq V_{DD}$				±5	μA
Output Leakage Current	I_{LO}	$V_{SS} \leq V_O \leq V_{DD}$ ③ High Impedance, BUS, T0				±1	μA
Standby Current	I_{DD1}	HALT mode	V_{DD} = 3V; t_{CY} = 5 μs		0.3	0.6	mA
			V_{DD} = 6V; t_{CY} = 1.25 μs		2.0	4.0	mA
	I_{DD2}	STOP Mode ②	V_{DD} = 3V		1	20	μA
			V_{DD} = 6V		1	50	μA
Supply Current	I_{DD}	V_{DD} = 3V; t_{CY} = 5 μs			2.0	5.0	mA
		V_{DD} = 6V; t_{CY} = 1.25 μs			10	25	mA

Notes:

① Option specification of type 0 and type 1 is available only for the μPD80C50H. The μPD80C40H has the type 0 only.

② The input pin voltage is $V_I \leq V_{IL}$ or $V_I \geq V_{IH}$.

③ Output pins of PORT1 and PORT2 specified as the type 2 are also included.

AC CHARACTERISTICS

T_a = −40 to +85°C, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	V_{DD} = +5V ±10%			V_{DD} = 2.5 to 6.0V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Cycle Time	t_{CY}		1.25		150	5		150	μs
ALE Pulse Width	t_{LL}		125			995			ns
Address Setup before ALE	t_{AL}		140			890			ns
Address Hold from ALE	t_{LA}		45			295			ns
Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	④	425			2300			ns
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}		300			1800			ns
Data Setup before $\overline{WR}$	t_{DW}		340			1965			ns
Data Hold after $\overline{WR}$	t_{WD}	⑤	45			295			ns
Data Hold after $\overline{RD}$, $\overline{PSEN}$	t_{DR}		0		95	0		470	ns
$\overline{RD}$ to Data in	t_{RD1}				300			1800	ns
$\overline{PSEN}$ to Data in	t_{RD2}				175			1300	ns
Address Setup before $\overline{WR}$	t_{AW}		350			1850			ns
Address Setup before Data in ($\overline{RD}$)	t_{AD1}				700			3585	ns
Address Setup before Data in ($\overline{PSEN}$)	t_{AD2}	④			500			2750	ns
Address Float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}		105			600			ns
Address Float to $\overline{PSEN}$	t_{AFC2}		5			125			ns
ALE to Control Signal ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}		175			925			ns
ALE to Control Signal ($\overline{PSEN}$)	t_{LAFC2}		50			425			ns
Control Signal ($\overline{RD}$, $\overline{WR}$, PROG) to ALE	t_{CA1}		35			285			ns
Control Signal ($\overline{PSEN}$) to ALE	t_{CA2}		280			1285			ns
Port Control Setup before Falling Edge of PROG	t_{CP}	⑥	85			460			ns
Port Control Hold after Falling Edge of PROG	t_{PC1}	⑥, ⑦	0		80	0		200 ⑨	ns
	t_{PC2}	⑥, ⑧	135			1135			ns
PROG to Time P2 Input must be Valid	t_{PR}				585			2715	ns
Input Data Hold Time	t_{PF}		0		125	0		500	ns
Output Data Setup Time	t_{DP}		350			1850			ns
Output Data Hold Time	t_{PD}		75			450			ns
PROG Pulse Width	t_{PP}	⑥	625			3250			ns
PORT2 I/O Data Setup Time	t_{PL}		135			1135			ns
PORT2 I/O Data Hold Time	t_{LP}		5			125			ns
ALE to PORT Output	t_{PV}				475			1600	ns
T0 Clock Period	t_{OPRR}		250			1000			ns

④ Control Output: C_L = 80 pF, BUS Output: C_L = 150 pF
⑤ C_L = 20 pF
⑥ Control Output: C_L = 80 pF
⑦ At execution of MOVD A, Pp instruction
⑧ At execution of MOVD Pp, A; ANLD Pp, A; ORLD Pp, A instruction

4

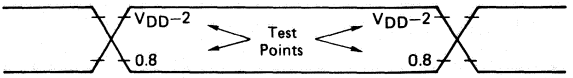
t_{CY}-DEPENDENT BUS TIMING DEFINITIONS

PARAMETER	CALCULATION FORMULA	MIN	MAX	UNIT
t_{LL}	(7/30) T − 170	•		ns
t_{AL}	(1/ 5) T − 110	•		ns
t_{LA}	(1/15) T − 40	•		ns
t_{CC1}	(1/ 2) T − 200	•		ns
t_{CC2}	(2/ 5) T − 200	•		ns
t_{DW}	(13/30) T − 200	•		ns
t_{WD}	(1/15) T − 40	•		ns
t_{DR}	(1/10) T − 30		•	ns
t_{RD1}	(2/ 5) T − 200		•	ns
t_{RD2}	(3/10) T − 200		•	ns
t_{AW}	(2/ 5) T − 150	•		ns
t_{AD1}	(23/30) T − 250		•	ns
t_{AD2}	(3/ 5) T − 250		•	ns
t_{AFC1}	(2/15) T − 65	•		ns
t_{AFC2}	(1/30) T − 40	•		ns
t_{LAFC1}	(1/ 5) T − 75	•		ns
t_{LAFC2}	(1/10) T − 75	•		ns
t_{CA1}	(1/15) T − 50	•		ns
t_{CA2}	(4/15) T − 50	•		ns
t_{CP}	(1/10) T − 40	•		ns
t_{PC2}	(4/15) T − 200	•		ns
t_{PR}	(17/30) T − 120		•	ns
t_{PF}	(1/10) T		•	ns
t_{DP}	(2/ 5) T − 150	•		ns
t_{PD}	(1/10) T − 50	•		ns
t_{PP}	(7/10) T − 250	•		ns
t_{PL}	(4/15) T − 200	•		ns
t_{LP}	(1/30) T − 40	•		ns
t_{PV}	(3/10) T + 100		•	ns
t_{OPRR}	(1/ 5) T	•		ns
t_{CY}	$(1/f_{XTAL})$ x 15			μs

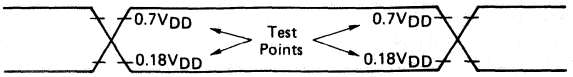
Remarks: T = t_{CY}

AC TIMING TEST POINTS (Except $\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$)

(a) V_{DD} = +5V ± 10 %

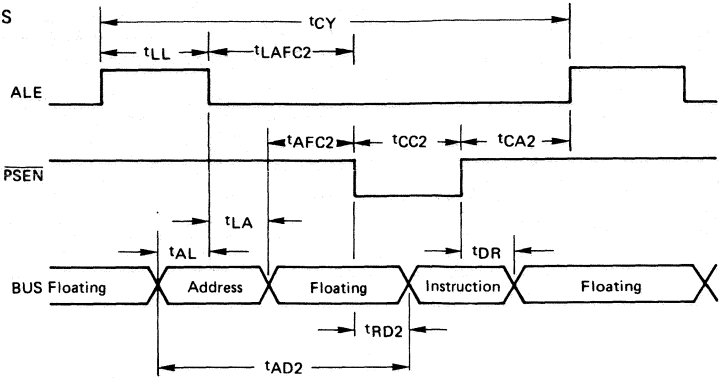


(b) V_{DD} = +2.5 to 6.0V

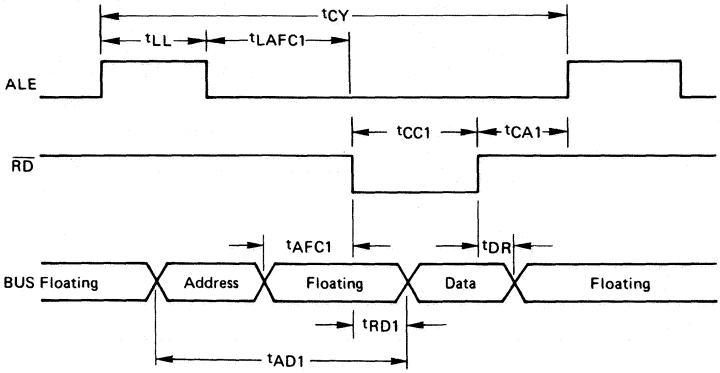


TIMING WAFEFORMS

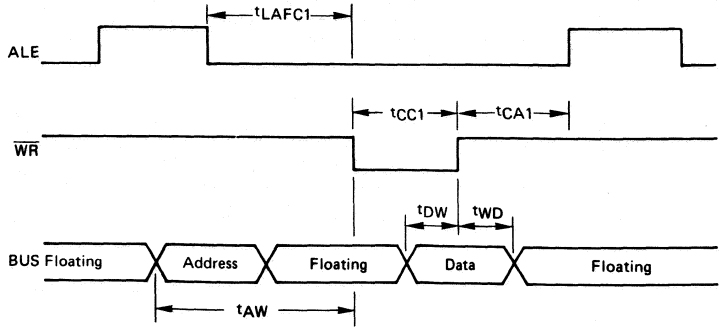
Instruction fetch from external program memory



Read from external data memory



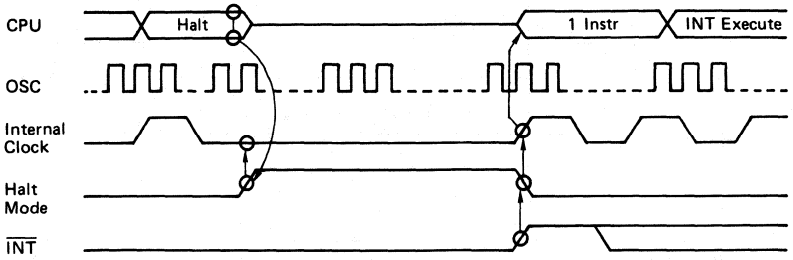
Write to external data memory



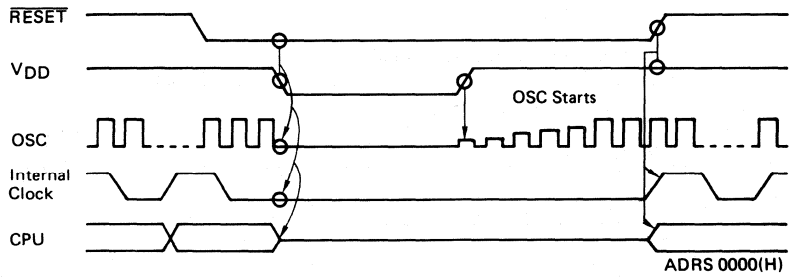
4

Low Power Standby Operation

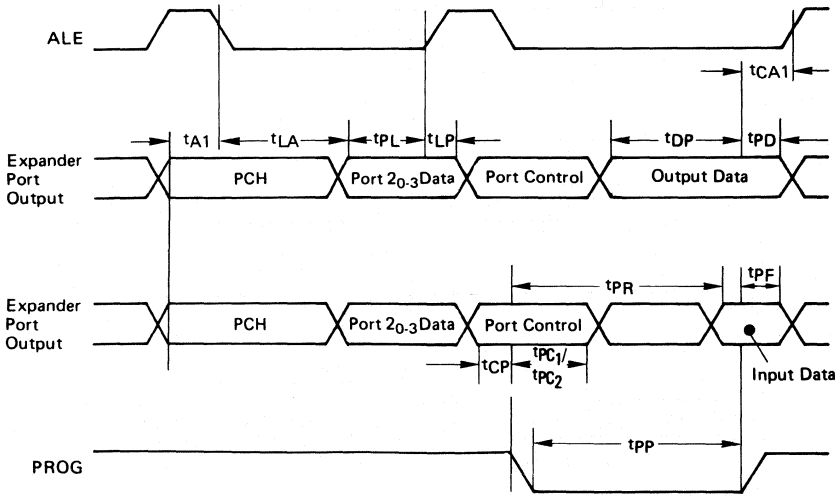
1) Halt Mode (When EI)



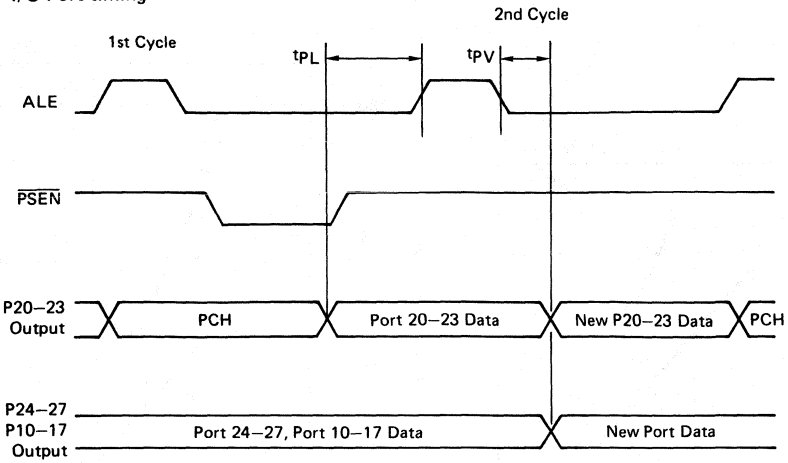
2) Stop Mode



Port 2 Timing

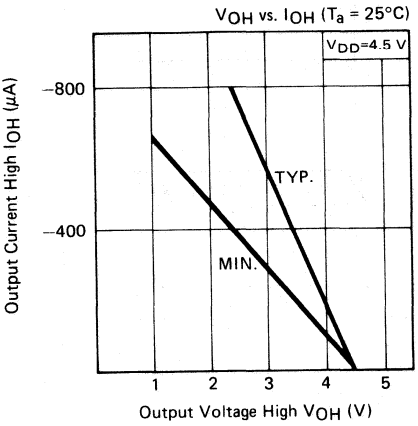


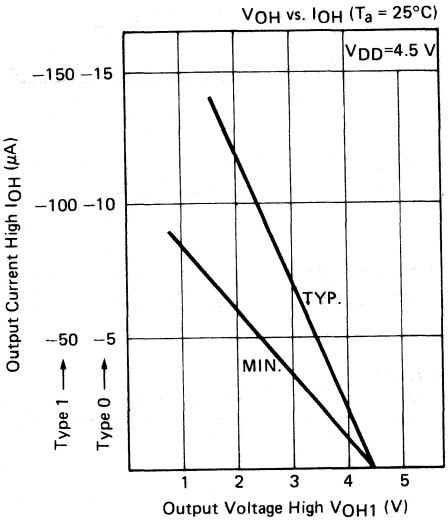
I/O Port timing

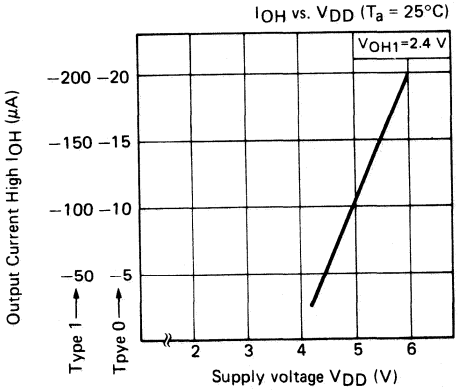


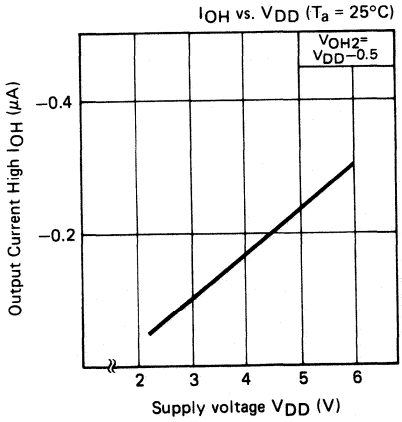
4

CHARACTERISTICS CURVES

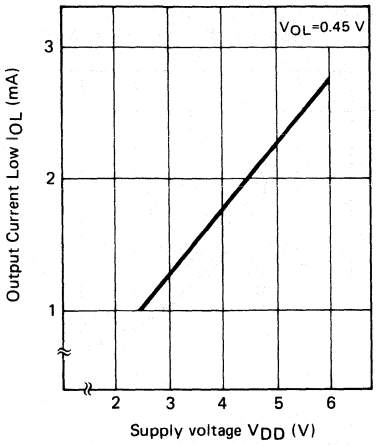




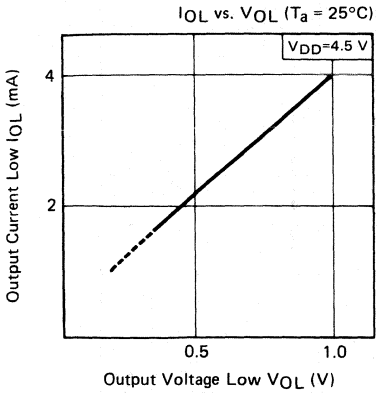




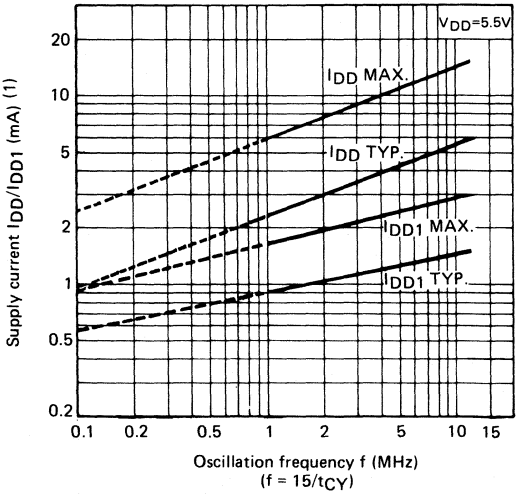
I_{OL} vs. V_{DD} (T_a = 25°C)



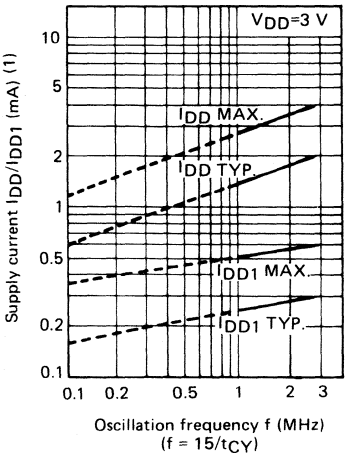
I_{OL} vs. V_{OL} (T_a = 25°C)



I_{DD}/I_{DD1} vs. f



I_{DD}/I_{DD1} vs. f (T_a = 25°C)

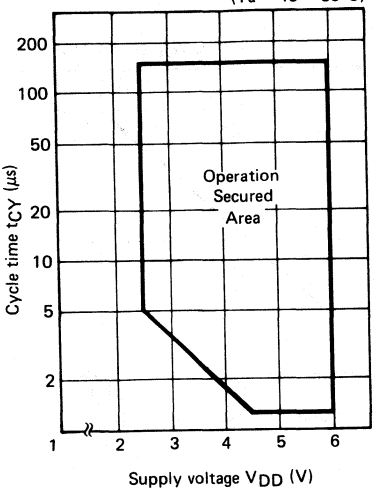


Note:

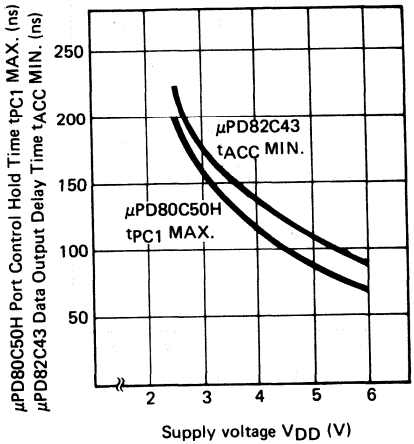
1) Curves below 1 MHz show characteristics for external oscillation.

4

t_{CY} vs. V_{DD}
(Ta=−40~+85°C)



t_{PC1} MAX. (μPD80C50H)/t_{ACC} MIN. (μPD82C43) vs. V_{DD} (T_a = 25°C)



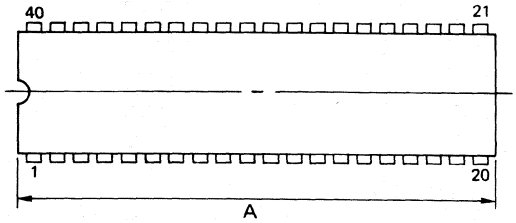
Note: Curves without "operation secured area" show reference data.

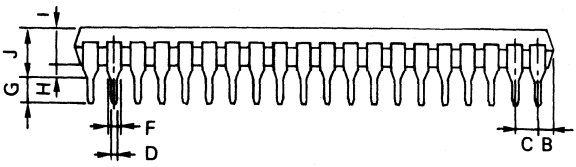
PACKAGE DIMENSIONS
μPD80C50HC/
μPD80C40HC
40 PIN PLASTIC DIP

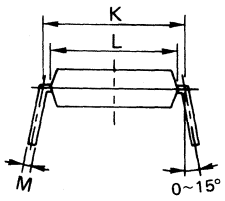
ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T. P.)	0.100 (T. P.)
D	0.50 ± 0.10	0.020 $^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6 ± 0.3	0.142 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T. P.)	0.600 (T. P.)
L	13.2	0.520
M	0.25 $^{+0.10}_{-0.05}$	0.010 $^{+0.004}_{-0.003}$
N	0.25	0.01

Notes: 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T. P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.



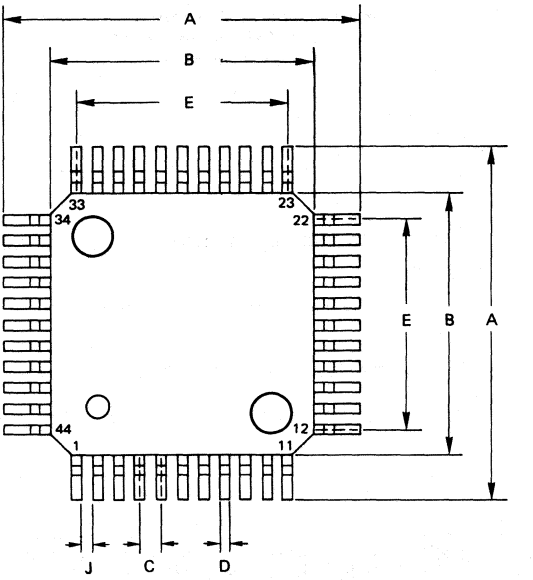


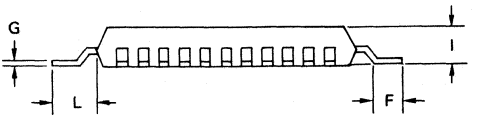


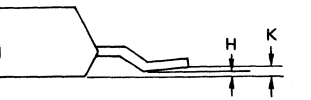
4

PACKAGE DIMENSIONS
μPD80C50HG
44 PIN PLASTIC
FLAT PACK

ITEM	MILLIMETERS	INCHES
A	13.6 ± 0.4	0.54 ± 0.016
B	10	.394
C	0.8 ± 0.15	.03 ± 0.006
D	.35 $^{+0.3}_{-0.1}$	.014 $^{+.01}_{-.004}$
E	8.0 ± 0.3	.315 ± .012
F	1.0 ± 0.2	.39 ± .008
G	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
H	0.0 ± 0.1	0.0 ± .004
I	1.4 $^{+0.2}_{-0.1}$	0.06 $^{+0.008}_{-0.004}$
J	0.2 min	0.008 min
K	0.0 ± 0.2	0.0 ± 0.008
L	1.8 ± 0.2	0.071 ± 0.008







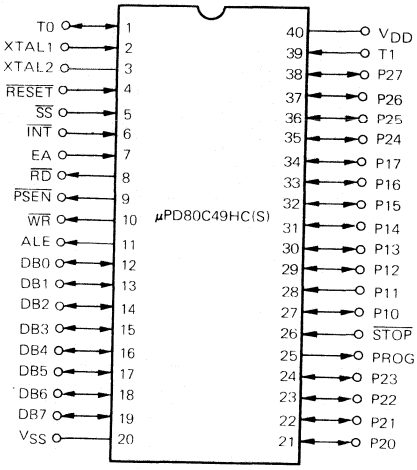
Lead bend (enlarged view)

The μPD80C49H is a single chip 8-bit microcomputer having 8-bit parallel processing ALU, ROM, RAM, I/O ports and control circuit on one CMOS chip. This microcomputer is provided with a standby function with consideration for low power consumption

FEATURES

- Extended temperature (T_a = −40 to +110 °C)
- Single chip 8-bit microcomputer
- 98 types of instructions
- Instruction cycle, 1.5 μs/10 MHz
- Operating function
  - Addition, logic operation, and decimal adjust
- ROM 2 K x 8 bits
- RAM 128 x 8 bits
- Stand-by function
- 8-level stack
- Dual Register Banks
- Interrupt capability
- Two test inputs
- On-chip 8 bit Timer/Counters
- Easily expandable Memory and I/O ports
- 27 lines Input/output ports
  - Input/output ports, 8 bits x 2
  - Data bus (common to I/O ports), 8 bits x 1
  - Sense Input (T0, T1, $\overline{INT}$) 1 bits x 3
- Single step function
- On chip Clock oscillator circuit
- CMOS
- Single power supply, +2.5 to +6.0 V
- 40 pin plastic DIP
- μPD8049H pin compatible

PIN CONFIGURATION (Top View)

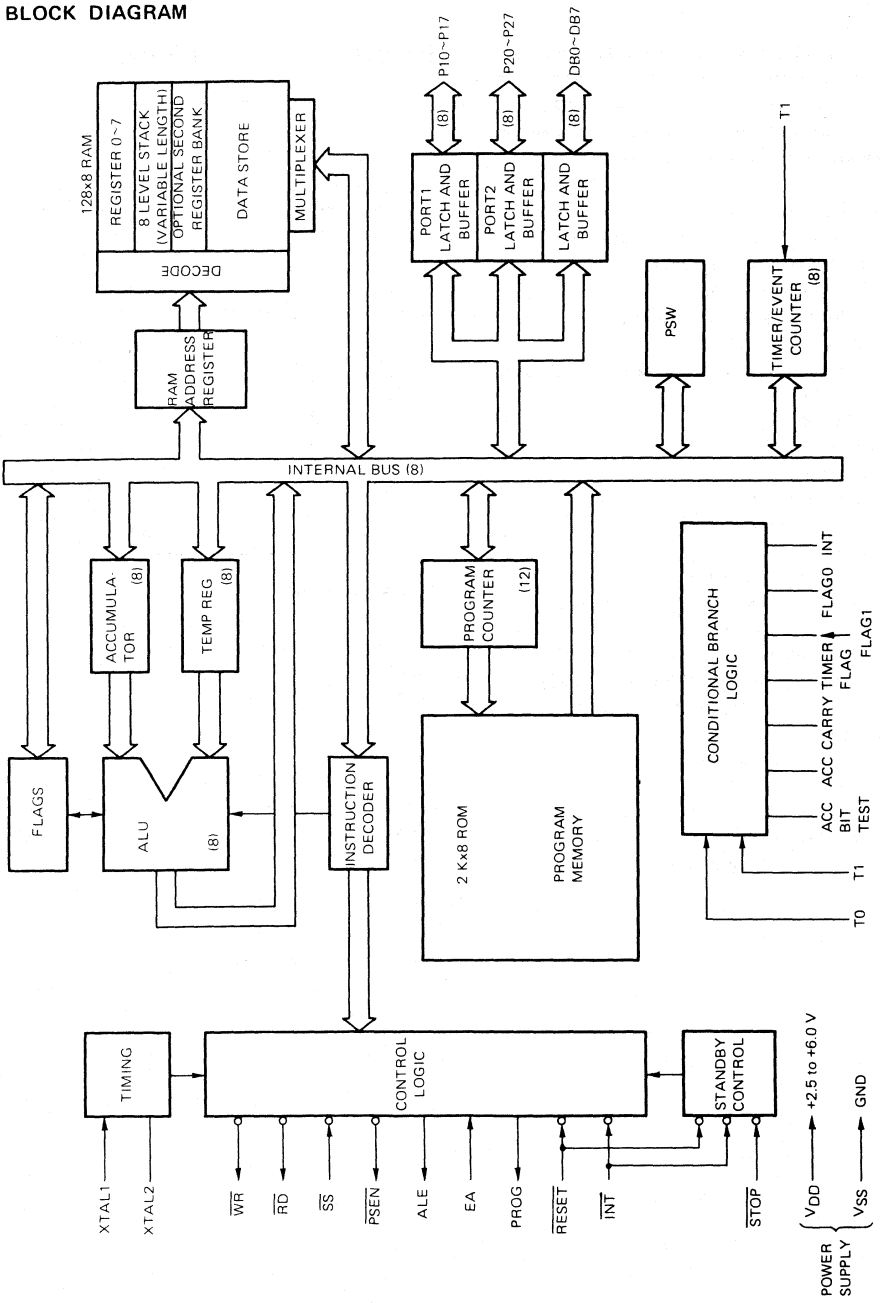


PIN FUNCTION

P10 ~ P17	:	Input/output port (PORT 1)
P20 ~ P27	:	Input/output port (PORT 2)
DB0 ~ DB7	:	Data bus (BUS PORT)
T0, T1	:	Test Input
$\overline{INT}$	:	Interrupt Input
$\overline{RD}$	:	Data Read Strobe Output
$\overline{WR}$	:	Data Write Strobe Output
ALE	:	Address Latch Enable Output
$\overline{PSEN}$	:	Program Strobe Enable Strobe Output
$\overline{RESET}$	:	Reset Input
$\overline{SS}$	:	Single step Input
EA	:	External Access Input
XTAL 1, 2	:	Crystal
$\overline{STOP}$	:	Stop Input

4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	−0.3 to +7	V
Input Voltage	V_I	−0.3 to V_{DD}+0.3	V
Output Voltage	V_O	−0.3 to V_{DD}+0.3	V
Operating Temperature	T_{opt}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +110	°C

DC CHARACTERISTICS (T_a = −40 °C to +110 °C, V_{DD} = +5 V ± 10 %, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage Low	V_{IL}		−0.3		+0.8	V
Input Voltage High	V_{IH}	Except XTAL1, XTAL2, $\overline{RESET}$, $\overline{SS}$	V_{DD}−2		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$	V_{DD}−1		V_{DD}	V
Output Voltage Low	V_{OL}	I_{OL}=1.2 mA			+0.45	V
Output Voltage High	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0 I_{OH}=−250 μA	2.4			V
	V_{OH1}(1)	I_{OH}=−3 μA (Type 0) PORT1, PORT2	2.4			V
		I_{OH}=−30 μA (Type 1) PORT1, PORT2	2.4			V
	V_{OH2}	All Outputs, I_{OH}=−0.2 μA	V_{DD}−0.5			V
Input Current	I_{ILP}(1)	PORT1, PORT2; $V_I \leq V_{IL}$ (Type 0)		−15	−40	μA
		PORT1, PORT2; $V_I \leq V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leq V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leq V_I \leq V_{DD}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leq V_I \leq V_{DD}$			±3	μA
Output Leakage Current	I_{LO}	$V_{SS} \leq V_O \leq V_{DD}$ High Impedance, BUS, T0 (3)			±1	μA
Standby Current	I_{DD1}	HALT Mode; t_{CY} =1.5 μs		1.5	3.0	mA
	I_{DD2}	STOP Mode (2)		1	50	μA
Supply Current (Total)	I_{DD}	t_{CY} =1.5 μs		6	15	mA
Data Retention Voltage	V_{DDDR}	at the hardware STOP mode ($\overline{STOP}$, $\overline{RESET} \leq$ 0.4 V) or RESET ($\overline{RESET} \leq$ 0.4 V)	2.5			V

4

DC CHARACTERISTICS (T_a = −40 °C to +110 °C, V_{DD} = +2.5 V to +6.0 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Voltage Low	V_{IL}			−0.3		0.18 V_{DD}	V
Input Voltage High	V_{IH}	Except XTAL1, XTAL2, $\overline{RESET}$, $\overline{SS}$		0.7 V_{DD}		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$		0.8 V_{DD}		V_{DD}	V
Output Voltage Low	V_{OL}	I_{OL}=0.5 mA				0.45	V
Output Voltage High	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0 I_{OH}=50 μA		0.75 V_{DD}			V
	V_{OH1}(1)	I_{OH}=−0.5 μA (Type 0) PORT1, PORT2		0.7 V_{DD}			V
		I_{OH}=−5 μA (Type 1) PORT1, PORT2		0.7 V_{DD}			V
Input Current	I_{LIP}(1)	PORT1, PORT2; $V_I \leqq V_{IL}$ (Type 0)			−15	−40	μA
		PORT1, PORT2; $V_I \leqq V_{IL}$ (Type 1)				−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqq V_{IL}$				−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leqq V_I \leqq V_{DD}$				±1	μA
	I_{LI2}	EA; $V_{SS} \leqq V_I \leqq V_{DD}$				±5	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_O \leqq V_{DD}$ (3) High Impedance, BUS, T0				±1	μA
Stand-by Current	I_{DD1}	HALT Mode	V_{DD}=3 V; t_{CY}=6 μs		0.3	0.6	mA
			V_{DD}=6 V; t_{CY}=1.5 μs		2.0	4.0	mA
	I_{DD2}	STOP Mode (2)	V_{DD}=3 V		1	50	μA
			V_{DD}=6 V		1	100	μA
Supply Current	I_{DD}	V_{DD}=3 V; t_{CY}=6 μs			2.0	4.0	mA
		V_{DD}=6 V; t_{CY}=1.5 μs			10	20	mA

Note 1: Option specification of type 0 and type 1 is available only for the μPD80C49H.

Note 2: The input pin voltage is $V_I \leqq V_{IL}$ or $V_I \leqq V_{IH}$.

Note 3: Output pins PORT1 and PORT2 specified as option in the type 2 are also included.

AC CHARACTERISTICS (T_a = 40 to 110 °C, V_{SS} = 0 V)

PARAMETER	SYMBOL	CONDITIONS	V_{DD}=+5 V±10 %		V_{DD}=2.5 to 6.0 V		UNIT
			MIN.	MAX.	MIN.	MAX.	
Cycle Time	t_{CY}		1.5		6		μs
ALE Pulse Width	t_{LL}	(4)	180		1230		ns
Address Setup before ALE	t_{AL}		190		1090		ns
Address Hold from ALE	t_{LA}		60		360		ns
Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}		550		2 800		ns
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}		400		2 200		ns
Data Setup before $\overline{WR}$	t_{DW}		450		2 400		ns
Data Hold after $\overline{WR}$	t_{WD}	(5)	60		360		ns
Data Hold after $\overline{RD}$, $\overline{PSEN}$	t_{DR}	(4)	0	120	0	400	ns
$\overline{RD}$ to Data in	t_{RD1}			400		2 200	ns
$\overline{PSEN}$ to Data in	t_{RD2}			250		1 600	ns
Address Setup before $\overline{WR}$	t_{AW}		450		2 250		ns
Address Setup before Data in ($\overline{RD}$)	t_{AD1}			900		4 350	ns
Address Setup before Data in ($\overline{PSEN}$)	t_{AD2}			650		3 350	ns
Address Float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}		135		735		ns
Address Float to $\overline{PSEN}$	t_{AFC2}		10		160		ns
ALE to Control Signal ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}		125		1 125		ns
ALE to Control Signal ($\overline{PSEN}$)	t_{LAFC2}		75		525		ns
Control Signal ($\overline{RD}$, $\overline{WR}$, PROG) to ALE	t_{CA1}		50		350		ns
Control Signal ($\overline{PSEN}$) to ALE	t_{CA2}		350		1 550		ns
Port Control Setup before Falling Edge of PROG	t_{CP}	(6)	110		560		ns
Port Control Hold after Falling Edge of PROG	t_{PC1}	(6) (7)	0	85	0	220	ns
	t_{PC2}	(6) (8)	220		1 400		ns
PROG to Time P2 Input must be Valid	t_{PR}	(6)		730		3 280	ns
Input Data Hold Time	t_{PF}		0	150	0	600	ns
Output Data Setup Time	t_{DP}		450		2 250		ns
Output Data Hold Time	t_{PD}		100		550		ns
PROG Pulse Width	t_{PP}		800		3 950		ns
PORT2 I/O Data Setup Time	t_{PL}		200		1 400		ns
PORT2 I/O Data Hold Time	t_{LP}		10		160		ns
ALE to PORT Output	t_{PV}			550		1 900	ns
T0 Clock Period	t_{OPRR}		300		1 200		ns

Note 4. Control Output: C_L = 80 pF, BUS Output: C_L = 150 pF

Note 5. C_L = 20 pF

Note 6. Control output: C_L = 80 pF

Note 7. At execution of MOVD A, P_p instruction

Note 8. At execution of MOVD P_p, A; ORLD P_p, A instruction

4

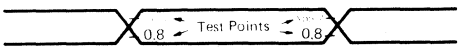
DEFINITION OF t_{CY} DEPENDENT BUS TIMING

PARAMETER	CALCULATION FORMULA	MIN./MAX.	UNIT
t_{LL}	(7/30) T-170	MIN.	ns
t_{AL}	(1/5) T-110	MIN.	ns
t_{LA}	(1/15) T-40	MIN.	ns
t_{CC1}	(1/2) T-200	MIN.	ns
t_{CC2}	(2/5) T-200	MIN.	ns
t_{DW}	(13/30) T-200	MIN.	ns
t_{WD}	(1/15) T-40	MIN.	ns
t_{DR}	(1/10) T-30	MAX.	ns
t_{RD1}	(2/5) T-200	MAX.	ns
t_{RD2}	(3/10) T-200	MAX.	ns
t_{AW}	(2/5) T-150	MIN.	ns
t_{AD1}	(23/30) T-250	MAX.	ns
t_{AD2}	(3/5) T-250	MAX.	ns
t_{AFC1}	(2/15) T-65	MIN.	ns
t_{AFC2}	(1/30) T-40	MIN.	ns
t_{LAFC1}	(1/5) T-75	MIN.	ns
t_{LAFC2}	(1/10) T-75	MIN.	ns
t_{CA1}	(1/15) T-50	MIN.	ns
t_{CA2}	(4/15) T-50	MIN.	ns
t_{CP}	(1/10) T-40	MIN.	ns
t_{PC2}	(4/15) T-200	MIN.	ns
t_{PR}	(17/30) T-120	MAX.	ns
t_{PF}	(1/10) T	MAX.	ns
t_{DP}	(2/5) T-150	MIN.	ns
t_{PD}	(1/10) T-50	MIN.	ns
t_{PP}	(7/10) T-250	MIN.	ns
t_{PL}	(4/15) T-200	MIN.	ns
t_{LP}	(1/30) T-40	MIN.	ns
t_{PV}	(3/10) T+100	MAX.	ns
t_{OPRR}	(1/5) T	MIN.	ns
t_{CY}	$(1/f_{XTAL})$ x 15		μs

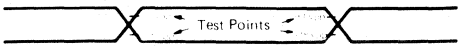
Remarks : $T = t_{CY}$

AC Test Input/Output Waveform

(1) V_{DD} = +5.0 V ± 10%

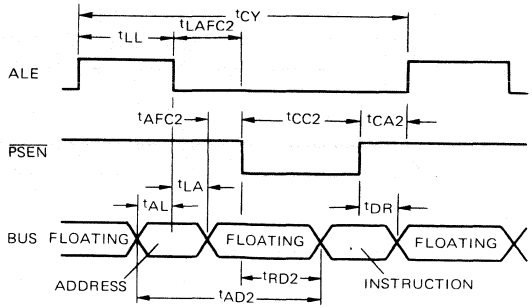


(2) V_{DD} = +2.5 V to +6.0 V

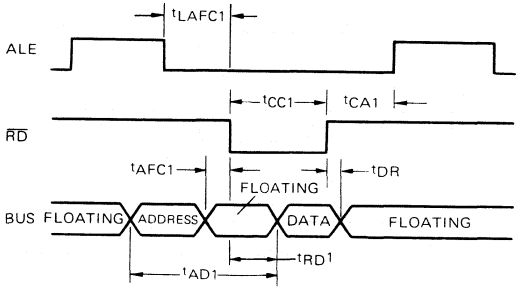


TIMING WAVEFORMS

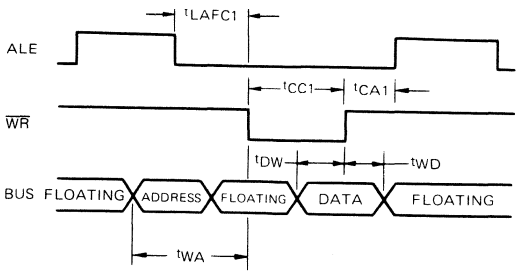
INSTRUCTION FETCH (External Program Memory)



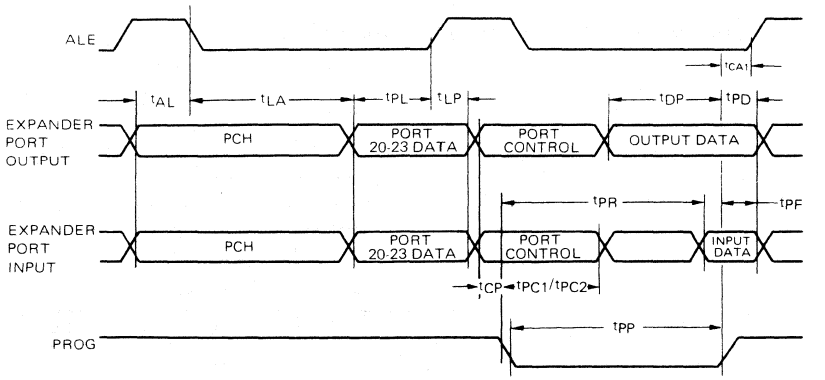
READ (External Data Memory)



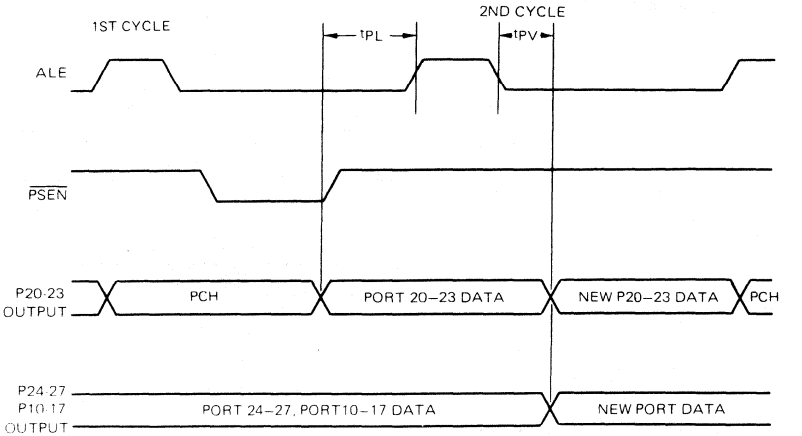
WRITE (External Data Memory)



PORT 2 EXPANSION TIMING



I/O PORT TIMING



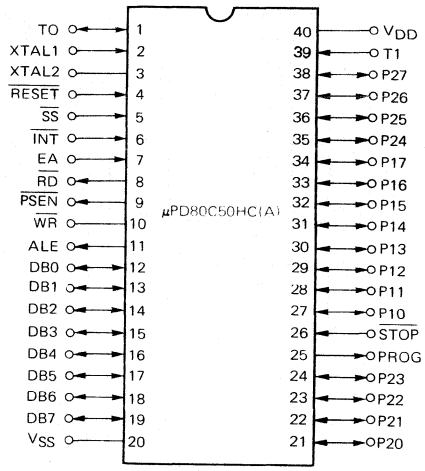
The μPD80C50HC(A) is a single chip microcomputer containing 8-bit CPU, ROM, RAM, I/O ports and control circuit on one CMOS chip.

The μPD80C50HC(A), fabricated by CMOS technology, realizes low power consumption and data retention is also available with less power consumption.

FEATURES

- Single chip 8-bit microcomputer
- 98 instructions
- Instruction cycle: 1.25 μs/12 MHz
- Operating function
  - Addition, logic operation, and decimal adjust
- ROM 4 K x 8 bits
- RAM 256 x 8 bits
- Stand-by function
- 8-level stack
- Two sets of working registers
- Interrupt capability
- Two test inputs
- Internal Timer/Event Counter
- Easy expandable Memory and I/O ports
- Input/output ports
  - Input/output ports: 8 bits x 2
  - Data bus (alternative for I/O ports): 8 bits x 1
- Single step function
- Internal Clock generator
- CMOS
- Single power supply: +2.5 to +6.0 V
- 40 pin plastic DIP

PIN CONNECTION (Top View)

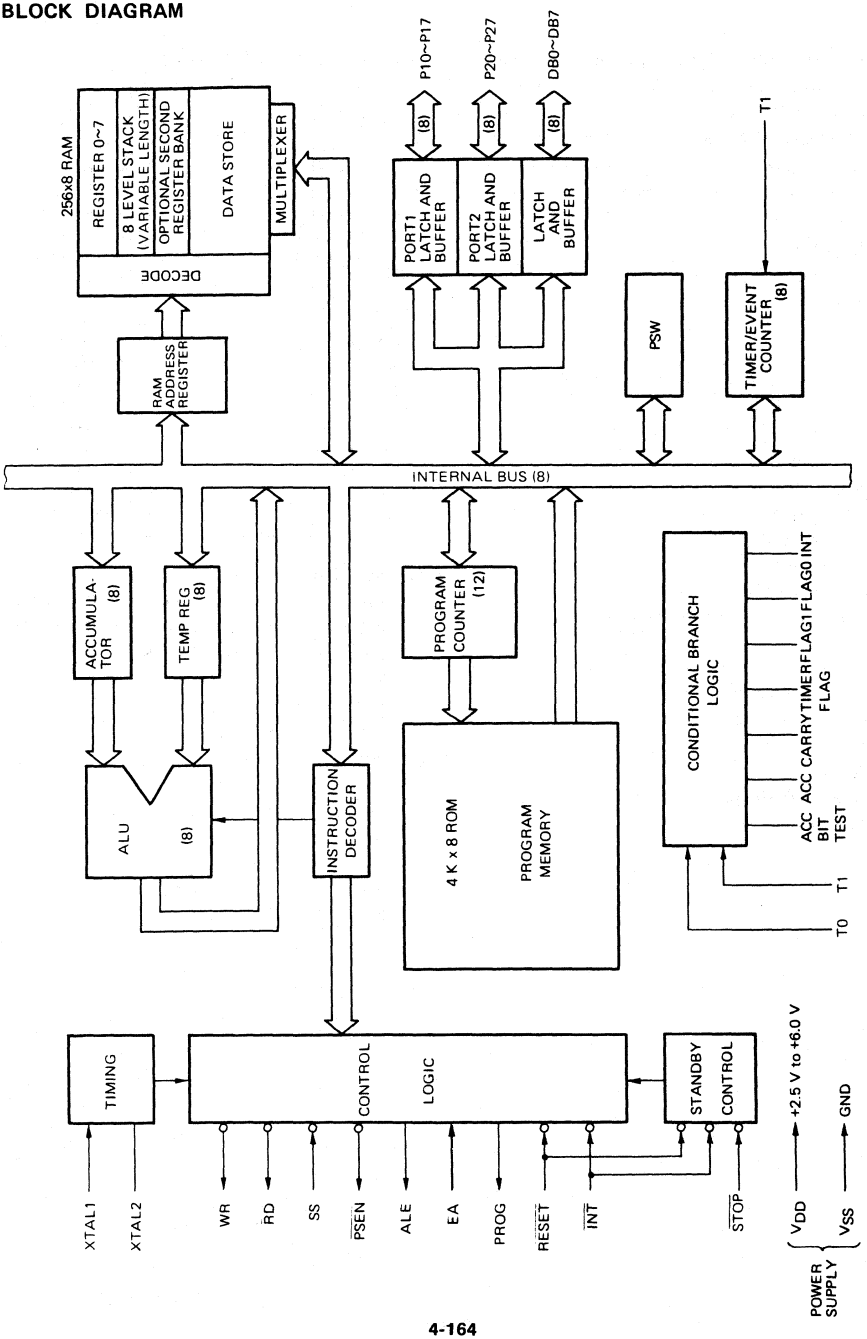


PIN IDENTIFICATIONS

P10~P17	:	Input/output port (PORT 1)
P20~P27	:	Input/output port (PORT 2)
DB0~DB7	:	Data bus (BUS)
T0, T1	:	Test
INT	:	Interrupt
RD	:	Read
WR	:	Write
ALE	:	Address Latch Enable
PSEN	:	Program Store Enable
RESET	:	Reset
SS	:	Single step
EA	:	External Access
XTAL1, 2	:	Crystal
STOP	:	Stop

4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V_{DD}	V_{SS} −0.3 to +7	V
Input Voltage	V_I	V_{SS} −0.3 to V_{DD} +0.3	V
Output Voltage	V_O	V_{SS} −0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input low voltage	V_{IL}		−0.3		0.8	V
Input high voltage	V_{IH}	(All except XTAL1, XTAL2, $\overline{RESET}$ $\overline{SS}$)	V_{DD}−2		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$	V_{DD}−1		V_{DD}	V
Output low voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output high voltage	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, LAE, PROG, T0; I_{OH} = −400 μA	2.4			V
	V_{OH1}	PORT1, PORT2; I_{OH} = −5 μA (Type 0)	2.4			V
		PORT1, PORT2; I_{OH} = 50 μA (Type 1)	2.4			V
	V_{OH2}	All outputs; I_{OH} = −0.2 μA	V_{DD}−0.5			V
Input current	I_{ILP}	PORT1, PORT2; $V_I \leqq V_{IL}$ (Type 0)		−15	−40	μA
		PORT1, PORT2; $V_I \leqq V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqq V_{IL}$			−40	μA
Input leakage current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leqq V_I \leqq V_{DD}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqq V_I \leqq V_{DD}$			±3	μA
Output leakage current	I_{LO}	BUS, T0, High impedance state (2) $V_{SS} \leqq V_O \leqq V_{DD}$			±1	μA
Standby current	I_{DD1}	HALT mode; t_{CY} = 1.25 μs		1.5	3.0	mA
	I_{DD2}	STOP mode (1)		1	20	μA
Supply current	I_{DD}	t_{CY} = 1.25 μs		6	18	mA
Data holding voltage	V_{DDDR}	Hardware STOP mode ($\overline{STOP}$, $\overline{RESET}$ ≦ 0.4 V) or reset ($\overline{RESET}$ ≦ 0.4 V)	2.0			V

Notes:

1) Input pin voltage $V_I \leqq V_{IL}$ or $V_I \geqq V_{IH}$
2) Includes PORT1 and PORT2 pins optionally specified with type 2.

4

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = +2.5 V to +6.0 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input low voltage	V_{IL}			−0.3		0.18 V_{DD}	V
Input high voltage	V_{IH}	(All except XTAL1, XTAL2, $\overline{RESET}$, $\overline{SS}$)		0.7 V_{DD}		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$		0.8 V_{DD}		V_{DD}	V
Input low voltage	V_{OL}	I_{OL} = 1.0 mA				0.45	V
Output high voltage	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; I_{OH} = −100 μA		0.75 V_{DD}			V
	V_{OH1}	PORT1, PORT2; I_{OH} = −1 μA (Type 0)		0.7 V_{DD}			V
		PORT1, PORT2; I_{OH} = −10 μA (Type 1)		0.7 V_{DD}			V
Input current	I_{ILP}	PORT1, PORT2; $V_I \leqq V_{IL}$ (Type 0)			−15	−40	μA
		PORT1, PORT2; $V_I \leqq V_{IL}$ (Type 1)				−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqq V_{IL}$				−40	μA
Input leakage current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leqq V_I \leqq V_{DD}$				±1	μA
	I_{LI2}	EA; $V_{SS} \leqq V_I \leqq V_{DD}$				±5	μA
Output leakage current	I_{LO}	BUS, T0 High impedance state (3) $V_{SS} \leqq V_O \leqq V_{DD}$				±1	μA
Standby current	I_{DD1}	HALT mode	V_{DD} = 3 V; t_{CY} = 5 μs		0.3	0.6	mA
			V_{DD} = 6 V; t_{CY} = 1.25 μs		2.0	4.0	mA
	I_{DD2}	STOP mode (2)	V_{DD} = 3 V		1	20	μA
			V_{DD} = 6 V		1	50	μA
Supply current	I_{DD}	V_{DD} = 3 V; t_{CY} = 5 μs			2.0	5.0	mA
		V_{DD} = 6 V; t_{CY} = 1.25 μs			10	25	mA

Notes:

1) Type 0, type 1 and type 2 options can be specified in μPD80C50H
2) Input pin voltage $V_I \leqq V_{IL}$ or $V_I \geqq V_{IH}$
3) Includes PORT1 and PORT2 pins optionally specified with type 2.

AC CHARACTERISTICS (T_a = −40 to + 85 ° C, V_{SS} = 0 V)

PARAMETER	SYMBOL	CONDITIONS	V_{DD}=+5 V ±10 %		V_{DD}=+2.5 to +6.0 V		UNIT
			MIN.	MAX.	MIN.	MAX.	
Cycle time	t_{CY}		1.25	150	5	150	μs
ALE pulse width	t_{LL}		125		995		ns
Address setup to ALE	t_{AL}		140		890		ns
Address hold from ALE	t_{LA}	(4)	45		295		ns
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}		425		2 300		ns
Control pulse width ($\overline{PSEN}$)	t_{CC2}		300		1 800		ns
Data setup before $\overline{WR}$	t_{DW}		340		1 965		ns
Data hold after $\overline{WR}$	t_{WD}	(5)	45		295		ns
Data hold after $\overline{RD}$, $\overline{PSEN}$	t_{DR}		0	95	0	470	ns
$\overline{RD}$ to data in	t_{RD1}			300		1 800	ns
$\overline{PSEN}$ to data in	t_{RD2}			175		1 300	ns
Address setup to $\overline{WR}$	t_{AW}		350		1 850		ns
Address setup to $\overline{RD}$ data in	t_{AD1}			700		3 585	ns
Address setup to $\overline{PSEN}$ data in	t_{AD2}	(4)		500		2 750	ns
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}		105		600		ns
Address float to $\overline{PSEN}$	t_{AFC2}		5		125		ns
ALE to $\overline{RD}$, $\overline{WR}$ delay	t_{LAFC1}		175		925		ns
ALE to $\overline{PSEN}$ delay	t_{LAFC2}		50		425		ns
$\overline{RD}$, $\overline{WR}$, PROG to ALE delay	t_{CA1}		35		285		ns
$\overline{PSEN}$ to ALE delay	t_{CA2}		280		1 285		ns
Port control setup to PROG	t_{CP}	(6)	85		460		ns
Port control hold from PROG	t_{PC1}	(6) (7)	0	80	0	200 (9)	ns
	t_{PC2}	(6) (8)	135		1 135		ns
Input data setup to PROG	t_{PR}	(6)		585		2 715	ns
Input data hold from PROG	t_{PF}		0	125	0	500	ns
Output data setup to PROG	t_{DP}		350		1 850		ns
Output data hold from PROG	t_{PD}		75		450		ns
PROG pulse width	t_{PP}	(6)	625		3 250		ns
Port 2 I/O data setup to ALE	t_{PL}		135		1 135		ns
Port 2 I/O data hold from ALE	t_{LP}		5		125		ns
ALE to port output	t_{PV}			475		1 600	ns
T0 output cycle time	t_{0PRR}		250		1 000		ns

Notes:

4) Control outputs C_L = 80 pF; BUS output: C_L = 150 pF

5) C_L = 20 pF

6) Control outputs: C_L = 80 pF

7) During execution of MOVD A, P_P

8) During execution of MOVD P_P, A, ANLD P_P, A, ORLD P_P, A

9) See supply voltage and port control hold time characteristic curves

t_{CY}-DEPENDENT BUS TIMING DEFINITIONS

PARAMETER	CALCULATION FORMULA	MIN./MAX.	UNIT
t_{LL}	(7/30) T−170	MIN.	ns
t_{AL}	(1/5) T−110	MIN.	ns
t_{LA}	(1/15) T−40	MIN.	ns
t_{CC1}	(1/2) T−200	MIN.	ns
t_{CC2}	(2/5) T−200	MIN.	ns
t_{DW}	(13/30) T−200	MIN.	ns
t_{WD}	(1/15) T−40	MIN.	ns
t_{DR}	(1/10) T−30	MAX.	ns
t_{RD1}	(2/5) T−200	MAX.	ns
t_{RD2}	(3/10) T−200	MAX.	ns
t_{AW}	(2/5) T−150	MIN.	ns
t_{AD1}	(23/30) T−250	MAX.	ns
t_{AD2}	(3/5) T−250	MAX.	ns
t_{AFC1}	(2/15) T−65	MIN.	ns
t_{AFC2}	(1/30) T−40	MIN.	ns
t_{LAFC1}	(1/5) T−75	MIN.	ns
t_{LAFC2}	(1/10) T−75	MIN.	ns
t_{CA1}	(1/15) T−50	MIN.	ns
t_{CA2}	(4/15) T−50	MIN.	ns
t_{CP}	(1/10) T−40	MIN.	ns
t_{PC2}	(4/15) T−200	MIN.	ns
t_{PR}	(17/30) T−120	MAX.	ns
t_{PF}	(1/10) T	MAX.	ns
t_{DP}	(2/5) T−150	MIN.	ns
t_{PD}	(1/10) T−50	MIN.	ns
t_{PP}	(7/10) T−250	MIN.	ns
t_{PL}	(4/15) T−200	MIN.	ns
t_{LP}	(1/30) T−40	MIN.	ns
t_{PV}	(3/10) T+100	MAX.	ns
t_{OPRR}	(1/5) T	MIN.	ns
t_{CY}	$(1/f_{XTAL})$x15		μs

Remarks: T = t_{CY}

Section 5: Sentry Test Tapes

Sentry Test Tape

NEC offers a number of sentry test tapes for customer entrance testing. These test tapes run on sentry VII and check all AC and DC parameters. Test tapes are available for the following devices:

μPD7807
μPD7810
μPD7811
μPD78C11
μPD78C14
μPD8035HL
μPD8039HL
μPD8041AH
μPD8048H
μPD8049H
μPD80C48H
μPD80C49H

NEC Customer Services

NEC's Commitment to Information

Our offices throughout Europe are always at your service for comprehensive support. Here are some of the technical services we provide:

- INSECT
- Seminars
- Update service
- Hotline
- Mailing list
- University program

INSECT

INformation **S**ystem and **E**lectronic **CaT**alog.

This is an on-line information service. Via a telephone link you can call up the latest data on all VLSI devices available from NEC. This includes enhancements, news and the most recent application know-how.

The service is free to our customers and other interested parties. For a menu-driven guest session, you can dial in to INSECT via the international packet switching network – in Germany this is DATEX-P – using of these numbers
45 21 10 13 020/030
and responding to the request for USERNAME and PASSWORD simply with "customer".

Seminars

No-one is more aware than NEC of the difference that a brief intensive training course can make to your mastery of advanced and often complex devices. We hold regular workshops and seminars at local NEC offices, in our Düsseldorf headquarters, or on customer premises. For information on NEC workshops and seminars, please contact your nearest office.

Update Service

When you buy an evaluation package from NEC, you become automatically entitled to one year's free updates for both hardware and software. All updates reach you fast and reliably via a courier service. In a field where rapid changes are the norm, you can be thus be sure of working with the most up-to-date development tools.

Hotlines

NEC's offices located throughout Europe are responsible for technical support and customer services. On the back cover of this brochure you can check which office is most convenient for you to contact. You are also welcome to contact our European headquarters in Düsseldorf directly.

Mailing list

Our engineering staff produces frequent additions to the available technical documentation in the form of application notes, product news and technical letters. If you would like to be included on our mailing list for this documentation, please inform us.

University Program

Many of our products, because of their complexity and dedicated application support through EB tools, are interesting subjects for graduate studies. NEC is always ready to discuss this possibility.

EUROPEAN DISTRIBUTORS

AUSTRIA
G. DEMEL
HANDELSGESELLSCHAFT MBH
HOFFMEISTERGASSE 8-10/1
1120 WIEN
TEL.: (222) 81 32 50 70

BELGIUM
INTRA ELECTRONICS P.V.B.A.
BOSUIL 80, BUS 1
2100 DEURNE
TEL.: (03) 3 25 23 20
TLX.: 31102

MALCHUS ELECTRONICS B.V.B.A.
PLANTIN EN MORETUSLEI 172
2018 ANTWERPEN
TEL.: (03) 2 35 32 72
TLX.: 33 637

INNOCIRCUIT BENELUX B.V.B.A.
PLANTIN EN MORETUSLEI 172
2018 ANTWERPEN
TEL.: (03) 2 35 32 72 (B)
TEL.: (00 31) 10-4 27 77 80
TLX.: 33 637

DENMARK
MER-EL A/S
VED KLAEDEBO 18
2970 HOERSHOLM
TEL.: (2) 57 10 00
TLX.: 37 360

FINLAND
OY COMDAX AB
ITAELAHDENKATU 23A
PI 1
00210 HELSINKI
TEL.: (0) 67 02 77
TLX.: 57 125 876

FRANCE
ASAP
2 AVENUE DES CHAUMES
78180 MONTIGNY LE BRETONNEUX
TÉL.: (1) 30 43 82 33
TLX.: 698 887

C.C.I.
5, RUE MARCELIN BERTHELOT
B.P. 92
92164 ANTONY
TÉL.: (1) 46 66 21 82
TLX.: 203 881

CGE COMPOSANTS
32 RUE GRANGE DAME ROSE
92360 MEUDON
TÉL.: (1) 46 30 24 25
TLX.: 632 118

PANTEC (GROUPE SCIENTECH)
29 RUE MARCEL DASSAULT
92100 BOULOGNE
TÉL.: (1) 46 20 06 74
TLX.: 633 048

GERMANY
BIT-ELECTRONIC AG
DINGOLFINGER STRASSE 6
8000 MÜNCHEN 80
TEL.: (0 89) 41 80 07-0
TLX.: 5 212 931

GLEICHMANN + CO ELECTRONICS GMBH
WORMSER STRASSE 34
6710 FRANKENTHAL
TEL.: (0 62 33) 2 50 56
TLX.: 4 65 270

GLYN GMBH
SCHÖNE AUSSICHT 30
6272 NIEDERNHAUSEN
TEL.: (0 61 27) 80 77
TLX.: 4 186 911

H3W ELEKTRONIK VERTRIEBS GMBH
STAHLGRUBERRING 12
8000 MÜNCHEN 82
TEL.: (0 89) 42 92 71
TLX.: 5 214 514

MICROSCAN GMBH
ÜBERSEERING 31
2000 HAMBURG 60
TEL.: (0 40) 6 32 00 30
TLX.: 2 13 288

REIN ELEKTRONIK GMBH
LÖTSCHERWEG 66
4054 NETTETAL 1
TEL.: (0 21 53) 73 31 11
TLX.: 8 54 251

SYSTEM ELEKTRONIK VERTRIEBS GMBH
HEESFELD 4
3300 BRAUNSCHWEIG
TEL.: (05 31) 31 40 95
TLX.: 9 52 351

ULTRATRONIK GMBH
GEWERBESTRASSE 4
8036 HERRSCHING
TEL.: (0 81 52) 37 09-0
TLX.: 5 26 459

UNIELECTRONIC VERTRIEBS GMBH
IM GEFIERTH 11 A
6072 DREIEICH 1 B. FRANKFURT
TEL.: (0 61 03) 3 51 75
TLX.: 4 11 213

ITALY
ADELSY S.R.L.
VIA DEL FONDITORE, 5
LOCALITA ROVERI
40127 BOLOGNA
TEL.: (51) 532119
TLX.: 510 226

CLAITRON S.P.A.
VIA GALLARATE, 211
20151 MILANO
TEL.: (1) 33404000
TLX.: 313 843

DIS.EL. S.P.A.
VIA ALA DI STURA 71
10148 TORINO
TEL.: (011) 2201522
TLX.: 215 118

MELCHIONI S.P.A.
VIA COLLETTA, 37
20135 MILANO
TEL.: (01) 57941
TLX.: 315 293

NETHERLANDS
MALCHUS B.V.
FOKKERSTRAAT 511
3125 BD SCHIEDAM
TEL.: (10) 4 27 77 77
TLX.: 21 598

INNOCIRCUIT BENELUX B.V.
POSTBUS 48
3100 AA SCHIEDAM
TEL.: (10) 4 27 77 80
TLX.: 21 598

INTRA ELECTRONICS B.V.
GULBERG 33
5674 TE NUENEN
TEL.: (40) 83 80 09
TLX.: 59 418

NORWAY
JAKOB HATTELAND ELECTRONIC A/S
P.B. 25
5578 NEDRE VATS
TEL.: (47) 63 111
TLX.: 428 50

PORTUGAL
AMPEREL S.A.
AV. FONTES PEREIRA DE MELO 47, 4D
1000 LISBOA
TEL.: (1) 53 26 98
TLX.: 18588

SPAIN
COMELTA SA
EMILIO MUNOZ 41. NAVE 1-1-2
28037 MADRID
TEL.: (1) 7 54 30 77
TLX.: 42 007

VENCO
CALLE GALILEO 249
08028 BARCELONA
TEL.: (3) 330 97 51
TLX.: 98 266

SWEDEN
NAX AB KOMPONENTBOLAGET
BOX 4115
17104 SOLNA
TEL.: (8) 98 51 40
TLX.: 17912

NORDQVIST & BERG
BOX 1458
17128 SOLNA
TEL.: (8) 7 64 67 10
TLX.: 10407

TH'S ELEKTRONIK
BOX 3027
16303 SPAANGA
TEL.: (8) 36 29 70
TLX.: 11145

SWITZERLAND
MEMOTEC AG
GASWERKSTRASSE 32
4901 LANGENTHAL
TEL.: (63) 28 11 22
TLX.: 9 82 550

UNITED KINGDOM
2001 ELECTRONIC COMPONENTS
WOOLMERS WAY
STEVENAGE
HERTS
SG1 3AJ
TEL.: (4 38) 74 20 01
TLX.: 827 701

ANZAC COMPONENTS LIMITED
822, YEOVIL ROAD
SLOUGH TRADING ESTATE
SLOUGH
BERKSHIRE
SL1 4JA
TEL.: (62 86) 44 11
TLX.: 847 949

CELDIS LIMITED
37, LOVEROCK ROAD
READING
BERKSHIRE
RG3 1EL
TEL.: (7 34) 58 51 71
TLX.: 848 370

IMPULSE ELECTRONICS LIMITED
HAMMOND HOUSE
CATERHAM
SURREY
CR3 6XG
TEL.: (8 83) 4 70 11
TLX.: 291 496

S.T.C. MULTICOMPONENTS LIMITED
EDINBURGH WAY
HARLOW
ESSEX
CM20 2DF
TEL.: (2 79) 44 11 44
TLX.: 818 763

V.S.I. ELECTRONICS (UK) LIMITED
ROYDONBURY INDUSTRIAL PARK
HORSECROFT ROAD
HARLOW
ESSEX
CM19 5BY
TEL.: (2 79) 2 96 66
TLX.: 81 387